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Understanding Embedded - FPGAs (Field Programmable Gate Array)

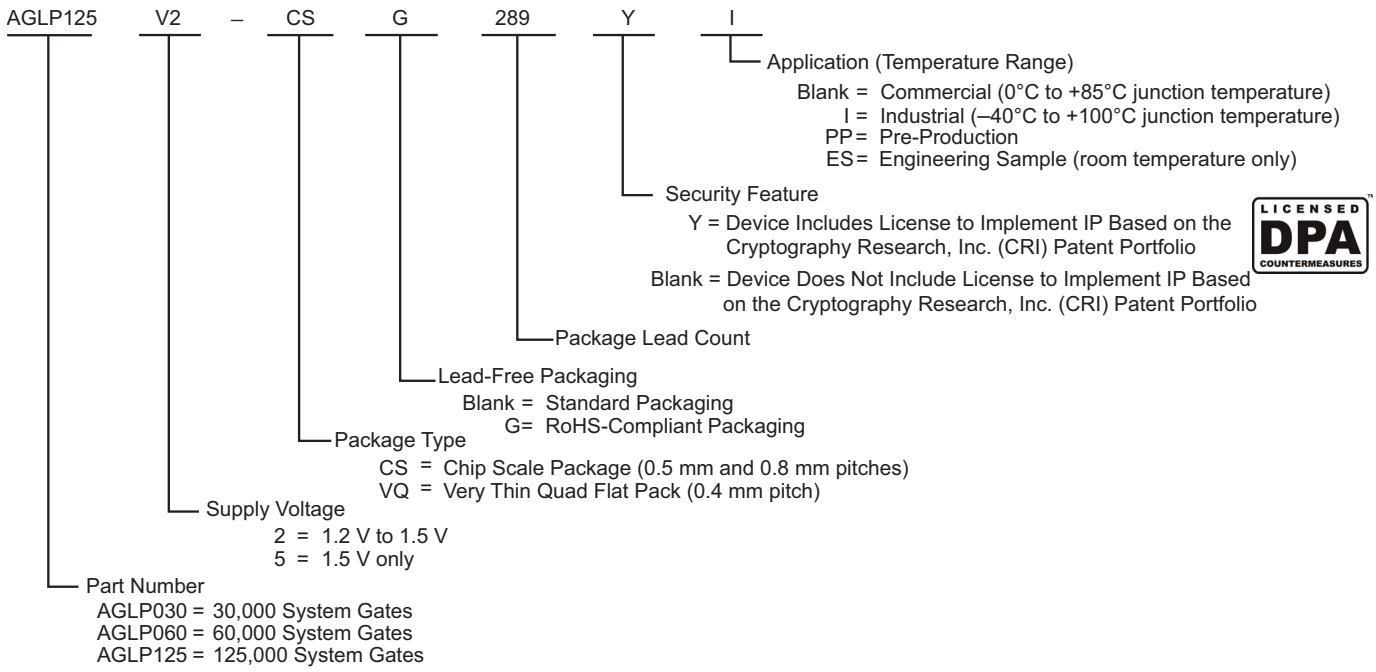
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	101
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v5-vqg128i

IGLOO PLUS Ordering Information



1. *Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.*
2. *"G" indicates RoHS-compliant packages.*

Temperature Grade Offerings

Package	AGLP030	AGLP060	AGLP125
CS201	C, I	C, I	–
CS281	–	–	C, I
CS289	C, I	C, I	C, I
VQ128	C, I	–	–
VQ176	–	C, I	–

Notes:
1. *C = Commercial temperature range: 0°C to 85°C junction temperature.*
2. *I = Industrial temperature range: –40°C to 100°C junction temperature.*

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/company/contact/default.aspx.

Table of Contents

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature [1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Table 2-24 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY})	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	5 pF	–	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.29	0.19	1.19	1.40	0.67	2.32	1.94	2.65	3.27	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns
1.2 V LVCMOS	2 mA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns
1.2 V LVCMOS Wide Range[3]	100 µA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Fully Registered I/O Buffers with Asynchronous Clear

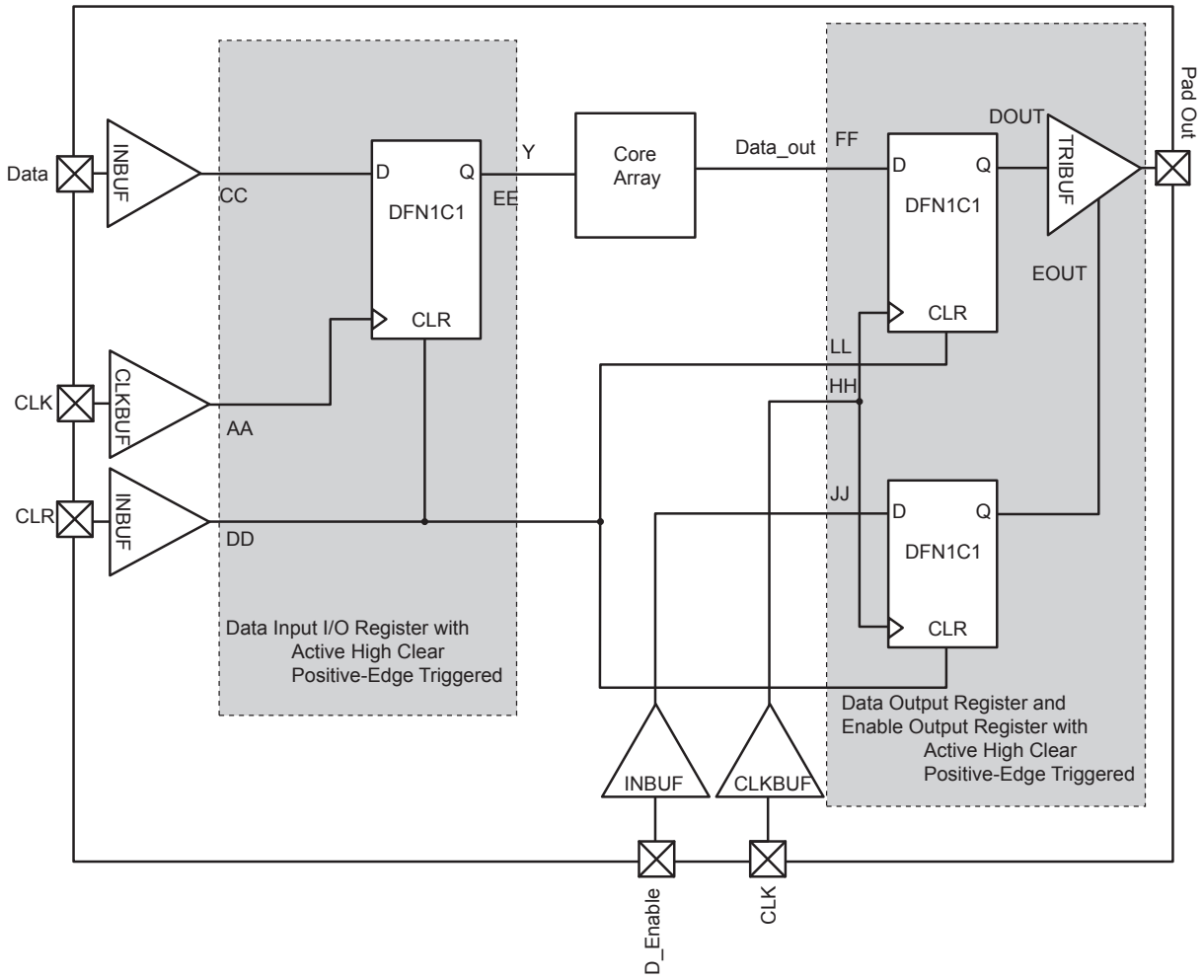


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

Output Register

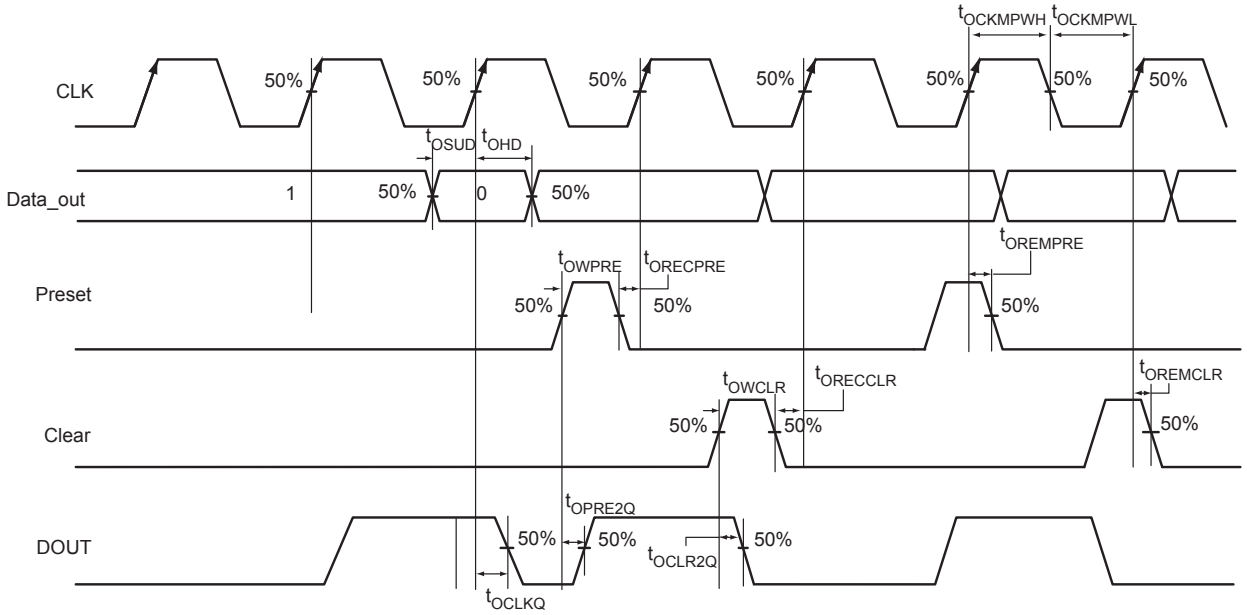


Figure 2-15 • **Output Register Timing Diagram**

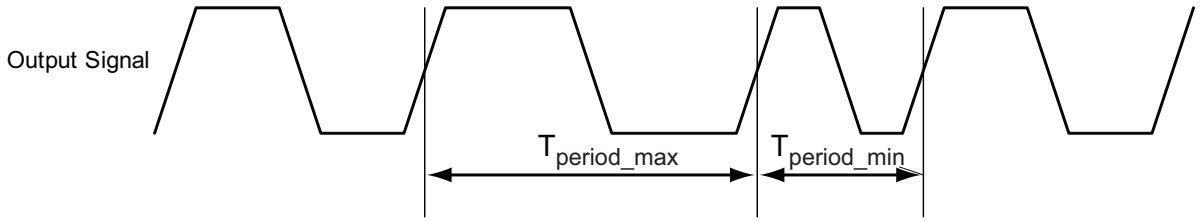
Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-22 • **Peak-to-Peak Jitter Definition**

Embedded SRAM and FIFO Characteristics

SRAM

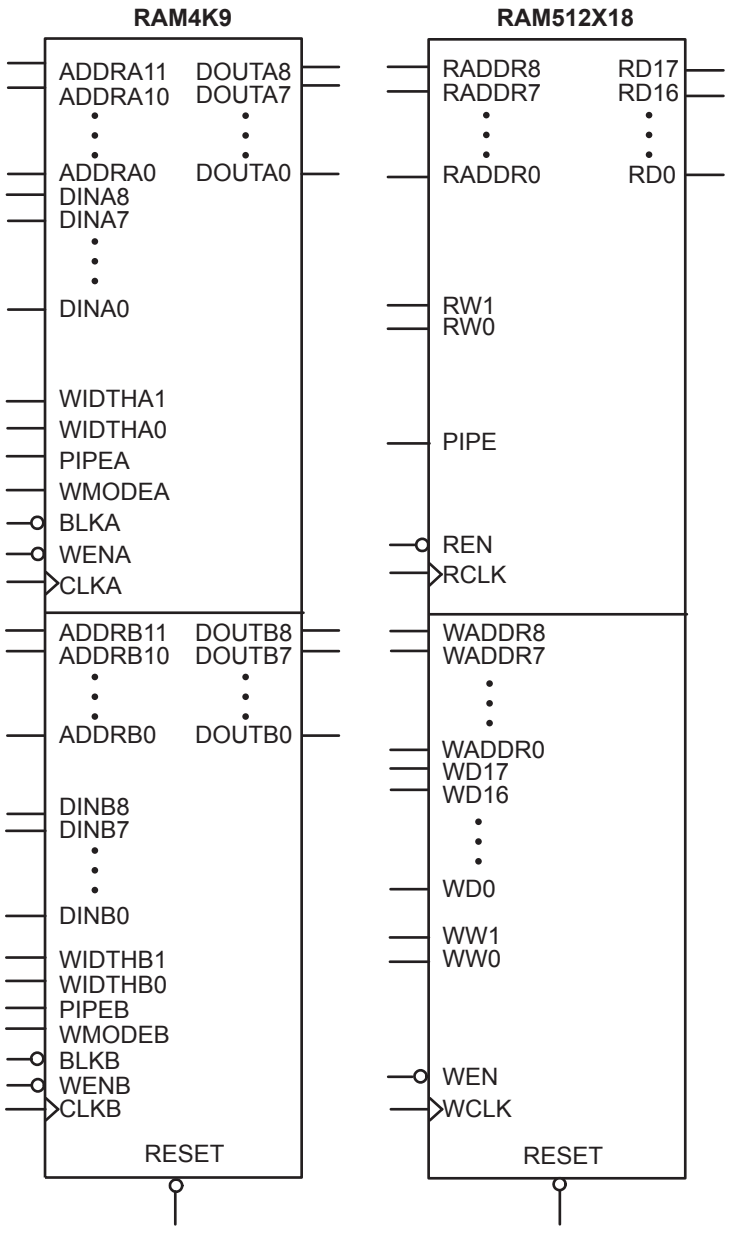


Figure 2-23 • **RAM Models**

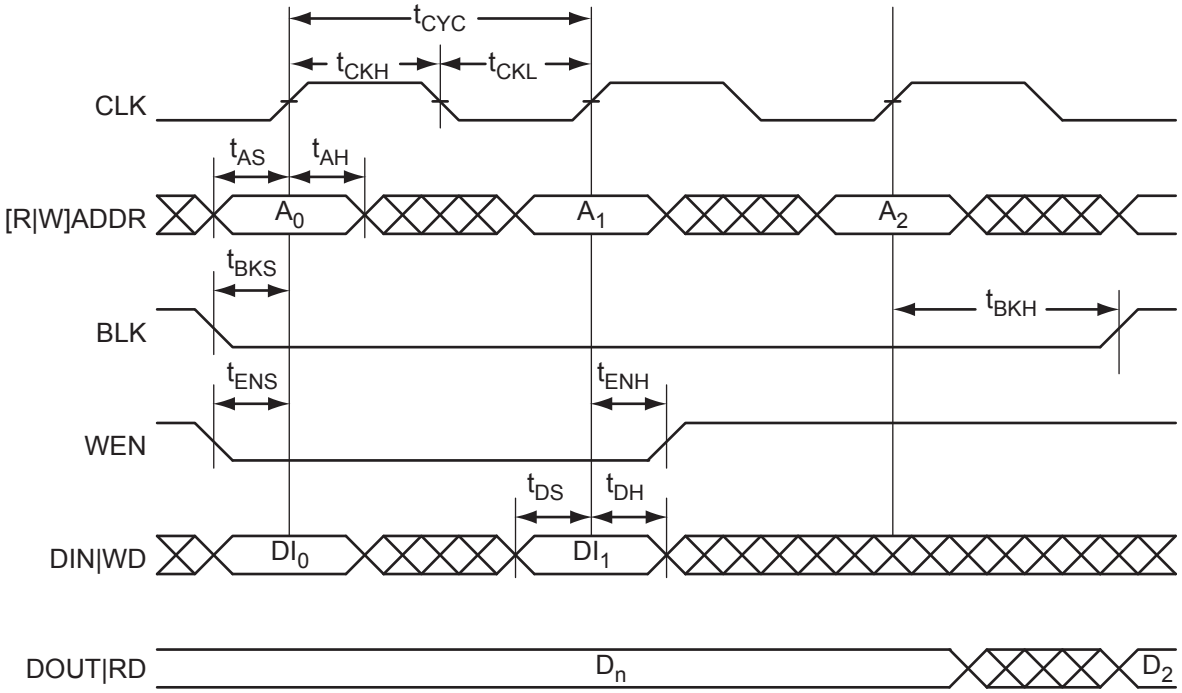


Figure 2-26 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

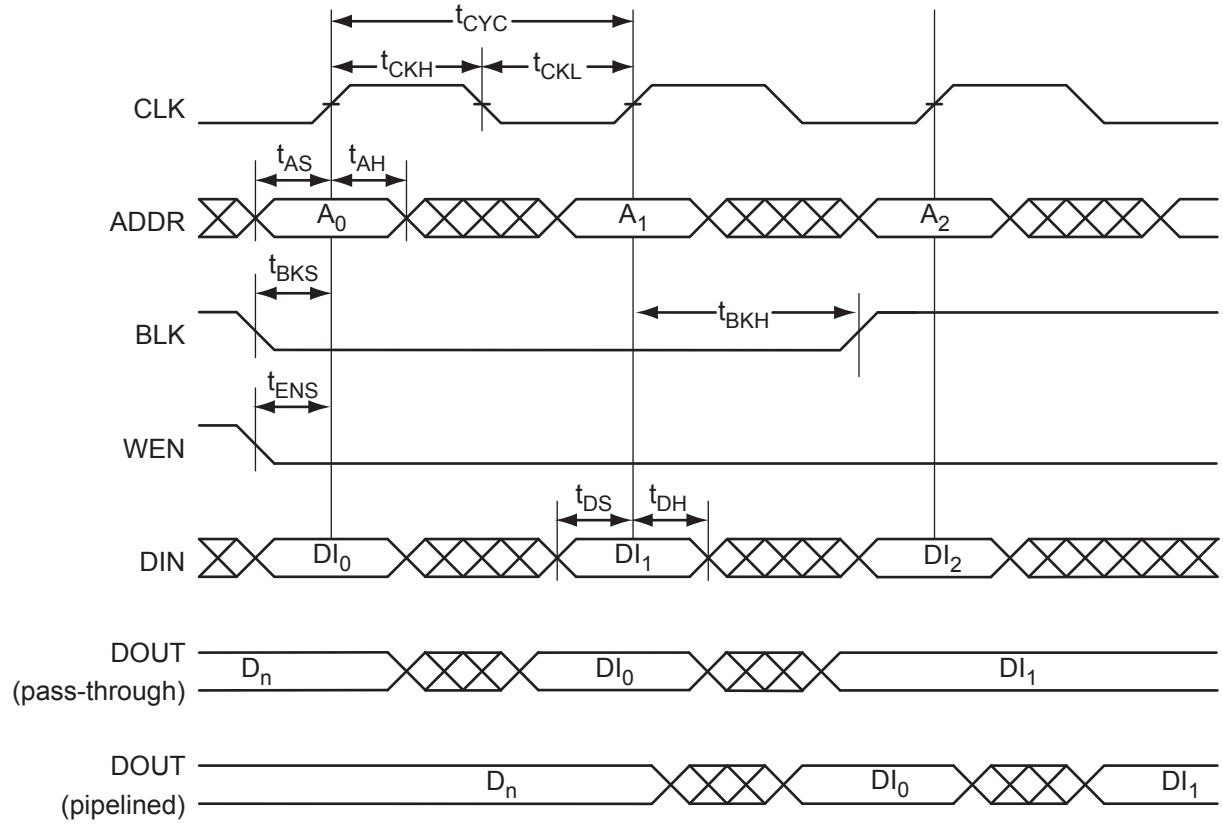


Figure 2-27 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

Table 2-95 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.29	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.36	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	3.21	ns
	RESET Low to data out Low on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

***Table 2-97* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.30	ns
t_{DH}	Input Data (WD) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	3.41	ns
	RESET Low to Data Out Low on RD (pipelined)	3.41	ns
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO PLUS V5 devices, and 1.2 V or 1.5 V for IGLOO PLUS V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO PLUS V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are four I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOO PLUS V5 devices
- 1.2 V or 1.5 V for IGLOO PLUS V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed signal FPGAs " chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on IGLOO PLUS devices.

FF Flash*Freeze Mode Activation Pin

The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

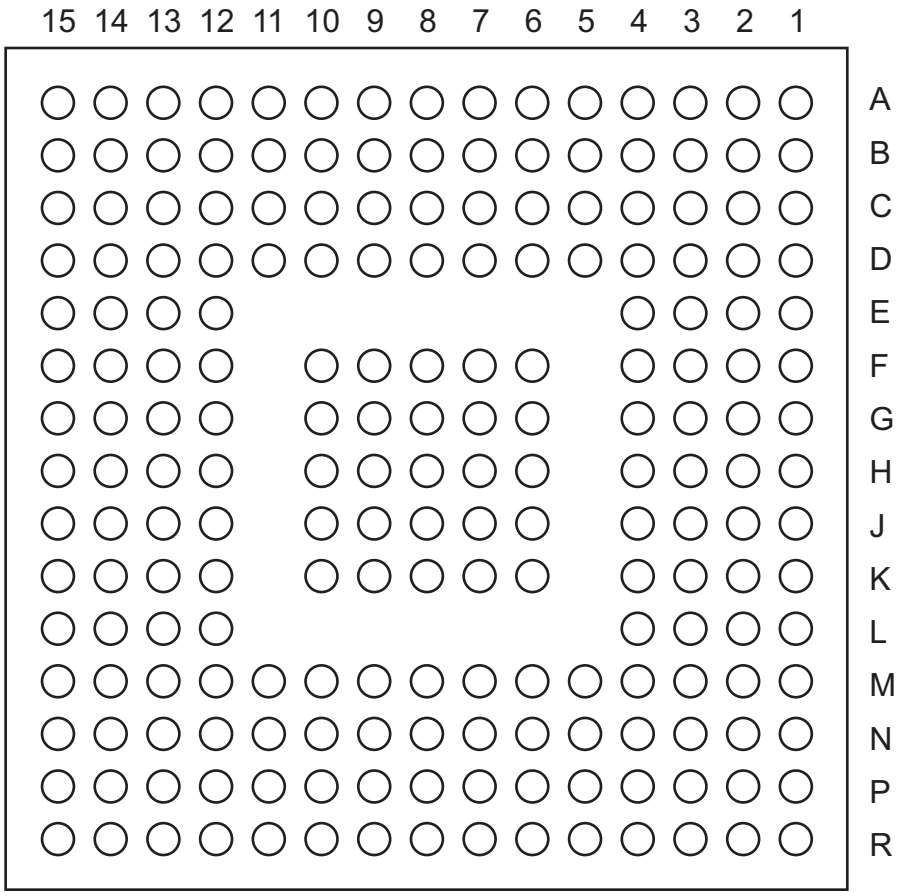
Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO and ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS Device Family User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 • **Flash*Freeze Pin Location in IGLOO PLUS Devices**

Package	Flash*Freeze Pin
CS281	W2
CS201	R4
CS289	U1
VQ128	34
VQ176	47

CS201



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS201	
Pin Number	AGLP030 Function
A1	NC
A2	IO04RSB0
A3	IO06RSB0
A4	IO09RSB0
A5	IO11RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO18RSB0
A9	IO24RSB0
A10	IO26RSB0
A11	IO27RSB0
A12	IO31RSB0
A13	NC
A14	NC
A15	NC
B1	NC
B2	NC
B3	IO08RSB0
B4	IO05RSB0
B5	IO07RSB0
B6	IO15RSB0
B7	IO14RSB0
B8	IO16RSB0
B9	IO20RSB0
B10	IO22RSB0
B11	IO34RSB0
B12	IO29RSB0
B13	NC
B14	NC
B15	NC
C1	NC
C2	NC
C3	GND
C4	IO00RSB0
C5	IO02RSB0

CS201	
Pin Number	AGLP030 Function
C6	IO12RSB0
C7	IO23RSB0
C8	IO19RSB0
C9	IO28RSB0
C10	IO32RSB0
C11	IO35RSB0
C12	NC
C13	GND
C14	IO41RSB1
C15	IO37RSB1
D1	IO117RSB3
D2	IO118RSB3
D3	NC
D4	GND
D5	IO01RSB0
D6	IO03RSB0
D7	IO10RSB0
D8	IO21RSB0
D9	IO25RSB0
D10	IO30RSB0
D11	IO33RSB0
D12	GND
D13	NC
D14	IO36RSB1
D15	IO39RSB1
E1	IO115RSB3
E2	IO114RSB3
E3	NC
E4	NC
E12	NC
E13	NC
E14	GDC0/IO46RSB1
E15	GDB0/IO48RSB1
F1	IO113RSB3
F2	IO116RSB3

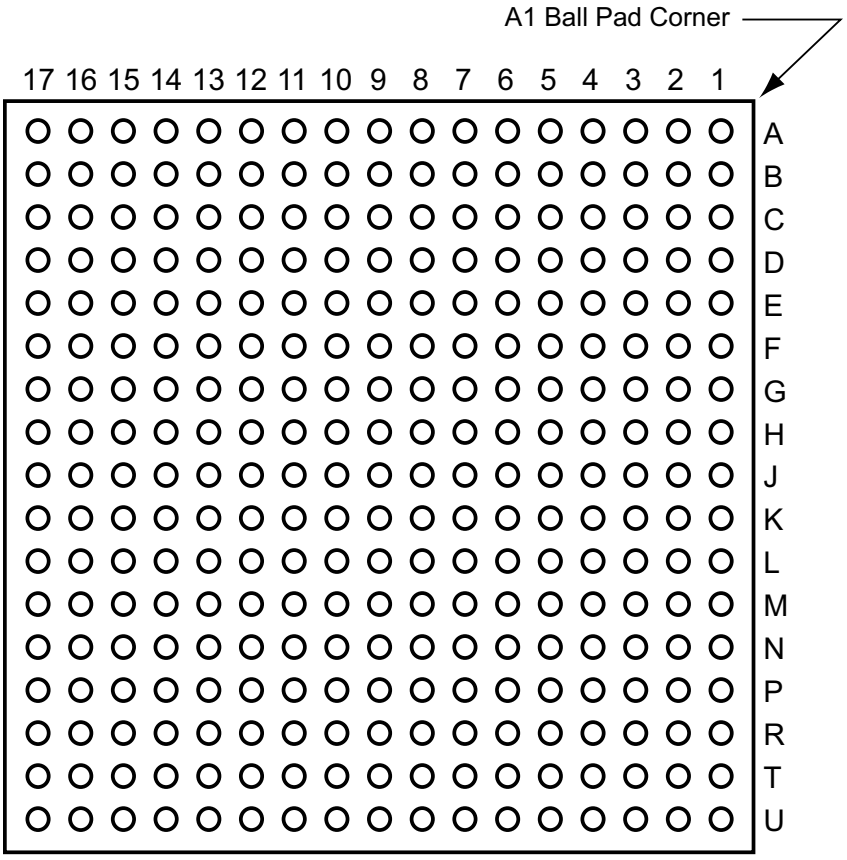
CS201	
Pin Number	AGLP030 Function
F3	IO119RSB3
F4	IO111RSB3
F6	GND
F7	VCC
F8	VCCIB0
F9	VCCIB0
F10	VCCIB0
F12	NC
F13	NC
F14	IO40RSB1
F15	IO38RSB1
G1	NC
G2	IO112RSB3
G3	IO110RSB3
G4	IO109RSB3
G6	VCCIB3
G7	GND
G8	VCC
G9	GND
G10	GND
G12	NC
G13	NC
G14	IO42RSB1
G15	IO44RSB1
H1	NC
H2	GEB0/IO106RSB3
H3	GEC0/IO108RSB3
H4	NC
H6	VCCIB3
H7	GND
H8	VCC
H9	GND
H10	VCCIB1
H12	IO54RSB1
H13	GDA0/IO47RSB1

CS281	
Pin Number	AGLP125 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO77RSB1
H16	GCB0/IO82RSB1
H18	GCA1/IO83RSB1
H19	GCA2/IO85RSB1
J1	VCOMPLF
J2	GFA0/IO189RSB3
J4	VCCPLF
J5	GFC0/IO193RSB3
J7	GFA2/IO188RSB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO79RSB1
J15	GCA0/IO84RSB1
J16	GCB2/IO86RSB1
J18	IO76RSB1
J19	IO78RSB1
K1	VCCIB3
K2	GFA1/IO190RSB3
K4	GND
K5	IO19RSB0
K7	IO197RSB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO87RSB1

CS281	
Pin Number	AGLP125 Function
K15	IO89RSB1
K16	GND
K18	IO88RSB1
K19	VCCIB1
L1	GFB2/IO187RSB3
L2	IO185RSB3
L4	GFC2/IO186RSB3
L5	IO184RSB3
L7	IO199RSB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO95RSB1
L15	IO91RSB1
L16	NC
L18	IO90RSB1
L19	NC
M1	IO180RSB3
M2	IO179RSB3
M4	IO181RSB3
M5	IO183RSB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO122RSB2
M16	IO93RSB1
M18	IO92RSB1
M19	NC
N1	IO178RSB3
N2	IO175RSB3

CS281	
Pin Number	AGLP125 Function
N4	IO182RSB3
N5	IO161RSB2
N7	GEA2/IO164RSB2
N8	VCCIB2
N9	IO137RSB2
N10	IO135RSB2
N11	IO131RSB2
N12	VCCIB2
N13	VPUMP
N15	IO117RSB2
N16	IO96RSB1
N18	IO98RSB1
N19	IO94RSB1
P1	IO174RSB3
P2	GND
P3	IO176RSB3
P4	IO177RSB3
P5	GEA0/IO165RSB3
P15	IO111RSB2
P16	IO108RSB2
P17	GDC1/IO99RSB1
P18	GND
P19	IO97RSB1
R1	IO173RSB3
R2	IO172RSB3
R4	GEC1/IO170RSB3
R5	GEB1/IO168RSB3
R6	IO154RSB2
R7	IO149RSB2
R8	IO146RSB2
R9	IO138RSB2
R10	IO134RSB2
R11	IO132RSB2
R12	IO130RSB2
R13	IO118RSB2
R14	IO112RSB2

CS289



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx .

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

Revision	Changes	Page
Revision 17 (December 2015)	Updated Commercial and Industrial temperature range to show junction temperature in "IGLOO PLUS Ordering Information" section and "Temperature Grade Offerings" section (SAR 73547).	1-III, 1-IV
	Removed Ambient temperature parameter in Table 2-2 • Recommended Operating Conditions[1,2] (SAR 73547).	2-2
	Table notes are added to Table 2-2 • Recommended Operating Conditions[1,2] stating that: • VMV pins must be connected to the corresponding VCCI pins. • Software default junction temperature range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial.	2-2
	Updated Table 2-5 • Package Thermal Resistivities (SAR 60078).	2-6
	Added 2 mA drive strength information in the following tables (SAR 57182): • Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage • Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage • Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage • Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-28, 2-28, 2-28, 2-29
	Fixed typo for "VQ128" section in "Package Pin Assignments" section	4-1
Revision 16 (December 2012)	The "IGLOO PLUS Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43175).	III
	The note in Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42566).	2-61, 2-62
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 15 (October 2012)	Values updated for IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage in Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices and for IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage in Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices (SAR 31988). Also added a new Note to the two tables.	2-10, 2-11
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40277).	N/A
Revision 14 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2