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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 1584 |
| Total RAM Bits | 18432 |
| Number of I/O | 157 |
| Number of Gates | 60000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 201-VFBGA, CSBGA |
| Supplier Device Package | 201-CSP (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/aglp060v2-csg201i |

## SRAM and FIFO

IGLOO PLUS devices (except AGLP030 devices) have embedded SRAM blocks along their north side. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in AGLP030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

IGLOO PLUS devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO PLUS family contains six CCCs. One CCC (center west side) has a PLL. The AGLP030 device does not have a PLL or CCCs; it contains only inputs to six globals.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases (for PLL only) is 40 ps × 250 MHz / $f_{OUT\_CCC}$

## Global Clocking

IGLOO PLUS devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

## I/Os with Advanced I/O Standards

The IGLOO PLUS family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO PLUS FPGAs support many different I/O standards.

The I/Os are organized into four banks. All devices in IGLOO PLUS have four banks. The configuration of these banks determines the I/O standards supported.

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

$P_{STAT}$ = (PDC1 or PDC2 or PDC3) + $N_{BANKS}$ * PDC5

$N_{BANKS}$ is the number of I/O banks powered in the design.

#### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

#### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S-CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

#### Sequential Cells Contribution—$P_{S-CELL}$

$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S-CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

***Table 2-26* • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.31 | 0.19 | 0.99 | 1.37 | 0.67 | 2.34 | 1.86 | 2.65 | 3.38 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 5 pF | – | 0.98 | 3.21 | 0.19 | 1.32 | 1.92 | 0.67 | 3.21 | 2.52 | 3.73 | 4.73 | ns |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.29 | 0.19 | 1.19 | 1.40 | 0.67 | 2.32 | 1.94 | 2.65 | 3.27 | ns |
| 1.8 V LVCMOS | 8 mA | 8 mA | High | 5 pF | – | 0.98 | 2.45 | 0.19 | 1.12 | 1.61 | 0.67 | 2.48 | 2.16 | 2.71 | 3.16 | ns |
| 1.5 V LVCMOS | 4 mA | 4 mA | High | 5 pF | – | 0.98 | 2.71 | 0.19 | 1.26 | 1.80 | 0.67 | 2.75 | 2.39 | 2.78 | 3.15 | ns |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |
| 1.2 V LVCMOS Wide Range[3] | 100 µA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Single-Ended I/O Characteristics

### *3.3 V LVTTL / 3.3 V LVCMOS*

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

***Table 2-34* • Minimum and Maximum DC Input and Output Levels**

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min. V** | **Max. V** | **Min. V** | **Max. V** | **Max. V** | **Min. V** | **mA** | **mA** | **Max. mA[3]** | **Max. mA[3]** | **µA[4]** | **µA[4]** |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |
| 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 103 | 109 | 10 | 10 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 103 | 109 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

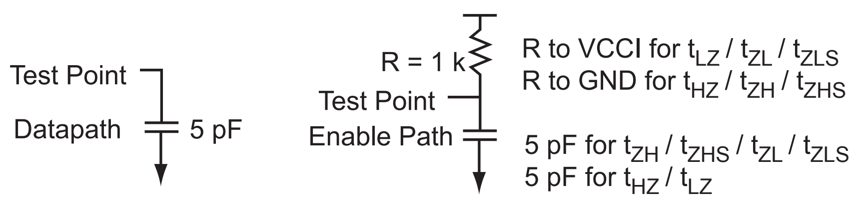



***Figure 2-7* • AC Loading**

***Table 2-35* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

*Note:* **Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

### Timing Characteristics

#### *Applies to 1.5 V DC Core Voltage*

***Table 2-36*** **• 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 4 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 6 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 8 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 12 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |
| 16 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-37*** **• 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 4 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 6 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 8 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 12 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |
| 16 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |

*Notes:*

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

#### *Applies to 1.2 V DC Core Voltage*

***Table 2-38*** **• 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 4 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 6 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 1.37 | 0.67 | 3.96 | 3.45 | 2.49 | 2.98 | ns |
| 8 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 137 | 0.67 | 3.86 | 3.45 | 2.49 | 2.98 | ns |
| 12 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |
| 16 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Characteristics

### *Applies to 1.5 V DC Core Voltage*

***Table 2-60*** **• 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 6.07 | 0.18 | 1.16 | 1.62 | 0.66 | 6.19 | 5.53 | 2.13 | 2.02 | ns |
| 4 mA | STD | 0.97 | 5.24 | 0.18 | 1.16 | 1.62 | 0.66 | 5.34 | 4.81 | 2.37 | 2.47 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-61*** **• 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.65 | 0.18 | 1.16 | 1.62 | 0.66 | 2.71 | 2.43 | 2.13 | 2.11 | ns |
| 4 mA | STD | 0.97 | 2.29 | 0.18 | 1.16 | 1.62 | 0.66 | 2.33 | 2.00 | 2.37 | 2.57 | ns |

*Notes:*

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

### *Applies to 1.2 V DC Core Voltage*

***Table 2-62*** **• 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 6.57 | 0.19 | 1.26 | 1.80 | 0.67 | 6.68 | 6.01 | 2.54 | 2.59 | ns |
| 4 mA | STD | 0.98 | 5.72 | 0.19 | 1.26 | 1.80 | 0.67 | 5.81 | 5.27 | 2.79 | 3.05 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-63*** **• 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 3.08 | 0.19 | 1.26 | 1.80 | 0.67 | 3.13 | 2.82 | 2.53 | 2.68 | ns |
| 4 mA | STD | 0.98 | 2.71 | 0.19 | 1.26 | 1.80 | 0.67 | 2.75 | 2.39 | 2.78 | 3.15 | ns |

*Notes:*

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

***Table 2-73* • Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

*Note: *See Figure 2-13 on page 2-43 for more information.*

## VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

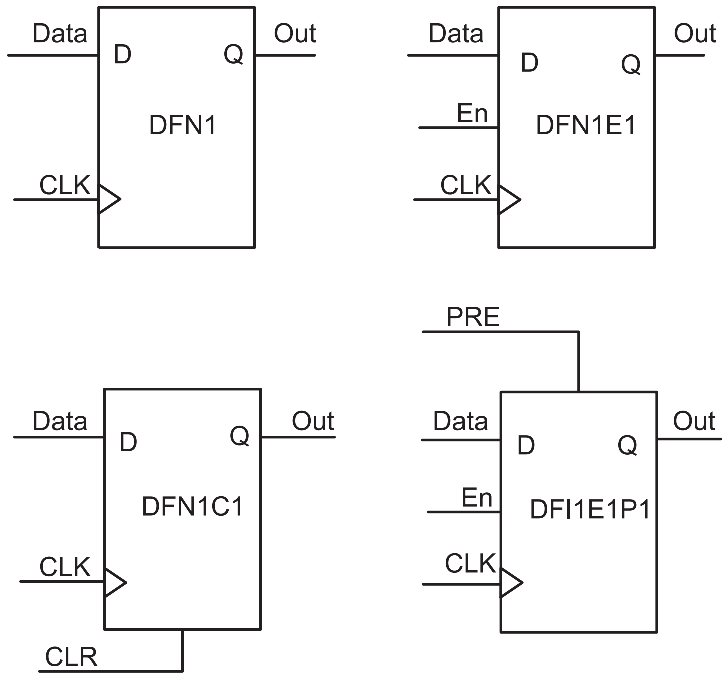



***Figure 2-19* • Sample of Sequential Cells**

### 1.2 V DC Core Voltage

***Table 2-83* • Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 1.61 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 1.17 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 1.29 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.95 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.95 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-88 • AGLP060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.02 | 2.43 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.09 | 2.65 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.56 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-89 • AGLP125 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.08 | 2.54 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.15 | 2.77 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## Timing Waveforms

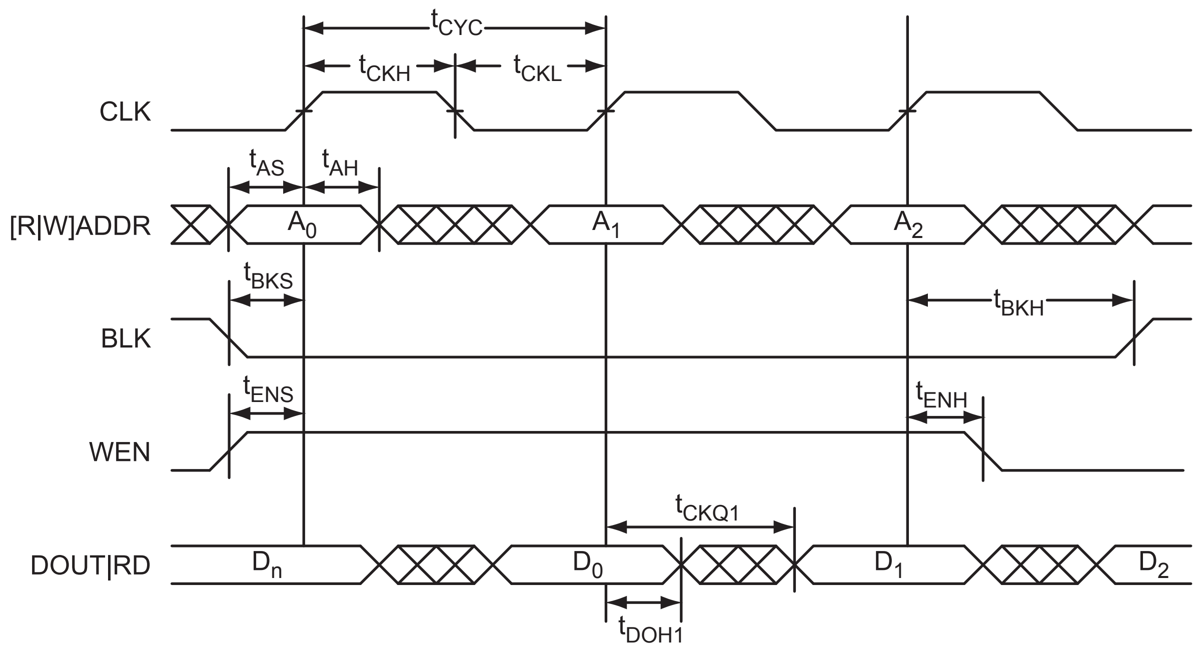



*Figure 2-24* • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

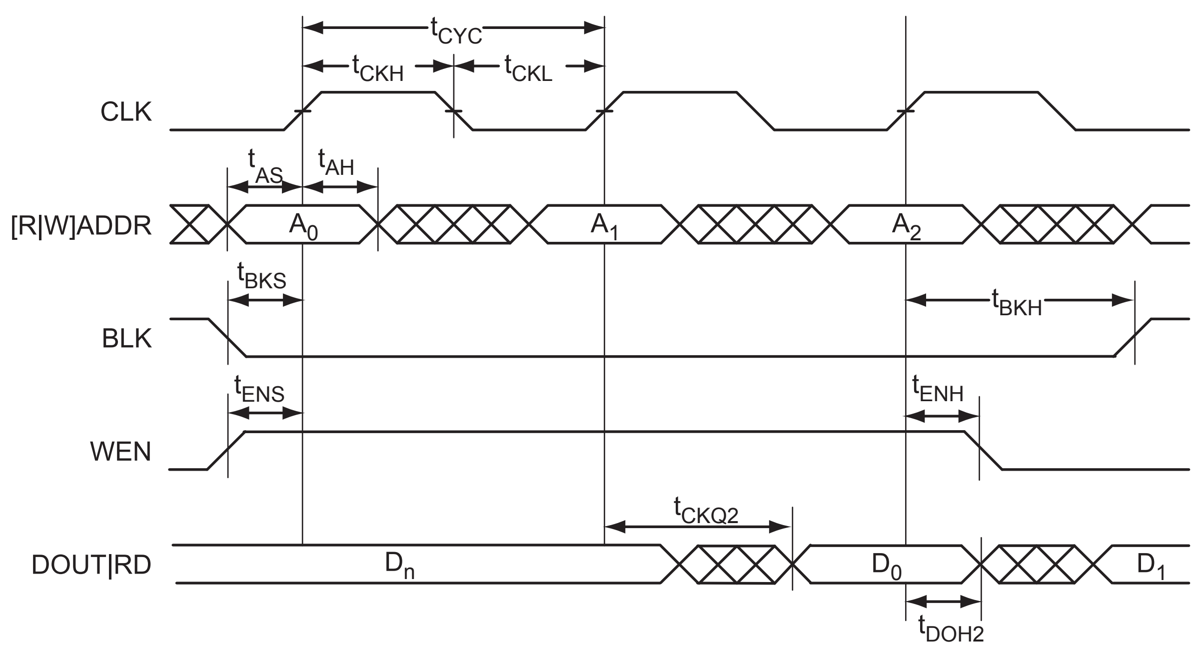



*Figure 2-25* • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

## *Timing Characteristics*

### 1.5 V DC Core Voltage

***Table 2-92*** **• RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.69 | ns |
| $t_{AH}$ | Address hold time | 0.13 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.68 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 1.37 | ns |
| $t_{BKH}$ | BLK hold time | 0.13 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.59 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.30 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.94 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.55 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 1.51 | ns |
| $t_{C2CWWL}$ [1] | Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge | 0.29 | ns |
| $t_{C2CRWH}$ [1] | Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge | 0.24 | ns |
| $t_{C2CWRH}$ [1] | Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge | 0.40 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 1.72 | ns |
| | RESET Low to data out Low on DOUT (pipelined) | 1.72 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.51 | ns |
| $t_{RECRSTB}$ | RESET recovery | 2.68 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-6 on page 2-6* *for derating values.*

## FIFO

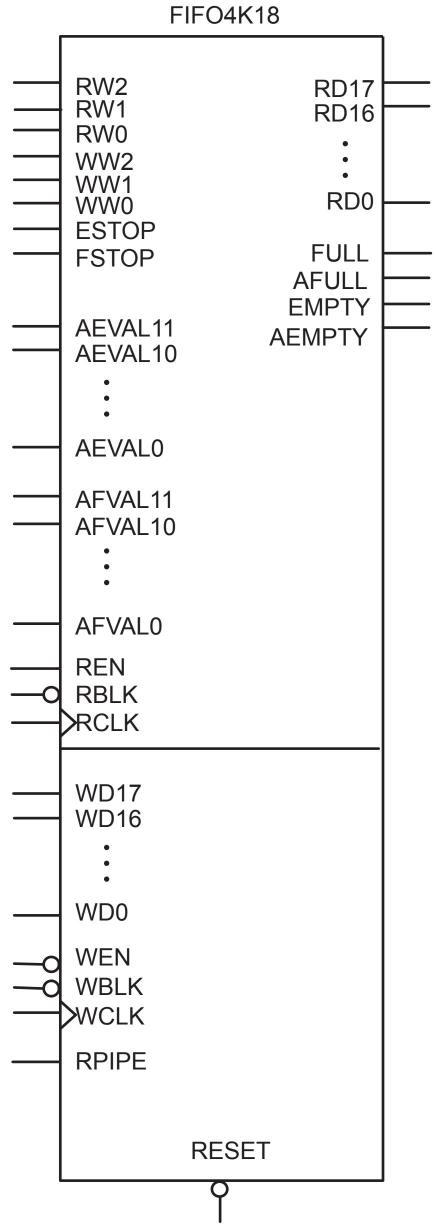



***Figure 2-29* • FIFO Model**

# JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

## *Timing Characteristics*

### 1.5 V DC Core Voltage

***Table 2-100* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.00 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 2.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.00 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 2.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 25.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 15 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-101* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.50 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 3.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.50 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 3.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 11.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 30.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**FF** **Flash*Freeze Mode Activation Pin**

The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

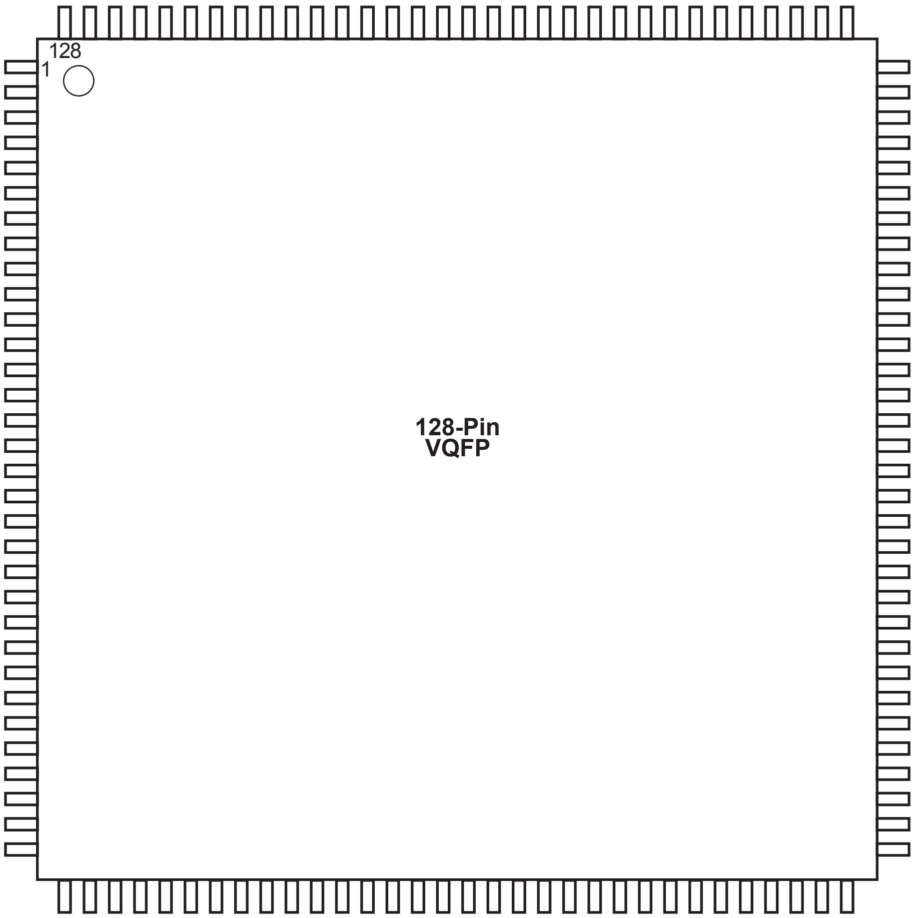
Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO and ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS Device Family User's Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1* • Flash*Freeze Pin Location in IGLOO PLUS Devices**

| Package | Flash*Freeze Pin |
|---|---|
| CS281 | W2 |
| CS201 | R4 |
| CS289 | U1 |
| VQ128 | 34 |
| VQ176 | 47 |

# 4 – Package Pin Assignments

## VQ128




*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

| CS281 | |
|---|---|
| **Pin Number** | **AGLP125 Function** |
| R15 | IO109RSB2 |
| R16 | GDA1/IO103RSB1 |
| R18 | GDB0/IO102RSB1 |
| R19 | GDC0/IO100RSB1 |
| T1 | IO171RSB3 |
| T2 | GEC0/IO169RSB3 |
| T4 | GEB0/IO167RSB3 |
| T5 | IO157RSB2 |
| T6 | IO158RSB2 |
| T7 | IO148RSB2 |
| T8 | IO145RSB2 |
| T9 | IO143RSB2 |
| T10 | GND |
| T11 | IO129RSB2 |
| T12 | IO126RSB2 |
| T13 | IO125RSB2 |
| T14 | IO116RSB2 |
| T15 | GDC2/IO107RSB2 |
| T16 | TMS |
| T18 | VJTAG |
| T19 | GDB1/IO101RSB1 |
| U1 | IO160RSB2 |
| U2 | GEA1/IO166RSB3 |
| U6 | IO151RSB2 |
| U14 | IO121RSB2 |
| U18 | TRST |
| U19 | GDA0/IO104RSB1 |
| V1 | IO159RSB2 |
| V2 | VCCIB3 |
| V3 | GEC2/IO162RSB2 |
| V4 | IO156RSB2 |
| V5 | IO153RSB2 |
| V6 | GND |
| V7 | IO144RSB2 |
| V8 | IO141RSB2 |
| V9 | IO140RSB2 |
| V10 | IO133RSB2 |
| V11 | IO127RSB2 |
| V12 | IO123RSB2 |
| V13 | IO120RSB2 |
| V14 | GND |
| V15 | IO113RSB2 |
| V16 | GDA2/IO105RSB2 |
| V17 | TDI |
| V18 | VCCIB2 |
| V19 | TDO |
| W1 | GND |
| W2 | FF/GEB2/IO163RSB2 |
| W3 | IO155RSB2 |
| W4 | IO152RSB2 |
| W5 | IO150RSB2 |
| W6 | IO147RSB2 |
| W7 | IO142RSB2 |
| W8 | IO139RSB2 |
| W9 | IO136RSB2 |
| W10 | VCCIB2 |
| W11 | IO128RSB2 |
| W12 | IO124RSB2 |
| W13 | IO119RSB2 |
| W14 | IO115RSB2 |
| W15 | IO114RSB2 |
| W16 | IO110RSB2 |
| W17 | GDB2/IO106RSB2 |
| W18 | TCK |
| W19 | GND |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| A1 | GAB1/IO03RSB0 |
| A2 | NC |
| A3 | NC |
| A4 | GND |
| A5 | IO10RSB0 |
| A6 | IO14RSB0 |
| A7 | IO16RSB0 |
| A8 | IO18RSB0 |
| A9 | GND |
| A10 | IO23RSB0 |
| A11 | IO27RSB0 |
| A12 | NC |
| A13 | NC |
| A14 | GND |
| A15 | NC |
| A16 | NC |
| A17 | GBC0/IO30RSB0 |
| B1 | GAA1/IO01RSB0 |
| B2 | GND |
| B3 | NC |
| B4 | NC |
| B5 | IO07RSB0 |
| B6 | NC |
| B7 | VCCIB0 |
| B8 | IO17RSB0 |
| B9 | IO19RSB0 |
| B10 | IO24RSB0 |
| B11 | IO28RSB0 |
| B12 | VCCIB0 |
| B13 | NC |
| B14 | NC |
| B15 | NC |
| B16 | GBC1/IO31RSB0 |
| B17 | GND |
| C1 | IO155RSB3 |
| C2 | GAA0/IO00RSB0 |
| C3 | GAC0/IO04RSB0 |
| C4 | NC |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| C5 | VCCIB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO21RSB0 |
| C10 | GND |
| C11 | IO29RSB0 |
| C12 | NC |
| C13 | NC |
| C14 | NC |
| C15 | GND |
| C16 | GBA0/IO34RSB0 |
| C17 | IO39RSB1 |
| D1 | IO150RSB3 |
| D2 | IO151RSB3 |
| D3 | GND |
| D4 | GAB0/IO02RSB0 |
| D5 | NC |
| D6 | NC |
| D7 | NC |
| D8 | GND |
| D9 | IO20RSB0 |
| D10 | IO25RSB0 |
| D11 | NC |
| D12 | NC |
| D13 | GND |
| D14 | GBB0/IO32RSB0 |
| D15 | GBA1/IO35RSB0 |
| D16 | IO37RSB1 |
| D17 | IO42RSB1 |
| E1 | VCCIB3 |
| E2 | IO147RSB3 |
| E3 | GAC2/IO152RSB3 |
| E4 | GAA2/IO156RSB3 |
| E5 | GAC1/IO05RSB0 |
| E6 | NC |
| E7 | IO06RSB0 |
| E8 | IO11RSB0 |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| E9 | IO22RSB0 |
| E10 | IO26RSB0 |
| E11 | VCCIB0 |
| E12 | NC |
| E13 | GBB1/IO33RSB0 |
| E14 | GBA2/IO36RSB1 |
| E15 | GBB2/IO38RSB1 |
| E16 | VCCIB1 |
| E17 | IO44RSB1 |
| F1 | GFC1/IO140RSB3 |
| F2 | IO142RSB3 |
| F3 | IO149RSB3 |
| F4 | VCCIB3 |
| F5 | GAB2/IO154RSB3 |
| F6 | IO153RSB3 |
| F7 | NC |
| F8 | IO08RSB0 |
| F9 | IO12RSB0 |
| F10 | NC |
| F11 | NC |
| F12 | NC |
| F13 | GBC2/IO40RSB1 |
| F14 | GND |
| F15 | IO43RSB1 |
| F16 | IO46RSB1 |
| F17 | IO45RSB1 |
| G1 | GFC0/IO139RSB3 |
| G2 | GND |
| G3 | IO144RSB3 |
| G4 | IO145RSB3 |
| G5 | IO146RSB3 |
| G6 | IO148RSB3 |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO48RSB1 |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| G13 | IO41RSB1 |
| G14 | IO47RSB1 |
| G15 | IO49RSB1 |
| G16 | IO50RSB1 |
| G17 | GND |
| H1 | VCOMPLF |
| H2 | GFB0/IO137RSB3 |
| H3 | NC |
| H4 | IO141RSB3 |
| H5 | IO143RSB3 |
| H6 | GFB1/IO138RSB3 |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | GND |
| H12 | GCC1/IO52RSB1 |
| H13 | IO51RSB1 |
| H14 | GCA0/IO57RSB1 |
| H15 | VCCIB1 |
| H16 | GCA2/IO58RSB1 |
| H17 | GCC0/IO53RSB1 |
| J1 | VCCPLF |
| J2 | GFA1/IO136RSB3 |
| J3 | VCCIB3 |
| J4 | IO131RSB3 |
| J5 | IO130RSB3 |
| J6 | IO129RSB3 |
| J7 | VCC |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO59RSB1 |
| J13 | GCB1/IO54RSB1 |
| J14 | IO62RSB1 |
| J15 | IO63RSB1 |
| J16 | GCB0/IO55RSB1 |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| J17 | GCA1/IO56RSB1 |
| K1 | GND |
| K2 | GFA0/IO135RSB3 |
| K3 | GFB2/IO133RSB3 |
| K4 | IO128RSB3 |
| K5 | IO123RSB3 |
| K6 | IO125RSB3 |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | IO64RSB1 |
| K13 | IO61RSB1 |
| K14 | IO66RSB1 |
| K15 | IO65RSB1 |
| K16 | GND |
| K17 | GCC2/IO60RSB1 |
| L1 | GFA2/IO134RSB3 |
| L2 | GFC2/IO132RSB3 |
| L3 | IO127RSB3 |
| L4 | GND |
| L5 | IO121RSB3 |
| L6 | GEC1/IO116RSB3 |
| L7 | GND |
| L8 | GND |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GDC1/IO72RSB1 |
| L13 | GDB1/IO74RSB1 |
| L14 | VCCIB1 |
| L15 | IO70RSB1 |
| L16 | IO68RSB1 |
| L17 | IO67RSB1 |
| M1 | IO126RSB3 |
| M2 | VCCIB3 |
| M3 | IO124RSB3 |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| M4 | IO122RSB3 |
| M5 | GEB0/IO113RSB3 |
| M6 | GEB1/IO114RSB3 |
| M7 | NC |
| M8 | NC |
| M9 | IO90RSB2 |
| M10 | NC |
| M11 | IO83RSB2 |
| M12 | NC |
| M13 | GDA1/IO76RSB1 |
| M14 | GDA0/IO77RSB1 |
| M15 | IO71RSB1 |
| M16 | IO69RSB1 |
| M17 | VCCIB1 |
| N1 | IO119RSB3 |
| N2 | IO120RSB3 |
| N3 | GEC0/IO115RSB3 |
| N4 | GEA0/IO111RSB3 |
| N5 | GND |
| N6 | NC |
| N7 | IO104RSB2 |
| N8 | IO98RSB2 |
| N9 | IO96RSB2 |
| N10 | VCCIB2 |
| N11 | NC |
| N12 | NC |
| N13 | GDB2/IO79RSB2 |
| N14 | NC |
| N15 | GND |
| N16 | GDB0/IO75RSB1 |
| N17 | GDC0/IO73RSB1 |
| P1 | IO118RSB3 |
| P2 | IO117RSB3 |
| P3 | GND |
| P4 | NC |
| P5 | NC |
| P6 | IO106RSB2 |
| P7 | IO99RSB2 |

| CS289 | |
|---|---|
| Pin Number | AGLP125 Function |
| P8 | GND |
| P9 | IO132RSB2 |
| P10 | IO125RSB2 |
| P11 | IO126RSB2 |
| P12 | IO112RSB2 |
| P13 | VCCIB2 |
| P14 | IO108RSB2 |
| P15 | GDA2/IO105RSB2 |
| P16 | GDC2/IO107RSB2 |
| P17 | VJTAG |
| R1 | GND |
| R2 | GEA2/IO164RSB2 |
| R3 | IO158RSB2 |
| R4 | IO155RSB2 |
| R5 | IO150RSB2 |
| R6 | VCCIB2 |
| R7 | IO145RSB2 |
| R8 | IO141RSB2 |
| R9 | IO134RSB2 |
| R10 | IO130RSB2 |
| R11 | GND |
| R12 | IO118RSB2 |
| R13 | IO116RSB2 |
| R14 | IO114RSB2 |
| R15 | IO110RSB2 |
| R16 | TMS |
| R17 | TRST |
| T1 | GEA1/IO166RSB3 |
| T2 | GEC2/IO162RSB2 |
| T3 | IO153RSB2 |
| T4 | GND |
| T5 | IO147RSB2 |
| T6 | IO143RSB2 |
| T7 | IO140RSB2 |
| T8 | IO139RSB2 |
| T9 | VCCIB2 |
| T10 | IO131RSB2 |
| T11 | IO127RSB2 |

| CS289 | |
|---|---|
| Pin Number | AGLP125 Function |
| T12 | IO124RSB2 |
| T13 | IO122RSB2 |
| T14 | GND |
| T15 | IO115RSB2 |
| T16 | TDI |
| T17 | TDO |
| U1 | FF/GEB2/IO163RSB2 |
| U2 | GND |
| U3 | IO151RSB2 |
| U4 | IO149RSB2 |
| U5 | IO146RSB2 |
| U6 | IO142RSB2 |
| U7 | GND |
| U8 | IO138RSB2 |
| U9 | IO136RSB2 |
| U10 | IO133RSB2 |
| U11 | IO129RSB2 |
| U12 | GND |
| U13 | IO123RSB2 |
| U14 | IO120RSB2 |
| U15 | IO117RSB2 |
| U16 | TCK |
| U17 | VPUMP |