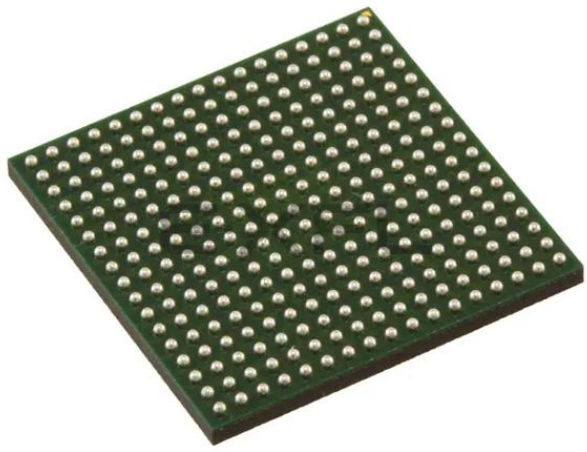

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

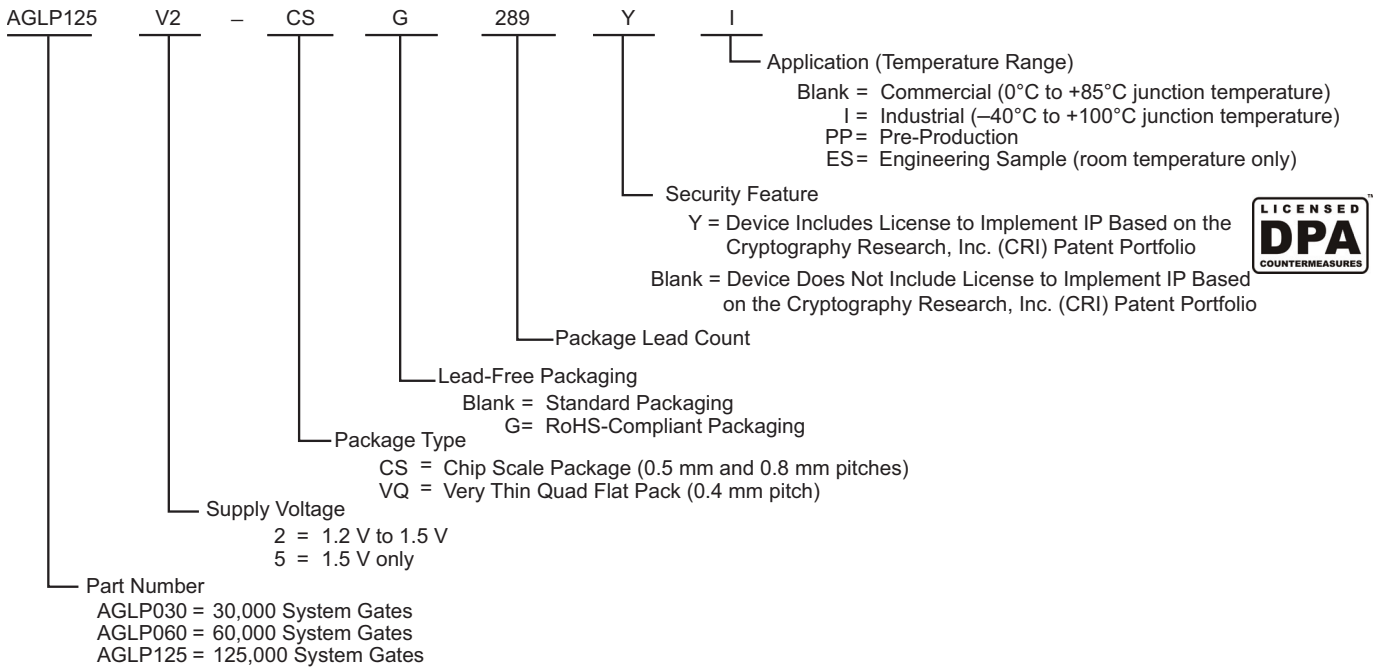
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

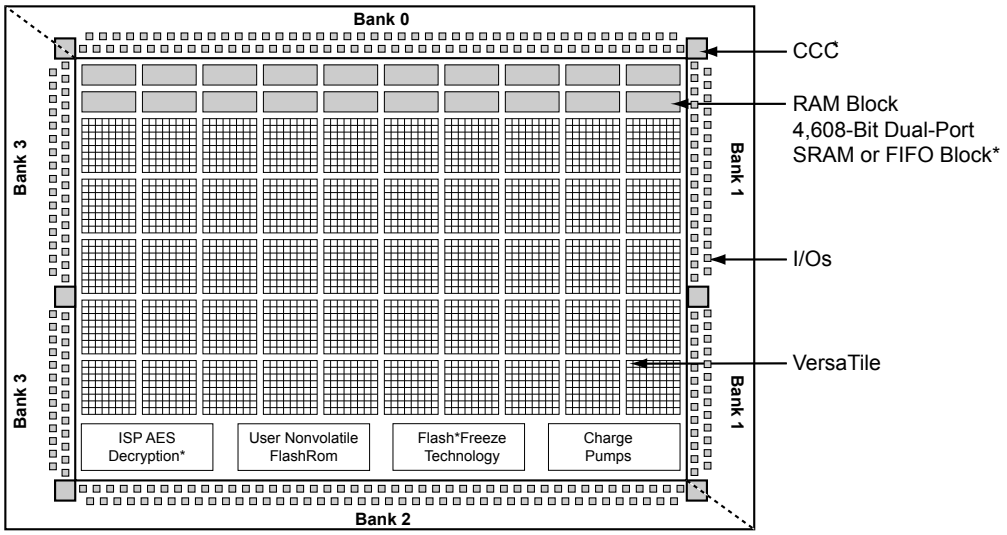
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	157
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v2-csg289i

IGLOO PLUS Ordering Information



1. *Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.*
2. *"G" indicates RoHS-compliant packages.*



*Note: *Not supported by AGLP030 devices*

Figure 1-1 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

*Flash*Freeze Technology*

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

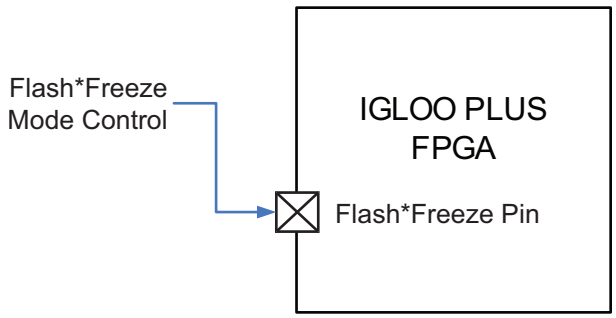


Figure 1-2 • **IGLOO PLUS Flash*Freeze Mode**

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature [1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes Low and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO PLUS Device Family User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

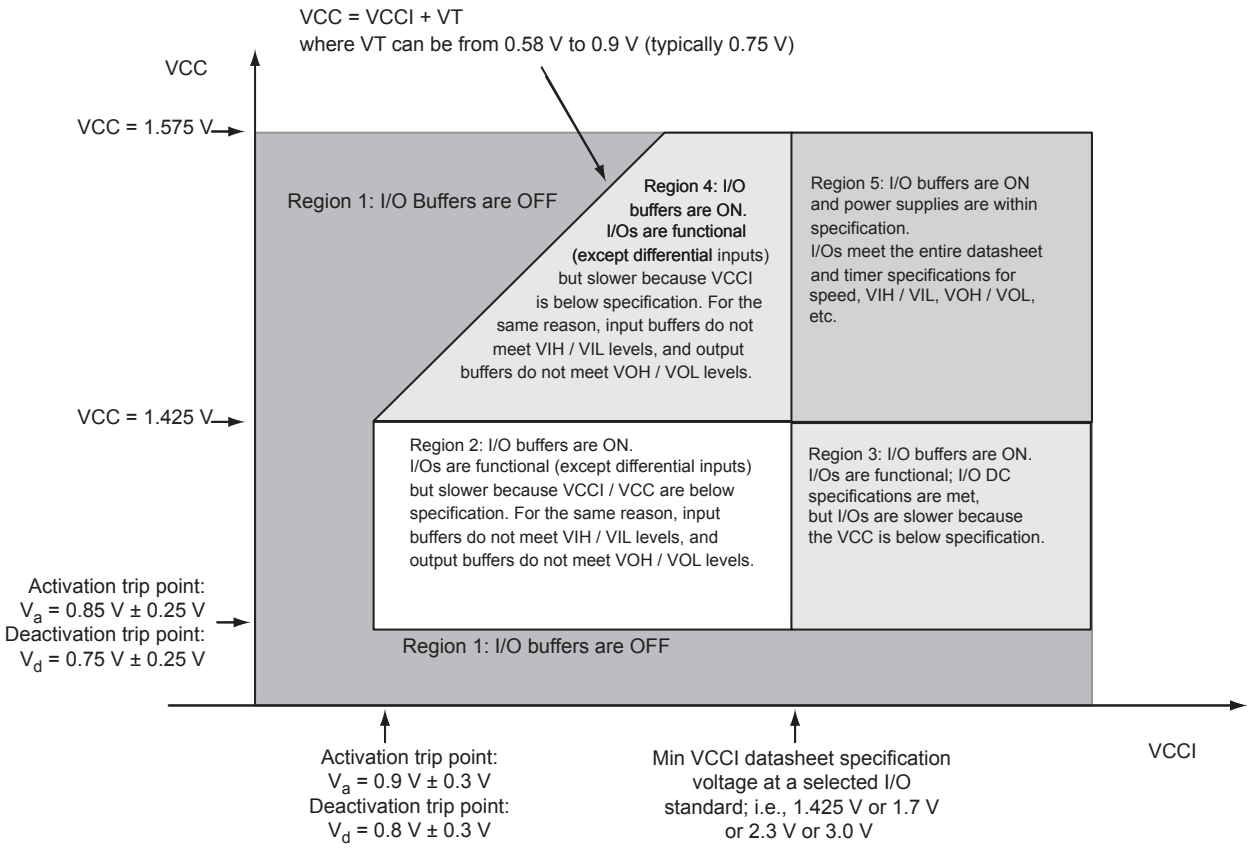


Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode***

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	µA
	1.5 V	6	10	18	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode***

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	µA

*Note: *IDD = N_{BANKS} * ICCI*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	µA

Power per I/O Pin

***Table 2-13* • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range[2]	3.3	16.26
3.3 V LVCMOS Wide Range[2] – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS[3]	1.2	0.55
1.2 V LVCMOS[3] – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range[3]	1.2	0.55
1.2 V LVCMOS Wide Range[3] – Schmitt Trigger	1.2	0.47

Notes:

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

***Table 2-14* • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range[3]	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS[4]	5	1.2	15.22
1.2 V LVCMOS Wide Range[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

User I/O Characteristics

Timing Model

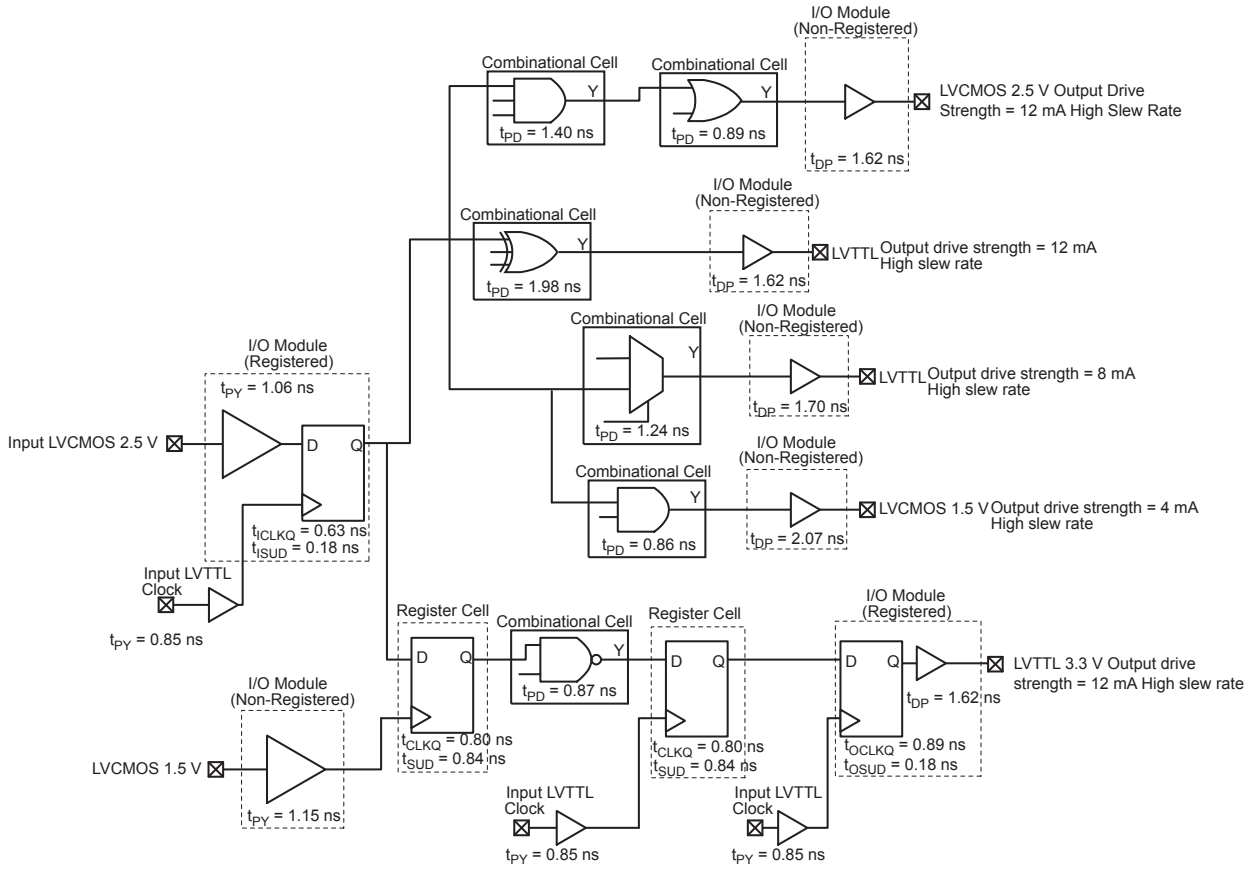


Figure 2-3 • **Timing Model**
Operating Conditions: STD Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Fully Registered I/O Buffers with Asynchronous Clear

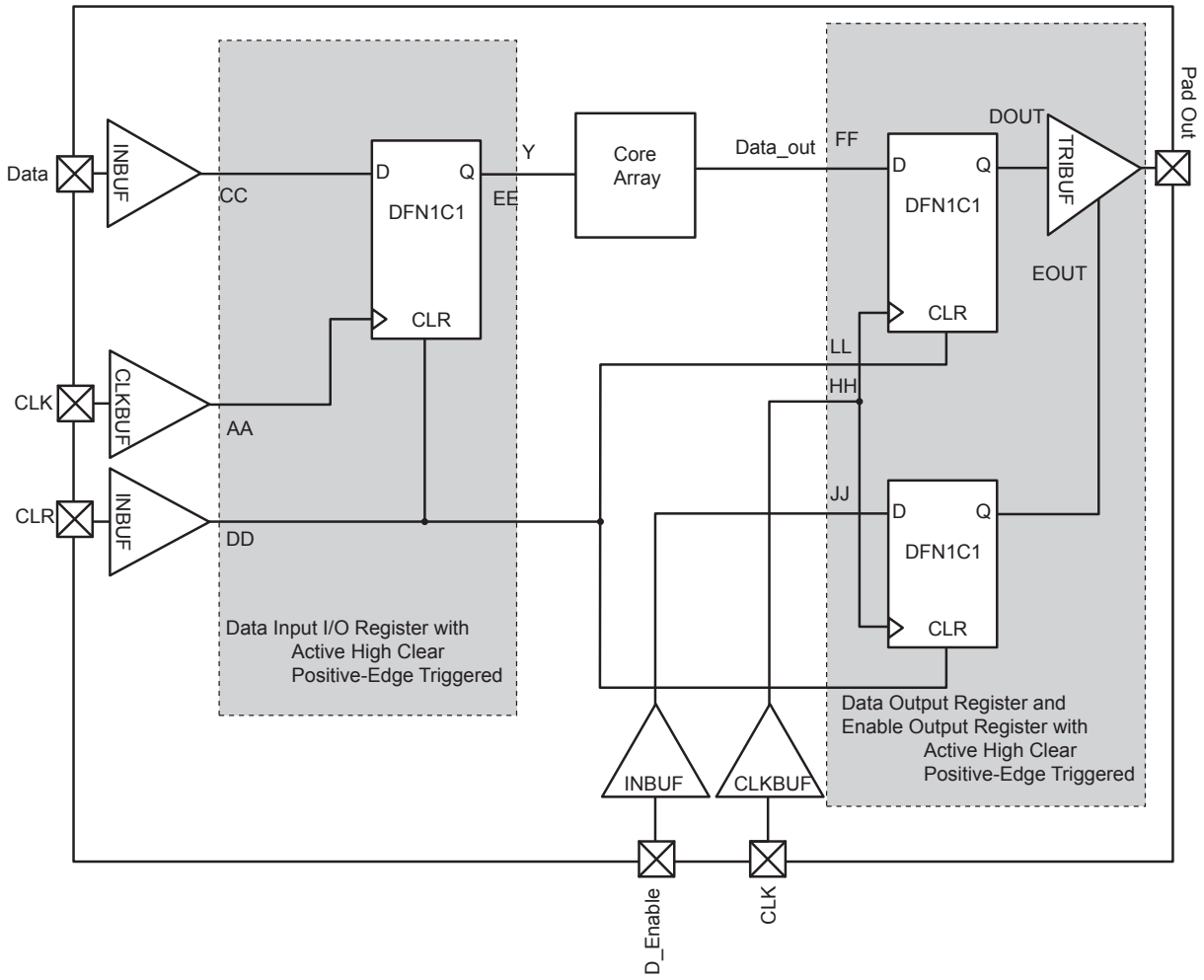


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

Output Register

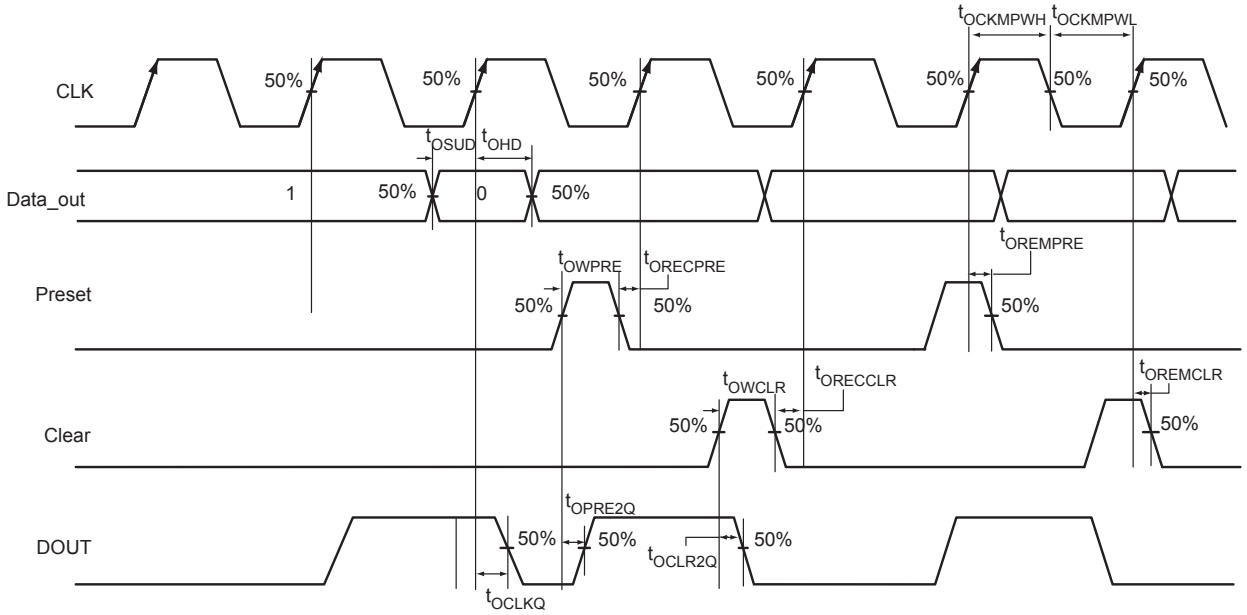


Figure 2-15 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-94* • RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.25	ns
t_{ENH}	REN, WEN hold time	0.25	ns
t_{BKS}	BLK setup time	2.54	ns
t_{BKH}	BLK hold time	0.25	ns
t_{DS}	Input data (DIN) setup time	1.10	ns
t_{DH}	Input data (DIN) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	5.51	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	2.82	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.32	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.21	ns
	RESET Low to data out Low on DOUT (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-100* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-101* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

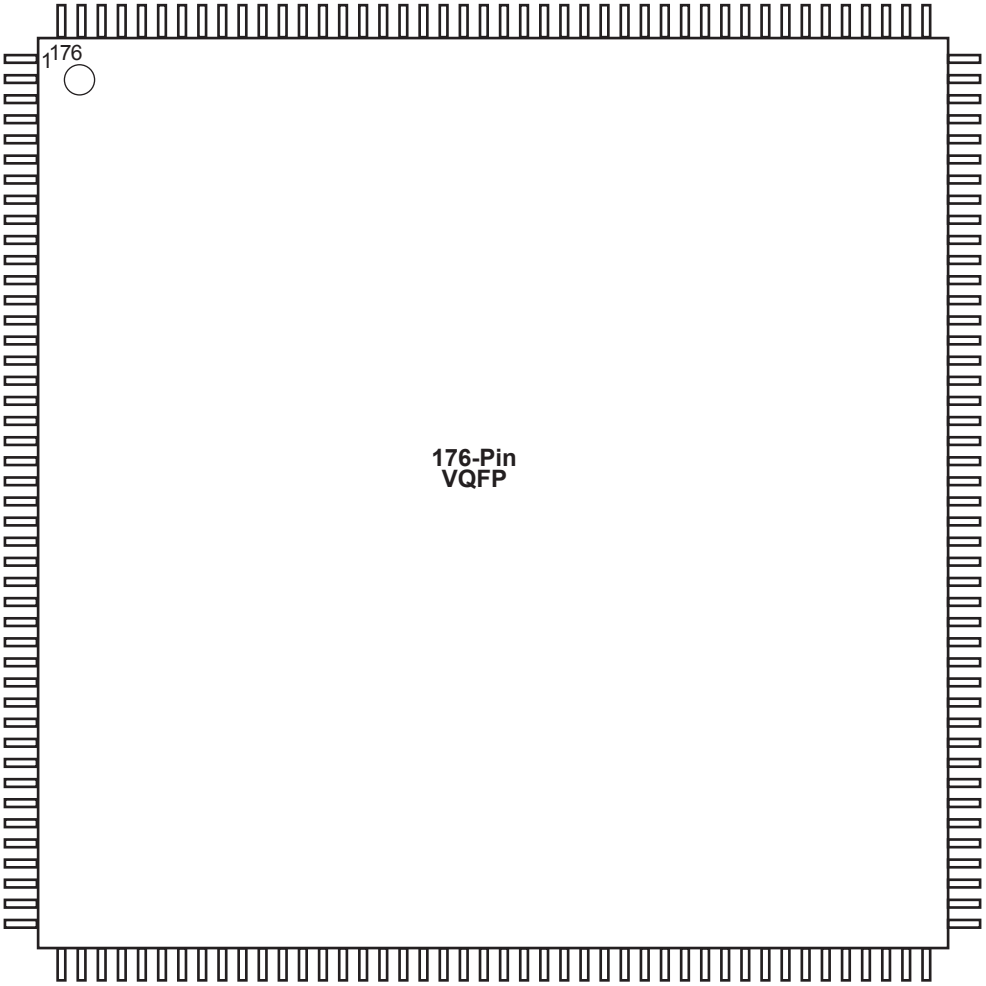
Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VQ128	
Pin Number	AGLP030 Function
1	IO119RSB3
2	IO118RSB3
3	IO117RSB3
4	IO115RSB3
5	IO116RSB3
6	IO113RSB3
7	IO114RSB3
8	GND
9	VCCIB3
10	IO112RSB3
11	IO111RSB3
12	IO110RSB3
13	IO109RSB3
14	GEC0/IO108RSB3
15	GEA0/IO107RSB3
16	GEB0/IO106RSB3
17	VCC
18	IO104RSB3
19	IO103RSB3
20	IO102RSB3
21	IO101RSB3
22	IO100RSB3
23	IO99RSB3
24	GND
25	VCCIB3
26	IO97RSB3
27	IO98RSB3
28	IO95RSB3
29	IO96RSB3
30	IO94RSB3
31	IO93RSB3
32	IO92RSB3
33	IO91RSB2
34	FF/IO90RSB2
35	IO89RSB2

VQ128	
Pin Number	AGLP030 Function
36	IO88RSB2
37	IO86RSB2
38	IO84RSB2
39	IO83RSB2
40	GND
41	VCCIB2
42	IO82RSB2
43	IO81RSB2
44	IO79RSB2
45	IO78RSB2
46	IO77RSB2
47	IO75RSB2
48	IO74RSB2
49	VCC
50	IO73RSB2
51	IO72RSB2
52	IO70RSB2
53	IO69RSB2
54	IO68RSB2
55	IO66RSB2
56	IO65RSB2
57	GND
58	VCCIB2
59	IO63RSB2
60	IO61RSB2
61	IO59RSB2
62	TCK
63	TDI
64	TMS
65	VPUMP
66	TDO
67	TRST
68	IO58RSB1
69	VJTAG
70	IO56RSB1

VQ128	
Pin Number	AGLP030 Function
71	IO57RSB1
72	VCCIB1
73	GND
74	IO55RSB1
75	IO54RSB1
76	IO53RSB1
77	IO52RSB1
78	IO51RSB1
79	IO50RSB1
80	IO49RSB1
81	VCC
82	GDB0/IO48RSB1
83	GDA0/IO47RSB1
84	GDC0/IO46RSB1
85	IO45RSB1
86	IO44RSB1
87	IO43RSB1
88	IO42RSB1
89	VCCIB1
90	GND
91	IO40RSB1
92	IO41RSB1
93	IO39RSB1
94	IO38RSB1
95	IO37RSB1
96	IO36RSB1
97	IO35RSB0
98	IO34RSB0
99	IO33RSB0
100	IO32RSB0
101	IO30RSB0
102	IO28RSB0
103	IO27RSB0
104	VCCIB0
105	GND

VQ176



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ176	
Pin Number	AGLP060 Function
1	GAA2/IO156RSB3
2	IO155RSB3
3	GAB2/IO154RSB3
4	IO153RSB3
5	GAC2/IO152RSB3
6	GND
7	VCCIB3
8	IO149RSB3
9	IO147RSB3
10	IO145RSB3
11	IO144RSB3
12	IO143RSB3
13	VCC
14	IO141RSB3
15	GFC1/IO140RSB3
16	GFB1/IO138RSB3
17	GFB0/IO137RSB3
18	VCOMPLF
19	GFA1/IO136RSB3
20	VCCPLF
21	GFA0/IO135RSB3
22	GND
23	VCCIB3
24	GFA2/IO134RSB3
25	GFB2/IO133RSB3
26	GFC2/IO132RSB3
27	IO131RSB3
28	IO130RSB3
29	IO129RSB3
30	IO127RSB3
31	IO126RSB3
32	IO125RSB3
33	IO123RSB3
34	IO122RSB3
35	IO121RSB3

VQ176	
Pin Number	AGLP060 Function
36	IO119RSB3
37	GND
38	VCCIB3
39	GEC1/IO116RSB3
40	GEB1/IO114RSB3
41	GEC0/IO115RSB3
42	GEB0/IO113RSB3
43	GEA1/IO112RSB3
44	GEA0/IO111RSB3
45	GEA2/IO110RSB2
46	NC
47	FF/GEB2/IO109RSB2
48	GEC2/IO108RSB2
49	IO106RSB2
50	IO107RSB2
51	IO104RSB2
52	IO105RSB2
53	IO102RSB2
54	IO103RSB2
55	GND
56	VCCIB2
57	IO101RSB2
58	IO100RSB2
59	IO99RSB2
60	IO98RSB2
61	IO97RSB2
62	IO96RSB2
63	IO95RSB2
64	IO94RSB2
65	IO93RSB2
66	VCC
67	IO92RSB2
68	IO91RSB2
69	IO90RSB2

VQ176	
Pin Number	AGLP060 Function
70	IO89RSB2
71	IO88RSB2
72	IO87RSB2
73	IO86RSB2
74	IO85RSB2
75	IO84RSB2
76	GND
77	VCCIB2
78	IO83RSB2
79	IO82RSB2
80	GDC2/IO80RSB2
81	IO81RSB2
82	GDA2/IO78RSB2
83	GDB2/IO79RSB2
84	NC
85	NC
86	TCK
87	TDI
88	TMS
89	VPUMP
90	TDO
91	TRST
92	VJTAG
93	GDA1/IO76RSB1
94	GDC0/IO73RSB1
95	GDB1/IO74RSB1
96	GDC1/IO72RSB1
97	VCCIB1
98	GND
99	IO70RSB1
100	IO69RSB1
101	IO67RSB1
102	IO66RSB1
103	IO65RSB1
104	IO63RSB1

VQ176	
Pin Number	AGLP060 Function
105	IO62RSB1
106	IO61RSB1
107	GCC2/IO60RSB1
108	GCB2/IO59RSB1
109	GCA2/IO58RSB1
110	GCA0/IO57RSB1
111	GCA1/IO56RSB1
112	VCCIB1
113	GND
114	GCB0/IO55RSB1
115	GCB1/IO54RSB1
116	GCC0/IO53RSB1
117	GCC1/IO52RSB1
118	IO51RSB1
119	IO50RSB1
120	VCC
121	IO48RSB1
122	IO47RSB1
123	IO45RSB1
124	IO44RSB1
125	IO43RSB1
126	VCCIB1
127	GND
128	GBC2/IO40RSB1
129	IO39RSB1
130	GBB2/IO38RSB1
131	IO37RSB1
132	GBA2/IO36RSB1
133	GBA1/IO35RSB0
134	NC
135	GBA0/IO34RSB0
136	NC
137	GBB1/IO33RSB0
138	NC
139	GBC1/IO31RSB0

VQ176	
Pin Number	AGLP060 Function
140	GBB0/IO32RSB0
141	GBC0/IO30RSB0
142	IO29RSB0
143	IO28RSB0
144	IO27RSB0
145	VCCIB0
146	GND
147	IO26RSB0
148	IO25RSB0
149	IO24RSB0
150	IO23RSB0
151	IO22RSB0
152	IO21RSB0
153	IO20RSB0
154	IO19RSB0
155	IO18RSB0
156	VCC
157	IO17RSB0
158	IO16RSB0
159	IO15RSB0
160	IO14RSB0
161	IO13RSB0
162	IO12RSB0
163	IO11RSB0
164	IO10RSB0
165	IO09RSB0
166	VCCIB0
167	GND
168	IO07RSB0
169	IO08RSB0
170	GAC1/IO05RSB0
171	IO06RSB0
172	GAB1/IO03RSB0
173	GAC0/IO04RSB0
174	GAB0/IO02RSB0

VQ176	
Pin Number	AGLP060 Function
175	GAA1/IO01RSB0
176	GAA0/IO00RSB0

CS289	
Pin Number	AGLP125 Function
A1	GAB1/IO03RSB0
A2	IO11RSB0
A3	IO08RSB0
A4	GND
A5	IO19RSB0
A6	IO24RSB0
A7	IO26RSB0
A8	IO30RSB0
A9	GND
A10	IO35RSB0
A11	IO38RSB0
A12	IO40RSB0
A13	IO42RSB0
A14	GND
A15	IO48RSB0
A16	IO54RSB0
A17	GBC0/IO57RSB0
B1	GAA1/IO01RSB0
B2	GND
B3	IO06RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO21RSB0
B7	VCCIB0
B8	IO28RSB0
B9	IO31RSB0
B10	IO37RSB0
B11	IO39RSB0
B12	VCCIB0
B13	IO44RSB0
B14	IO46RSB0
B15	IO49RSB0
B16	GBC1/IO58RSB0
B17	GND
C1	IO210RSB3
C2	GAA0/IO00RSB0
C3	GAC0/IO04RSB0
C4	IO09RSB0

CS289	
Pin Number	AGLP125 Function
C5	VCCIB0
C6	IO17RSB0
C7	IO23RSB0
C8	IO27RSB0
C9	IO33RSB0
C10	GND
C11	IO43RSB0
C12	IO45RSB0
C13	IO50RSB0
C14	IO52RSB0
C15	GND
C16	GBA0/IO61RSB0
C17	IO68RSB1
D1	IO204RSB3
D2	IO205RSB3
D3	GND
D4	GAB0/IO02RSB0
D5	IO07RSB0
D6	IO10RSB0
D7	IO18RSB0
D8	GND
D9	IO34RSB0
D10	IO41RSB0
D11	IO47RSB0
D12	IO55RSB0
D13	GND
D14	GBB0/IO59RSB0
D15	GBA1/IO62RSB0
D16	IO66RSB1
D17	IO70RSB1
E1	VCCIB3
E2	IO200RSB3
E3	GAC2/IO207RSB3
E4	GAA2/IO211RSB3
E5	GAC1/IO05RSB0
E6	IO12RSB0
E7	IO16RSB0
E8	IO22RSB0

CS289	
Pin Number	AGLP125 Function
E9	IO32RSB0
E10	IO36RSB0
E11	VCCIB0
E12	IO56RSB0
E13	GBB1/IO60RSB0
E14	GBA2/IO63RSB1
E15	GBB2/IO65RSB1
E16	VCCIB1
E17	IO73RSB1
F1	GFC1/IO194RSB3
F2	IO196RSB3
F3	IO202RSB3
F4	VCCIB3
F5	GAB2/IO209RSB3
F6	IO208RSB3
F7	IO14RSB0
F8	IO20RSB0
F9	IO25RSB0
F10	IO29RSB0
F11	IO51RSB0
F12	IO53RSB0
F13	GBC2/IO67RSB1
F14	GND
F15	IO75RSB1
F16	IO71RSB1
F17	IO77RSB1
G1	GFC0/IO193RSB3
G2	GND
G3	IO198RSB3
G4	IO203RSB3
G5	IO201RSB3
G6	IO206RSB3
G7	GND
G8	GND
G9	VCC
G10	GND
G11	GND
G12	IO72RSB1

CS289	
Pin Number	AGLP125 Function
G13	IO64RSB1
G14	IO69RSB1
G15	IO78RSB1
G16	IO76RSB1
G17	GND
H1	VCOMPLF
H2	GFB0/IO191RSB3
H3	IO195RSB3
H4	IO197RSB3
H5	IO199RSB3
H6	GFB1/IO192RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GCC1/IO79RSB1
H13	IO74RSB1
H14	GCA0/IO84RSB1
H15	VCCIB1
H16	GCA2/IO85RSB1
H17	GCC0/IO80RSB1
J1	VCCPLF
J2	GFA1/IO190RSB3
J3	VCCIB3
J4	IO185RSB3
J5	IO183RSB3
J6	IO181RSB3
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO86RSB1
J13	GCB1/IO81RSB1
J14	IO90RSB1
J15	IO89RSB1
J16	GCB0/IO82RSB1

CS289	
Pin Number	AGLP125 Function
J17	GCA1/IO83RSB1
K1	GND
K2	GFA0/IO189RSB3
K3	GFB2/IO187RSB3
K4	IO179RSB3
K5	IO175RSB3
K6	IO177RSB3
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO88RSB1
K13	IO94RSB1
K14	IO95RSB1
K15	IO93RSB1
K16	GND
K17	GCC2/IO87RSB1
L1	GFA2/IO188RSB3
L2	GFC2/IO186RSB3
L3	IO182RSB3
L4	GND
L5	IO173RSB3
L6	GEC1/IO170RSB3
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	GDC1/IO99RSB1
L13	GDB1/IO101RSB1
L14	VCCIB1
L15	IO98RSB1
L16	IO92RSB1
L17	IO91RSB1
M1	IO184RSB3
M2	VCCIB3
M3	IO176RSB3

CS289	
Pin Number	AGLP125 Function
M4	IO172RSB3
M5	GEB0/IO167RSB3
M6	GEB1/IO168RSB3
M7	IO159RSB2
M8	IO161RSB2
M9	IO135RSB2
M10	IO128RSB2
M11	IO121RSB2
M12	IO113RSB2
M13	GDA1/IO103RSB1
M14	GDA0/IO104RSB1
M15	IO97RSB1
M16	IO96RSB1
M17	VCCIB1
N1	IO180RSB3
N2	IO178RSB3
N3	GEC0/IO169RSB3
N4	GEA0/IO165RSB3
N5	GND
N6	IO156RSB2
N7	IO148RSB2
N8	IO144RSB2
N9	IO137RSB2
N10	VCCIB2
N11	IO119RSB2
N12	IO111RSB2
N13	GDB2/IO106RSB2
N14	IO109RSB2
N15	GND
N16	GDB0/IO102RSB1
N17	GDC0/IO100RSB1
P1	IO174RSB3
P2	IO171RSB3
P3	GND
P4	IO160RSB2
P5	IO157RSB2
P6	IO154RSB2
P7	IO152RSB2

CS289	
Pin Number	**AGLP125 Function**
P8	GND
P9	IO132RSB2
P10	IO125RSB2
P11	IO126RSB2
P12	IO112RSB2
P13	VCCIB2
P14	IO108RSB2
P15	GDA2/IO105RSB2
P16	GDC2/IO107RSB2
P17	VJTAG
R1	GND
R2	GEA2/IO164RSB2
R3	IO158RSB2
R4	IO155RSB2
R5	IO150RSB2
R6	VCCIB2
R7	IO145RSB2
R8	IO141RSB2
R9	IO134RSB2
R10	IO130RSB2
R11	GND
R12	IO118RSB2
R13	IO116RSB2
R14	IO114RSB2
R15	IO110RSB2
R16	TMS
R17	TRST
T1	GEA1/IO166RSB3
T2	GEC2/IO162RSB2
T3	IO153RSB2
T4	GND
T5	IO147RSB2
T6	IO143RSB2
T7	IO140RSB2
T8	IO139RSB2
T9	VCCIB2
T10	IO131RSB2
T11	IO127RSB2

CS289	
Pin Number	**AGLP125 Function**
T12	IO124RSB2
T13	IO122RSB2
T14	GND
T15	IO115RSB2
T16	TDI
T17	TDO
U1	FF/GEB2/IO163RSB2
U2	GND
U3	IO151RSB2
U4	IO149RSB2
U5	IO146RSB2
U6	IO142RSB2
U7	GND
U8	IO138RSB2
U9	IO136RSB2
U10	IO133RSB2
U11	IO129RSB2
U12	GND
U13	IO123RSB2
U14	IO120RSB2
U15	IO117RSB2
U16	TCK
U17	VPUMP

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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