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Understanding Embedded - FPGAs (Field Programmable Gate Array)

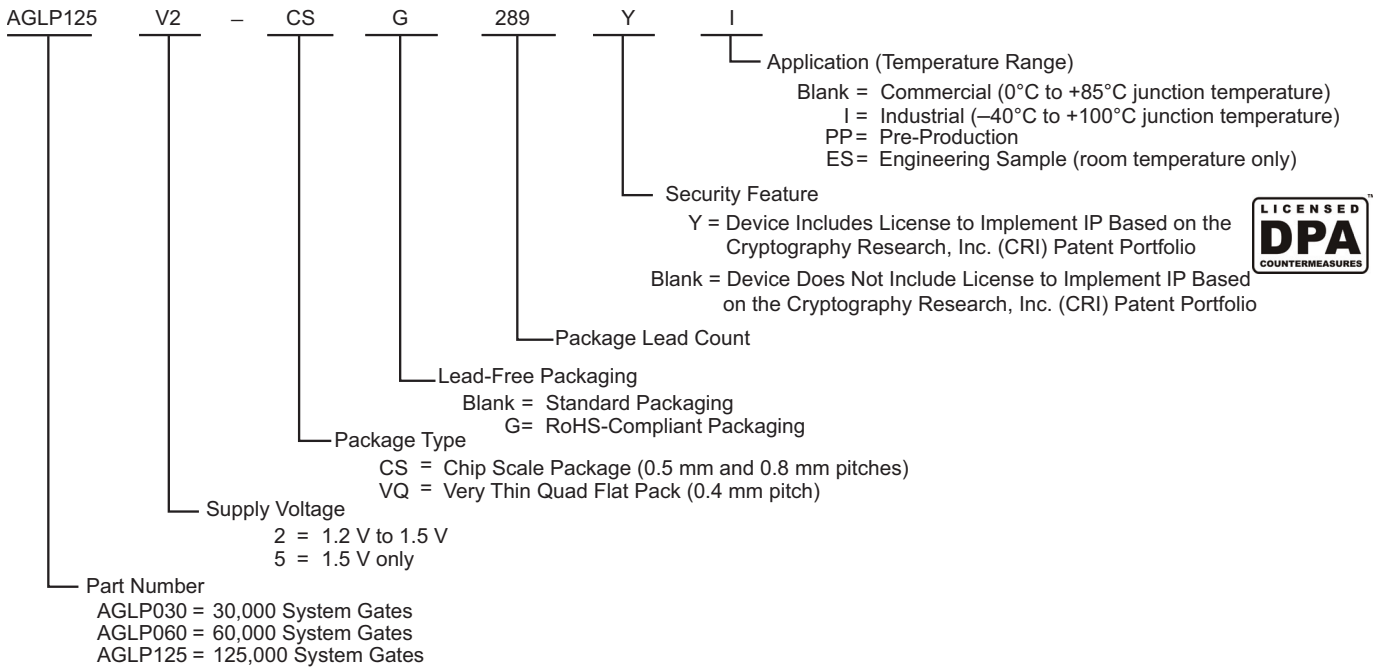
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	137
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	176-TQFP
Supplier Device Package	176-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v2-vq176

IGLOO PLUS Ordering Information



1. *Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.*
2. *"G" indicates RoHS-compliant packages.*

Temperature Grade Offerings

Package	AGLP030	AGLP060	AGLP125
CS201	C, I	C, I	–
CS281	–	–	C, I
CS289	C, I	C, I	C, I
VQ128	C, I	–	–
VQ176	–	C, I	–

Notes:
1. *C = Commercial temperature range: 0°C to 85°C junction temperature.*
2. *I = Industrial temperature range: –40°C to 100°C junction temperature.*

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/company/contact/default.aspx.

1 – IGLOO PLUS Device Family Overview

General Description

The IGLOO PLUS family of flash FPGAs, based on a 130 nm flash process, offers the lowest power FPGA, a single-chip solution, small-footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO PLUS devices enables entering and exiting an ultra-low power mode that consumes as little as 5 µW while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO PLUS device is completely functional in the system. This allows the IGLOO PLUS device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO PLUS devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOO PLUS is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO PLUS devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). IGLOO PLUS devices have up to 125 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 212 user I/Os. The AGLP030 devices have no PLL or RAM support.

Flash*Freeze Technology

The IGLOO PLUS device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO PLUS devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO PLUS V2 devices to support a wide range of core and I/O voltages (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, or set as HIGH or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high-pin-count packages, make IGLOO PLUS devices the best fit for portable electronics.

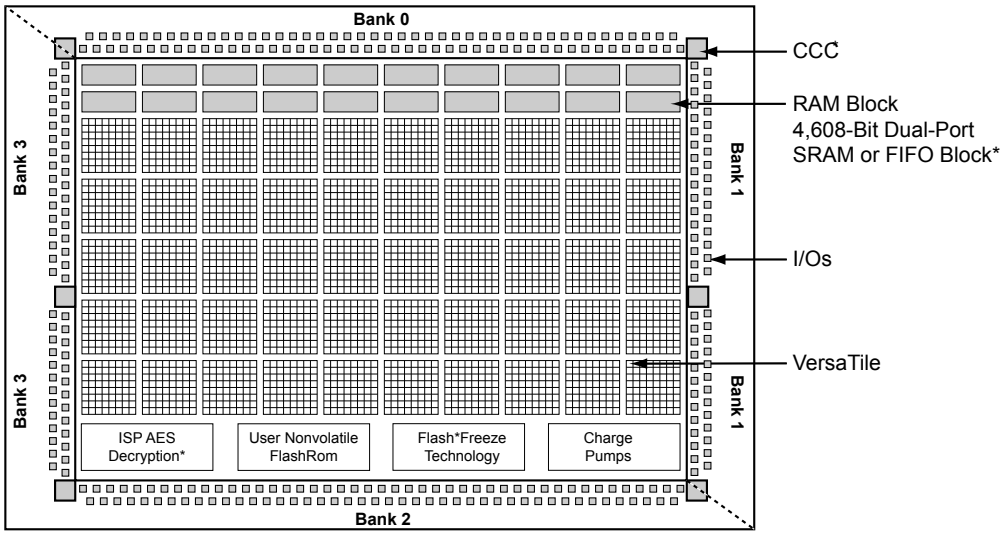
Flash Advantages

Low Power

IGLOO PLUS devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO PLUS devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO PLUS devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO PLUS device the lowest total system power offered by any FPGA.



*Note: *Not supported by AGLP030 devices*

Figure 1-1 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

*Flash*Freeze Technology*

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

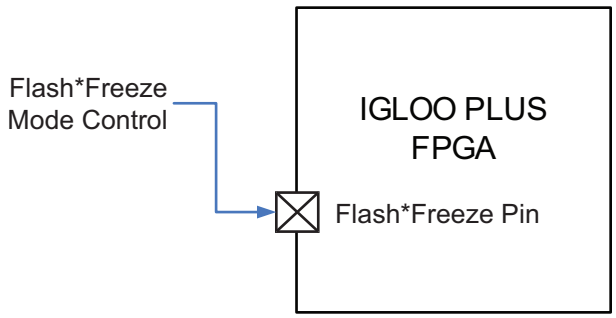


Figure 1-2 • **IGLOO PLUS Flash*Freeze Mode**

2 – IGLOO PLUS DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
V_I[1]	I/O input voltage	–0.3 V to 3.6 V	V
T_{STG}[2]	Storage temperature	–65 to +150	°C
T_J[2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

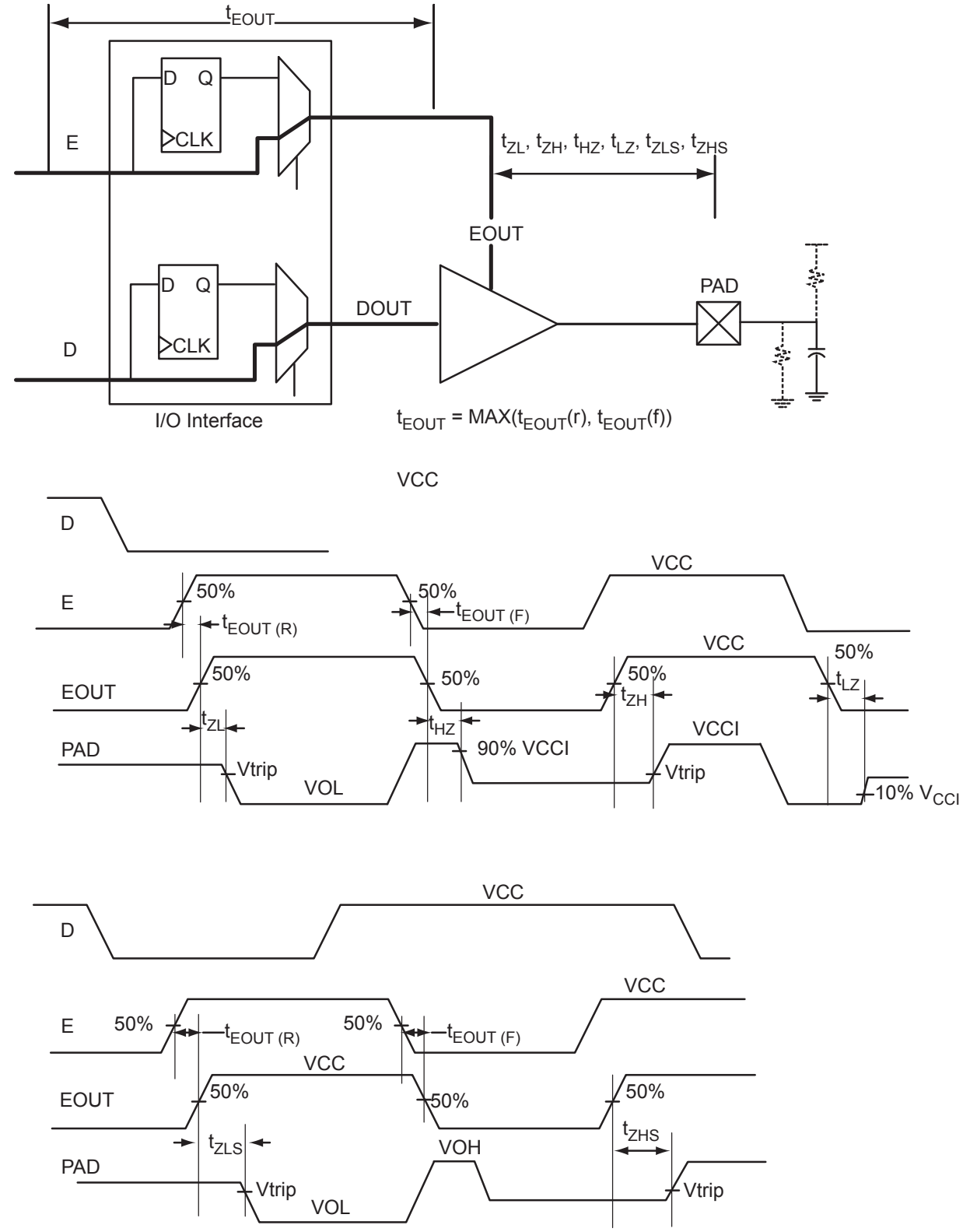


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-22 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
DC I/O Standards	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15
1.2 V LVCMOS Wide Range[5]	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Applicable to IGLOO PLUS V2 devices operating at VCCI ³ VCC.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V

Detailed I/O DC Characteristics

***Table 2-27* • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

***Table 2-28* • I/O Output Buffer Maximum Resistances [1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	157.5	163.8
1.2 V LVCMOS Wide Range[4]	100 µA	157.5	163.8

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC_I, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS model on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Applicable to IGLOO PLUS V2 devices operating at VCCI ≥ VCC.*

Input Register

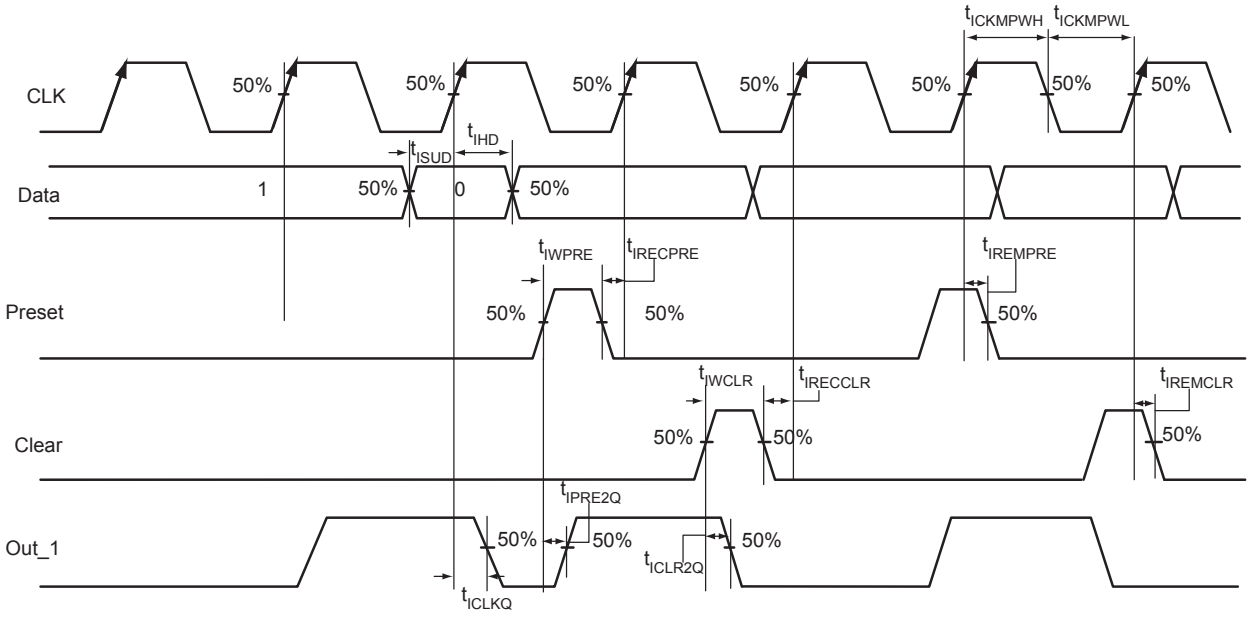


Figure 2-14 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.41	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Register

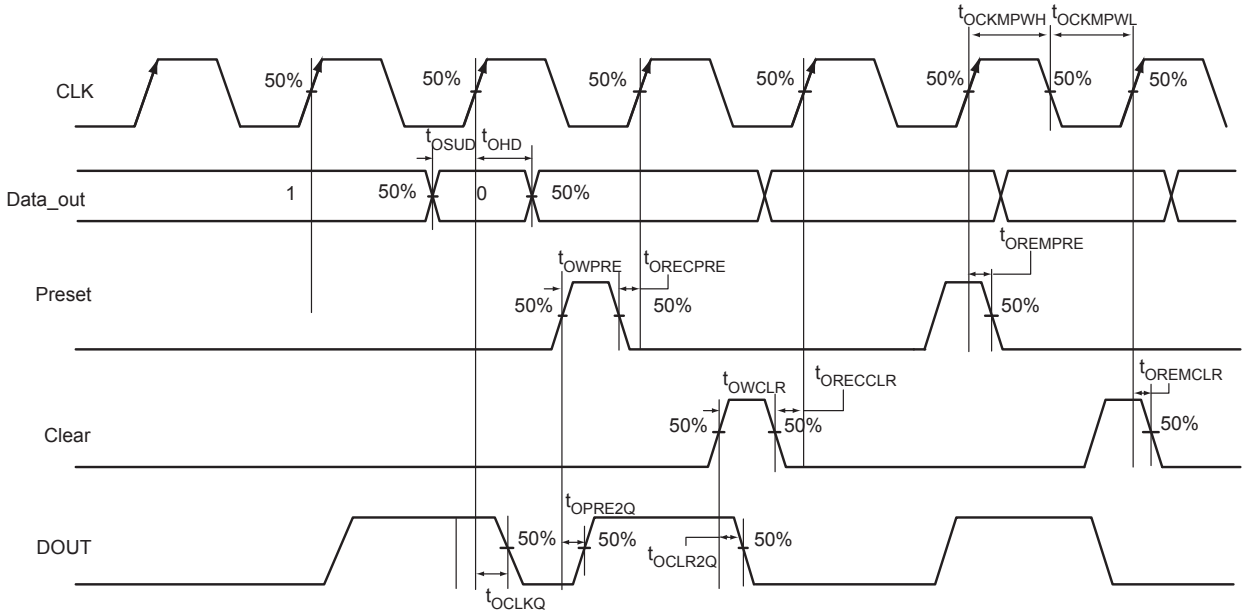


Figure 2-15 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-61. Table 2-84 to Table 2-89 on page 2-60 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-84* • AGLP030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-85* • AGLP060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.72	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-90 • IGLOO PLUS CCC/PLL Specification
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.20%
50 MHz to 250 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support a PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate, VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide.*

1.2 V DC Core Voltage

***Table 2-94* • RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.25	ns
t_{ENH}	REN, WEN hold time	0.25	ns
t_{BKS}	BLK setup time	2.54	ns
t_{BKH}	BLK hold time	0.25	ns
t_{DS}	Input data (DIN) setup time	1.10	ns
t_{DH}	Input data (DIN) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	5.51	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	2.82	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.32	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.21	ns
	RESET Low to data out Low on DOUT (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

***Table 2-97* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.30	ns
t_{DH}	Input Data (WD) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	3.41	ns
	RESET Low to Data Out Low on RD (pipelined)	3.41	ns
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VQ128	
Pin Number	AGLP030 Function
1	IO119RSB3
2	IO118RSB3
3	IO117RSB3
4	IO115RSB3
5	IO116RSB3
6	IO113RSB3
7	IO114RSB3
8	GND
9	VCCIB3
10	IO112RSB3
11	IO111RSB3
12	IO110RSB3
13	IO109RSB3
14	GEC0/IO108RSB3
15	GEA0/IO107RSB3
16	GEB0/IO106RSB3
17	VCC
18	IO104RSB3
19	IO103RSB3
20	IO102RSB3
21	IO101RSB3
22	IO100RSB3
23	IO99RSB3
24	GND
25	VCCIB3
26	IO97RSB3
27	IO98RSB3
28	IO95RSB3
29	IO96RSB3
30	IO94RSB3
31	IO93RSB3
32	IO92RSB3
33	IO91RSB2
34	FF/IO90RSB2
35	IO89RSB2

VQ128	
Pin Number	AGLP030 Function
36	IO88RSB2
37	IO86RSB2
38	IO84RSB2
39	IO83RSB2
40	GND
41	VCCIB2
42	IO82RSB2
43	IO81RSB2
44	IO79RSB2
45	IO78RSB2
46	IO77RSB2
47	IO75RSB2
48	IO74RSB2
49	VCC
50	IO73RSB2
51	IO72RSB2
52	IO70RSB2
53	IO69RSB2
54	IO68RSB2
55	IO66RSB2
56	IO65RSB2
57	GND
58	VCCIB2
59	IO63RSB2
60	IO61RSB2
61	IO59RSB2
62	TCK
63	TDI
64	TMS
65	VPUMP
66	TDO
67	TRST
68	IO58RSB1
69	VJTAG
70	IO56RSB1

VQ128	
Pin Number	AGLP030 Function
71	IO57RSB1
72	VCCIB1
73	GND
74	IO55RSB1
75	IO54RSB1
76	IO53RSB1
77	IO52RSB1
78	IO51RSB1
79	IO50RSB1
80	IO49RSB1
81	VCC
82	GDB0/IO48RSB1
83	GDA0/IO47RSB1
84	GDC0/IO46RSB1
85	IO45RSB1
86	IO44RSB1
87	IO43RSB1
88	IO42RSB1
89	VCCIB1
90	GND
91	IO40RSB1
92	IO41RSB1
93	IO39RSB1
94	IO38RSB1
95	IO37RSB1
96	IO36RSB1
97	IO35RSB0
98	IO34RSB0
99	IO33RSB0
100	IO32RSB0
101	IO30RSB0
102	IO28RSB0
103	IO27RSB0
104	VCCIB0
105	GND

CS201	
Pin Number	AGLP030 Function
H14	IO45RSB1
H15	IO43RSB1
J1	GEA0/IO107RSB3
J2	IO105RSB3
J3	IO104RSB3
J4	IO102RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	NC
J13	NC
J14	IO52RSB1
J15	IO50RSB1
K1	IO103RSB3
K2	IO101RSB3
K3	IO99RSB3
K4	IO100RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	NC
K13	IO57RSB1
K14	IO49RSB1
K15	IO53RSB1
L1	IO96RSB3
L2	IO98RSB3
L3	IO95RSB3
L4	IO94RSB3
L12	NC
L13	NC
L14	IO51RSB1

CS201	
Pin Number	AGLP030 Function
L15	IO58RSB1
M1	IO93RSB3
M2	IO92RSB3
M3	IO97RSB3
M4	GND
M5	NC
M6	IO79RSB2
M7	IO77RSB2
M8	IO72RSB2
M9	IO70RSB2
M10	IO61RSB2
M11	IO59RSB2
M12	GND
M13	NC
M14	IO55RSB1
M15	IO56RSB1
N1	NC
N2	NC
N3	GND
N4	NC
N5	IO88RSB2
N6	IO81RSB2
N7	IO75RSB2
N8	IO68RSB2
N9	IO66RSB2
N10	IO65RSB2
N11	IO71RSB2
N12	IO63RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	NC
P2	NC
P3	NC
P4	NC

CS201	
Pin Number	AGLP030 Function
P5	IO87RSB2
P6	IO86RSB2
P7	IO84RSB2
P8	IO80RSB2
P9	IO74RSB2
P10	IO73RSB2
P11	IO76RSB2
P12	IO67RSB2
P13	IO64RSB2
P14	VPUMP
P15	TRST
R1	NC
R2	NC
R3	IO91RSB2
R4	FF/IO90RSB2
R5	IO89RSB2
R6	IO83RSB2
R7	IO82RSB2
R8	IO85RSB2
R9	IO78RSB2
R10	IO69RSB2
R11	IO62RSB2
R12	IO60RSB2
R13	TMS
R14	TDI
R15	TCK

CS289	
Pin Number	AGLP125 Function
A1	GAB1/IO03RSB0
A2	IO11RSB0
A3	IO08RSB0
A4	GND
A5	IO19RSB0
A6	IO24RSB0
A7	IO26RSB0
A8	IO30RSB0
A9	GND
A10	IO35RSB0
A11	IO38RSB0
A12	IO40RSB0
A13	IO42RSB0
A14	GND
A15	IO48RSB0
A16	IO54RSB0
A17	GBC0/IO57RSB0
B1	GAA1/IO01RSB0
B2	GND
B3	IO06RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO21RSB0
B7	VCCIB0
B8	IO28RSB0
B9	IO31RSB0
B10	IO37RSB0
B11	IO39RSB0
B12	VCCIB0
B13	IO44RSB0
B14	IO46RSB0
B15	IO49RSB0
B16	GBC1/IO58RSB0
B17	GND
C1	IO210RSB3
C2	GAA0/IO00RSB0
C3	GAC0/IO04RSB0
C4	IO09RSB0

CS289	
Pin Number	AGLP125 Function
C5	VCCIB0
C6	IO17RSB0
C7	IO23RSB0
C8	IO27RSB0
C9	IO33RSB0
C10	GND
C11	IO43RSB0
C12	IO45RSB0
C13	IO50RSB0
C14	IO52RSB0
C15	GND
C16	GBA0/IO61RSB0
C17	IO68RSB1
D1	IO204RSB3
D2	IO205RSB3
D3	GND
D4	GAB0/IO02RSB0
D5	IO07RSB0
D6	IO10RSB0
D7	IO18RSB0
D8	GND
D9	IO34RSB0
D10	IO41RSB0
D11	IO47RSB0
D12	IO55RSB0
D13	GND
D14	GBB0/IO59RSB0
D15	GBA1/IO62RSB0
D16	IO66RSB1
D17	IO70RSB1
E1	VCCIB3
E2	IO200RSB3
E3	GAC2/IO207RSB3
E4	GAA2/IO211RSB3
E5	GAC1/IO05RSB0
E6	IO12RSB0
E7	IO16RSB0
E8	IO22RSB0

CS289	
Pin Number	AGLP125 Function
E9	IO32RSB0
E10	IO36RSB0
E11	VCCIB0
E12	IO56RSB0
E13	GBB1/IO60RSB0
E14	GBA2/IO63RSB1
E15	GBB2/IO65RSB1
E16	VCCIB1
E17	IO73RSB1
F1	GFC1/IO194RSB3
F2	IO196RSB3
F3	IO202RSB3
F4	VCCIB3
F5	GAB2/IO209RSB3
F6	IO208RSB3
F7	IO14RSB0
F8	IO20RSB0
F9	IO25RSB0
F10	IO29RSB0
F11	IO51RSB0
F12	IO53RSB0
F13	GBC2/IO67RSB1
F14	GND
F15	IO75RSB1
F16	IO71RSB1
F17	IO77RSB1
G1	GFC0/IO193RSB3
G2	GND
G3	IO198RSB3
G4	IO203RSB3
G5	IO201RSB3
G6	IO206RSB3
G7	GND
G8	GND
G9	VCC
G10	GND
G11	GND
G12	IO72RSB1

CS289	
Pin Number	AGLP125 Function
G13	IO64RSB1
G14	IO69RSB1
G15	IO78RSB1
G16	IO76RSB1
G17	GND
H1	VCOMPLF
H2	GFB0/IO191RSB3
H3	IO195RSB3
H4	IO197RSB3
H5	IO199RSB3
H6	GFB1/IO192RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GCC1/IO79RSB1
H13	IO74RSB1
H14	GCA0/IO84RSB1
H15	VCCIB1
H16	GCA2/IO85RSB1
H17	GCC0/IO80RSB1
J1	VCCPLF
J2	GFA1/IO190RSB3
J3	VCCIB3
J4	IO185RSB3
J5	IO183RSB3
J6	IO181RSB3
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO86RSB1
J13	GCB1/IO81RSB1
J14	IO90RSB1
J15	IO89RSB1
J16	GCB0/IO82RSB1

CS289	
Pin Number	AGLP125 Function
J17	GCA1/IO83RSB1
K1	GND
K2	GFA0/IO189RSB3
K3	GFB2/IO187RSB3
K4	IO179RSB3
K5	IO175RSB3
K6	IO177RSB3
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO88RSB1
K13	IO94RSB1
K14	IO95RSB1
K15	IO93RSB1
K16	GND
K17	GCC2/IO87RSB1
L1	GFA2/IO188RSB3
L2	GFC2/IO186RSB3
L3	IO182RSB3
L4	GND
L5	IO173RSB3
L6	GEC1/IO170RSB3
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	GDC1/IO99RSB1
L13	GDB1/IO101RSB1
L14	VCCIB1
L15	IO98RSB1
L16	IO92RSB1
L17	IO91RSB1
M1	IO184RSB3
M2	VCCIB3
M3	IO176RSB3

CS289	
Pin Number	AGLP125 Function
M4	IO172RSB3
M5	GEB0/IO167RSB3
M6	GEB1/IO168RSB3
M7	IO159RSB2
M8	IO161RSB2
M9	IO135RSB2
M10	IO128RSB2
M11	IO121RSB2
M12	IO113RSB2
M13	GDA1/IO103RSB1
M14	GDA0/IO104RSB1
M15	IO97RSB1
M16	IO96RSB1
M17	VCCIB1
N1	IO180RSB3
N2	IO178RSB3
N3	GEC0/IO169RSB3
N4	GEA0/IO165RSB3
N5	GND
N6	IO156RSB2
N7	IO148RSB2
N8	IO144RSB2
N9	IO137RSB2
N10	VCCIB2
N11	IO119RSB2
N12	IO111RSB2
N13	GDB2/IO106RSB2
N14	IO109RSB2
N15	GND
N16	GDB0/IO102RSB1
N17	GDC0/IO100RSB1
P1	IO174RSB3
P2	IO171RSB3
P3	GND
P4	IO160RSB2
P5	IO157RSB2
P6	IO154RSB2
P7	IO152RSB2

Revision	Changes	Page
Revision 13 (June 2012)	Figure 2-30 • FIFO Read and Figure 2-31 • FIFO Write have been added (SAR 34843).	2-73
	Updated the terminology used in Timing Characteristics in the following tables: Table 2-96 • FIFO and Table 2-97 • FIFO (SAR 38236).	2-76
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38320). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1
Revision 12 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34664).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOO PLUS Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34724).	III
	The "Specifying I/O States During Programming" section is new (SAR 34695).	1-7
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface" (SAR 34684).	1-3

Revision	Changes	Page
Revision 11 (continued)	The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying IIL and IIH were added. Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366). Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).	2-32
	The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.	2-45 through 2-56
	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM", "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-78