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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	137
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	176-TQFP
Supplier Device Package	176-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v2-vqg176

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated

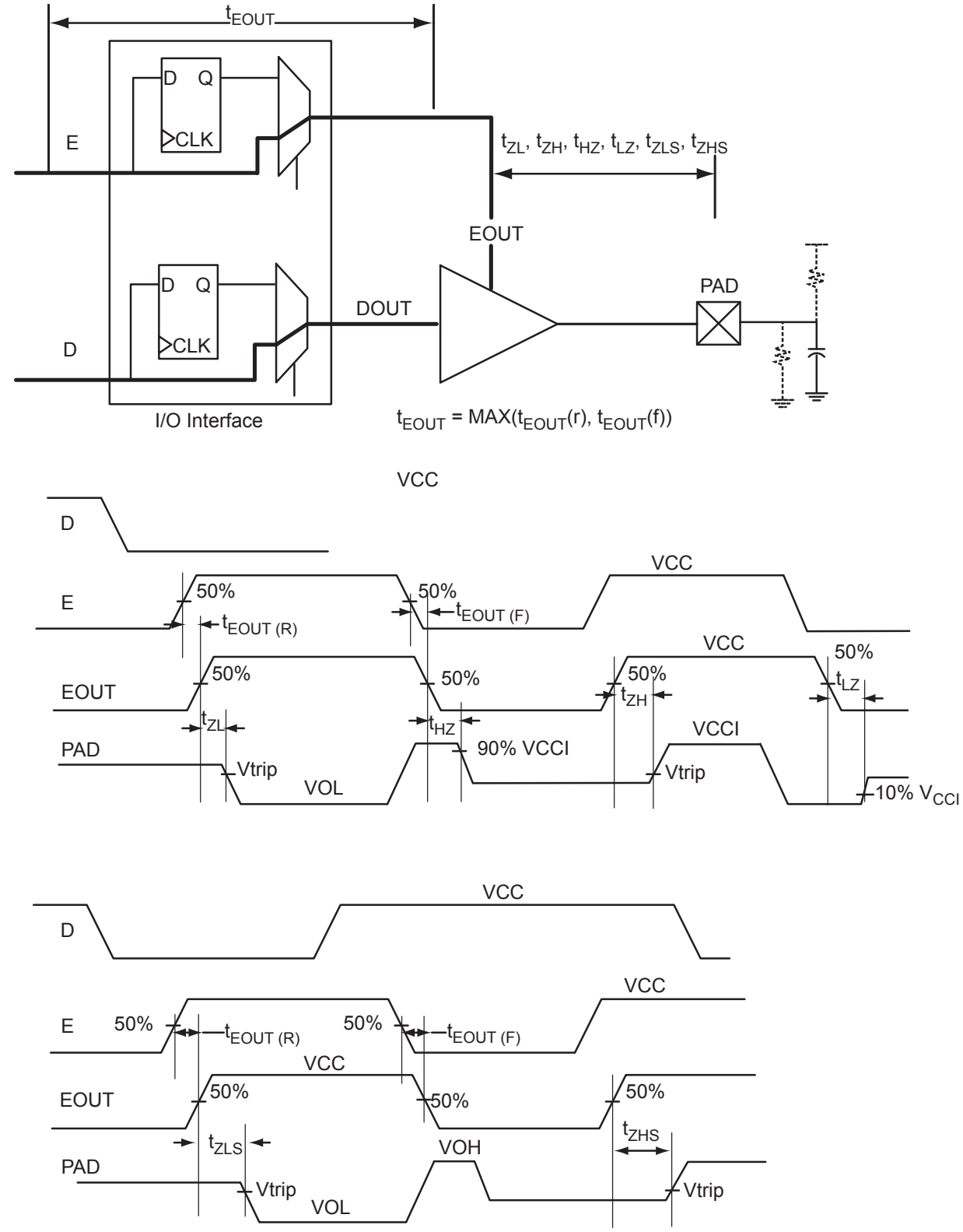


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	**IOSL (mA)***	**IOSH (mA)***
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 µA	26	20

*Note: *T_J = 100°C*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-70 • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-71 • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Fully Registered I/O Buffers with Asynchronous Clear

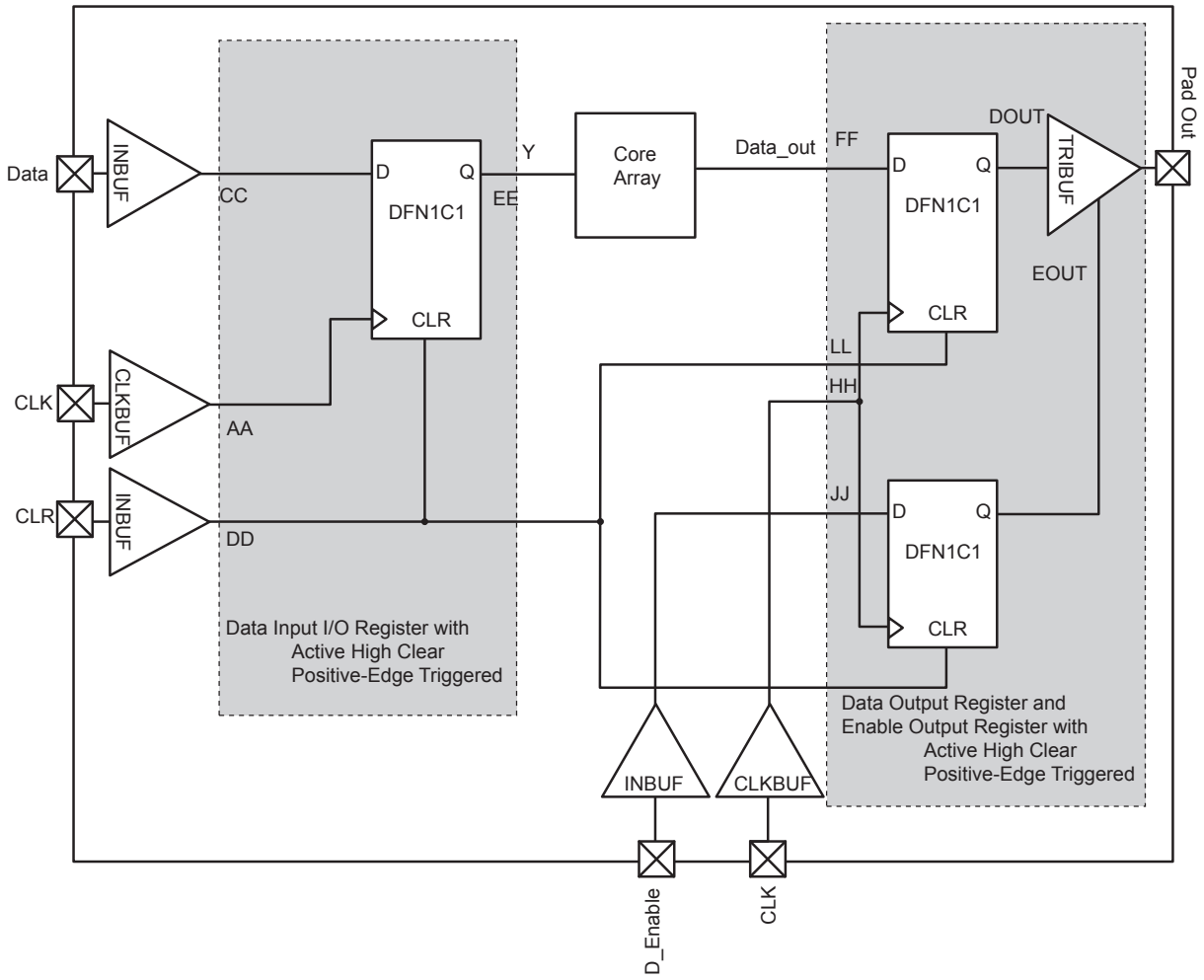


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

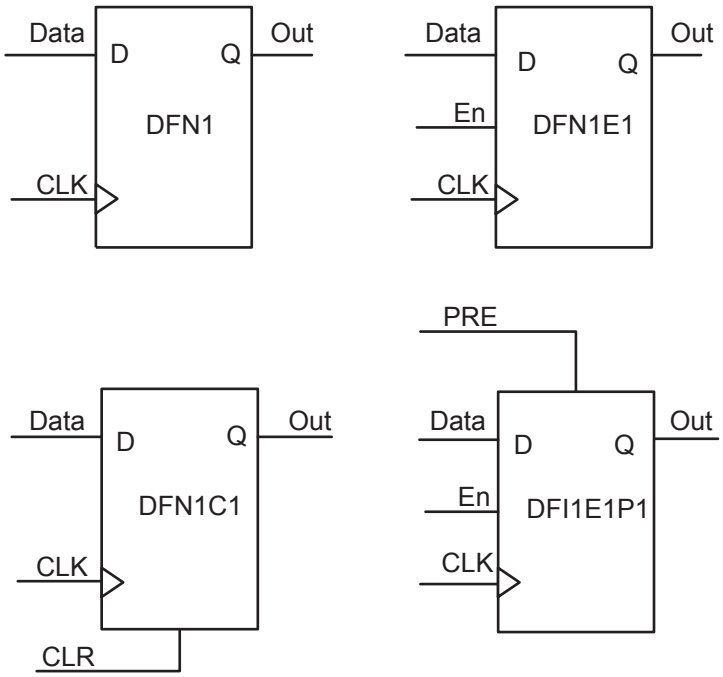


Figure 2-19 • **Sample of Sequential Cells**

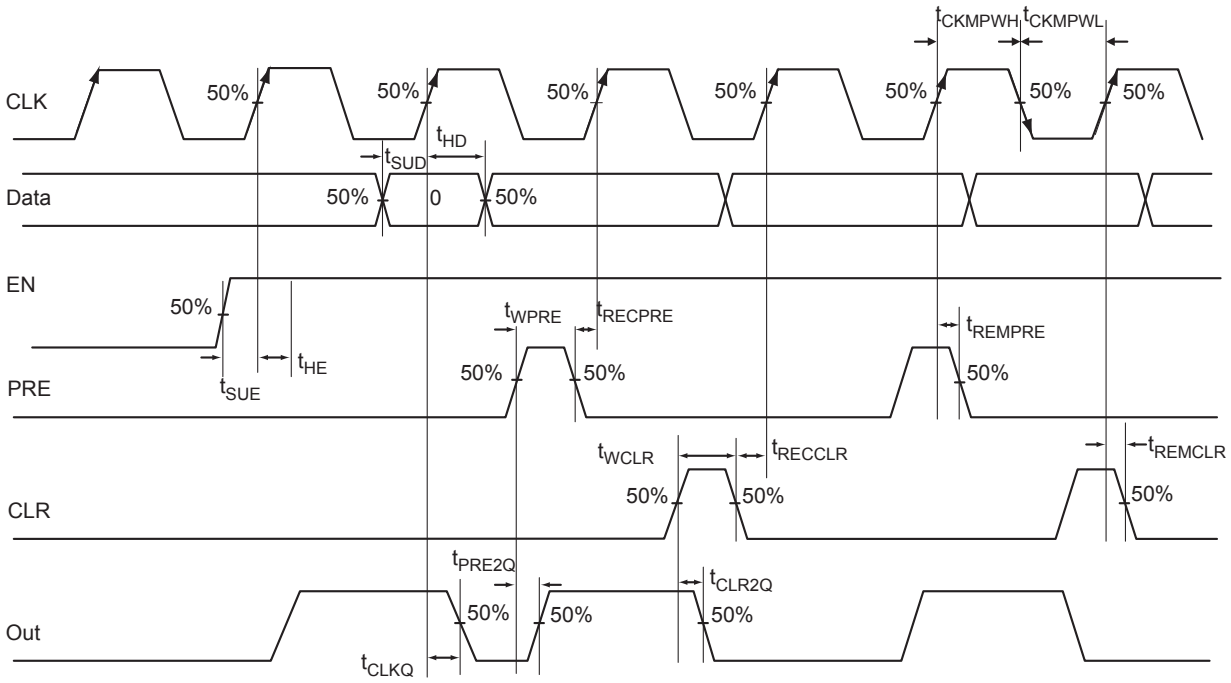


Figure 2-20 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-86 • AGLP125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-87 • AGLP030 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-88 • AGLP060 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.43	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-89 • AGLP125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-96 • FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.68	ns
	RESET Low to Data Out Low on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Embedded FlashROM Characteristics

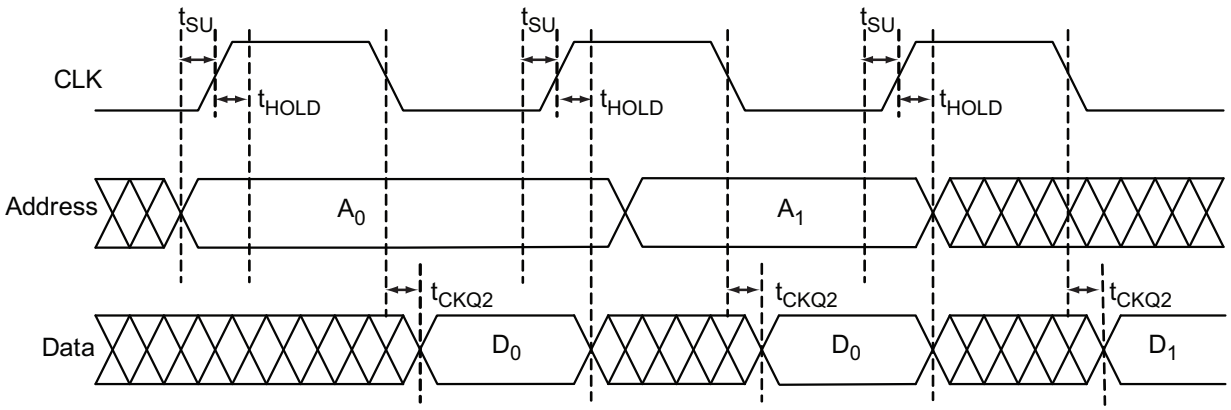


Figure 2-37 • **Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	17.58	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

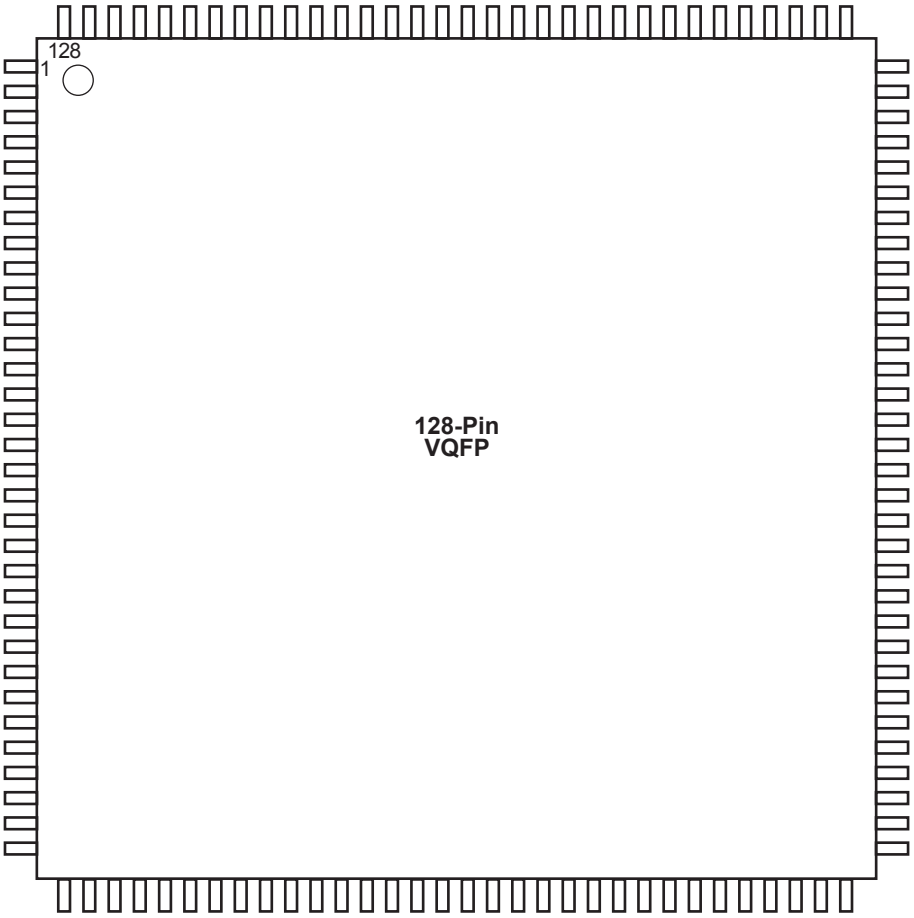
1.2 V DC Core Voltage

Table 2-99 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	30.94	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

4 – Package Pin Assignments

VQ128



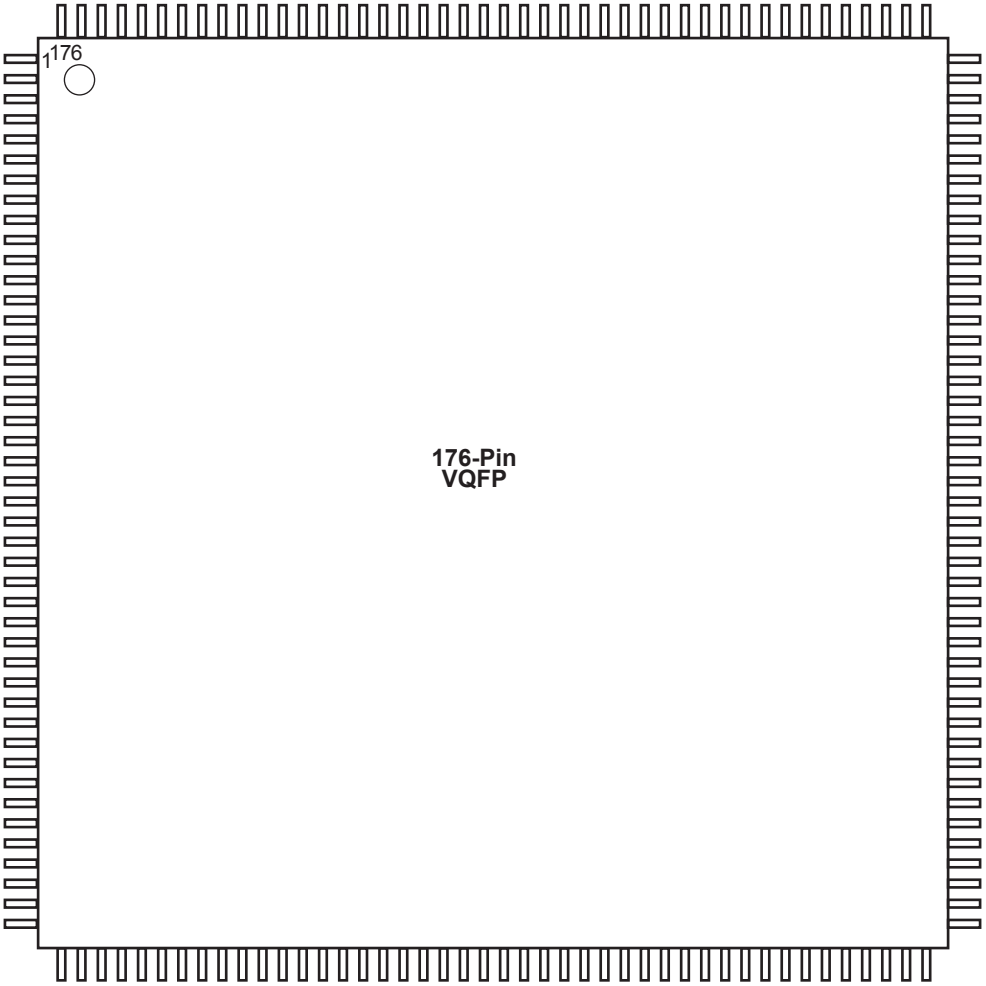
Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

VQ176



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS201	
Pin Number	AGLP060 Function
A1	IO150RSB3
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	IO08RSB0
A5	IO11RSB0
A6	IO15RSB0
A7	IO17RSB0
A8	IO18RSB0
A9	IO22RSB0
A10	IO26RSB0
A11	IO29RSB0
A12	GBC1/IO31RSB0
A13	GBA2/IO36RSB1
A14	IO41RSB1
A15	NC
B1	IO151RSB3
B2	GAB2/IO154RSB3
B3	IO06RSB0
B4	IO09RSB0
B5	IO13RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO25RSB0
B11	IO24RSB0
B12	IO27RSB0
B13	IO37RSB1
B14	IO46RSB1
B15	IO42RSB1
C1	IO155RSB3
C2	GAA2/IO156RSB3
C3	GND
C4	GAA1/IO01RSB0
C5	GAB1/IO03RSB0

CS201	
Pin Number	AGLP060 Function
C6	IO07RSB0
C7	IO16RSB0
C8	IO21RSB0
C9	IO28RSB0
C10	GBB1/IO33RSB0
C11	GBA1/IO35RSB0
C12	GBB2/IO38RSB1
C13	GND
C14	IO48RSB1
C15	IO39RSB1
D1	IO146RSB3
D2	IO144RSB3
D3	IO148RSB3
D4	GND
D5	GAB0/IO02RSB0
D6	GAC1/IO05RSB0
D7	IO14RSB0
D8	IO19RSB0
D9	GBC0/IO30RSB0
D10	GBB0/IO32RSB0
D11	GBA0/IO34RSB0
D12	GND
D13	GBC2/IO40RSB1
D14	IO51RSB1
D15	IO44RSB1
E1	IO142RSB3
E2	IO149RSB3
E3	IO153RSB3
E4	GAC2/IO152RSB3
E12	IO43RSB1
E13	IO49RSB1
E14	GCC0/IO53RSB1
E15	GCB0/IO55RSB1
F1	IO141RSB3
F2	GFC1/IO140RSB3

CS201	
Pin Number	AGLP060 Function
F3	IO145RSB3
F4	IO147RSB3
F6	GND
F7	VCC
F8	VCCIB0
F9	VCCIB0
F10	VCCIB0
F12	IO47RSB1
F13	IO45RSB1
F14	GCC1/IO52RSB1
F15	GCA1/IO56RSB1
G1*	VCOMPLF
G2	GFB0/IO137RSB3
G3	GFC0/IO139RSB3
G4	IO143RSB3
G6	VCCIB3
G7	GND
G8	VCC
G9	GND
G10	GND
G12	IO50RSB1
G13	GCB1/IO54RSB1
G14	GCC2/IO60RSB1
G15	GCA2/IO58RSB1
H1*	VCCPLF
H2	GFA1/IO136RSB3
H3	GFB1/IO138RSB3
H4	NC
H6	VCCIB3
H7	GND
H8	VCC
H9	GND
H10	VCCIB1
H12	GCB2/IO59RSB1
H13	GCA0/IO57RSB1

*Note: *Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.*

CS201	
Pin Number	AGLP060 Function
H14	IO64RSB1
H15	IO62RSB1
J1	GFA2/IO134RSB3
J2	GFA0/IO135RSB3
J3	GFB2/IO133RSB3
J4	IO131RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	IO61RSB1
J13	IO63RSB1
J14	IO68RSB1
J15	IO66RSB1
K1	IO130RSB3
K2	GFC2/IO132RSB3
K3	IO127RSB3
K4	IO129RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	IO65RSB1
K13	IO67RSB1
K14	IO69RSB1
K15	IO70RSB1
L1	IO126RSB3
L2	IO128RSB3
L3	IO121RSB3
L4	IO123RSB3
L12	GDB1/IO74RSB1
L13	GDC1/IO72RSB1
L14	IO71RSB1

CS201	
Pin Number	AGLP060 Function
L15	GDC0/IO73RSB1
M1	IO122RSB3
M2	IO124RSB3
M3	IO119RSB3
M4	GND
M5	IO125RSB3
M6	IO98RSB2
M7	IO96RSB2
M8	IO91RSB2
M9	IO89RSB2
M10	IO82RSB2
M11	GDA2/IO78RSB2
M12	GND
M13	GDA1/IO76RSB1
M14	GDA0/IO77RSB1
M15	GDB0/IO75RSB1
N1	IO117RSB3
N2	IO120RSB3
N3	GND
N4	GEB1/IO114RSB3
N5	IO107RSB2
N6	IO100RSB2
N7	IO94RSB2
N8	IO87RSB2
N9	IO85RSB2
N10	GDC2/IO80RSB2
N11	IO90RSB2
N12	IO84RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	GEC0/IO115RSB3
P2	GEC1/IO116RSB3
P3	GEA0/IO111RSB3
P4	GEA1/IO112RSB3

CS201	
Pin Number	AGLP060 Function
P5	IO106RSB2
P6	IO105RSB2
P7	IO103RSB2
P8	IO99RSB2
P9	IO93RSB2
P10	IO92RSB2
P11	IO95RSB2
P12	IO86RSB2
P13	IO83RSB2
P14	VPUMP
P15	TRST
R1	IO118RSB3
R2	GEB0/IO113RSB3
R3	GEA2/IO110RSB2
R4	FF/GEB2/IO109RSB2
R5	GEC2/IO108RSB2
R6	IO102RSB2
R7	IO101RSB2
R8	IO104RSB2
R9	IO97RSB2
R10	IO88RSB2
R11	IO81RSB2
R12	GDB2/IO79RSB2
R13	TMS
R14	TDI
R15	TCK

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

Revision	Changes	Page
Revision 17 (December 2015)	Updated Commercial and Industrial temperature range to show junction temperature in "IGLOO PLUS Ordering Information" section and "Temperature Grade Offerings" section (SAR 73547).	1-III, 1-IV
	Removed Ambient temperature parameter in Table 2-2 • Recommended Operating Conditions[1,2] (SAR 73547).	2-2
	Table notes are added to Table 2-2 • Recommended Operating Conditions[1,2] stating that: • VMV pins must be connected to the corresponding VCCI pins. • Software default junction temperature range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial.	2-2
	Updated Table 2-5 • Package Thermal Resistivities (SAR 60078).	2-6
	Added 2 mA drive strength information in the following tables (SAR 57182): • Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage • Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage • Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage • Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-28, 2-28, 2-28, 2-29
	Fixed typo for "VQ128" section in "Package Pin Assignments" section	4-1
Revision 16 (December 2012)	The "IGLOO PLUS Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43175).	III
	The note in Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42566).	2-61, 2-62
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 15 (October 2012)	Values updated for IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage in Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices and for IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage in Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices (SAR 31988). Also added a new Note to the two tables.	2-10, 2-11
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40277).	N/A
Revision 14 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2

Revision	Changes	Page
Revision 11 (continued)	Table 2-2 • Recommended Operating Conditions[1,2] was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were revised.	2-6, 2-6
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
	VIH maximum values in tables were updated as needed to 3.6 V (SARs 20990, 79370).	N/A
	The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable. Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Table 2-22 • Summary of Maximum and Minimum DC Input Levels Table 2-23 • Summary of AC Measuring Points Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-28 • I/O Output Buffer Maximum Resistances [1]	2-9 2-9 2-19 2-20 2-20 2-22 2-23 2-24
	A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.	2-10, 2-11
	Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining $R_{WEAK\ PULL\text{-}UP\text{-}MAX}$ and $R_{WEAK\ PULLDOWN\text{-}MAX}$ were revised (SAR 21348).	2-25
	Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).	2-25
	Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).	2-26

Revision	Changes	Page
Revision 3 (continued)	The table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode* to remove the sentence stating that values do not include I/O static contribution.	2-7
	The table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode* was updated to remove VJTAG and VCCI and the statement that values do not include I/O static contribution.	2-7
	The table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode was updated to remove the statement that values do not include I/O static contribution.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash*Freeze Mode 1 was updated to include VCCPLL. Table note 4 was deleted.	2-8
	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] were updated to remove static power. The table notes were updated to reflect that power was measured on VCC_I. Table note 2 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings.	2-9, 2-9
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices were updated to change the definition for P_{DC5} from bank static power to bank quiescent power. Table subtitles were added for Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices, Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices, and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices.	2-10, 2-11
	The "Total Static Power Consumption—P_{STAT}" section was revised.	2-12
	Table 2-32 • Schmitt Trigger Input Hysteresis is new.	2-26
Packaging v1.3	The "CS281" package drawing is new.	4-13
	The "CS281" table for the AGLP125 device is new.	4-13
Revision 3 (continued)	The "CS289" package drawing was incorrect. The graphic was showing the CS281 mechanical drawing and not the CS289 mechanical drawing. This has now been corrected.	4-17
Revision 2 (Jun 2008) Packaging v1.2	The "CS289" table for the AGLP030 device is new.	4-17
Revision 1 (Jun 2008) Packaging v1.1	The "CS289" table for the AGLP060 device is new.	4-20
	The "CS289" table for the AGLP125 device is new.	4-23

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

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