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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	157
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	201-VFBGA, CSBGA
Supplier Device Package	201-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v5-cs201

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated

Table 2-2 • **Recommended Operating Conditions[1,2]**

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction temperature[2]		0 to + 85	–40 to +100	°C
VCC[3]	1.5 V DC core supply voltage [4]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[5,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP[7]	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[4]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core voltage[5]	1.14 to 1.575	1.14 to 1.575	V
VCCI	1.2 V DC supply voltage[5]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage[5]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V wide range DC supply voltage[9]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-19. VCCI should be at the same voltage within a given I/O bank.*
4. *For IGLOO® PLUS V5 devices*
5. *For IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*
6. *All IGLOO PLUS devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the Pin Descriptions chapter of the IGLOO PLUS FPGA Fabric User's Guide for further information.*
9. *3.3 V wide range is compliant to the JDEC8b specification and supports 3.0 V VCCI operation.*
10. *VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User's Guide for further information.*
11. *Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{(°C/W)}} = \frac{100°C - 70°C}{20.5°C/W} = 1.46\ W$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{jb}	θ_{ja} Still Air	θ_{ja} 1 m/s	θ_{ja} 2.5 m/s	Unit
Chip Scale Package (CSP)	AGLP030	CS201	-	-	46.3	-	-	C/W
	AGLP060	CS201	7.1	19.7	40.5	35.1	32.9	C/W
	AGLP060	CS289	13.9	34.1	48.7	43.5	41.9	C/W
	AGLP125	CS289	10.8	27.9	42.2	37.1	35.5	C/W
	AGLP125	CS281	11.3	17.6	-	-	-	C/W
Thin Quad Flat Package (VQ)	AGLP030	VQ128	18.0	50.0	56.0	49.0	47.0	C/W
	AGLP060	VQ176	21.0	55.0	58.0	52.0	50.0	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.5	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V)**
For IGLOO PLUS V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.963	0.975	0.989	1.000	1.007	1.011
1.2	0.853	0.865	.0877	0.893	0.893	0.897
1.26	0.781	0.792	0.803	0.813	0.819	0.822

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode***

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	µA
	1.5 V	6	10	18	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode***

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	µA

Note: *IDD = N_{BANKS} * ICCI

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	µA

Power per I/O Pin

Table 2-13 **• Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range[2]	3.3	16.26
3.3 V LVCMOS Wide Range[2] – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS[3]	1.2	0.55
1.2 V LVCMOS[3] – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range[3]	1.2	0.55
1.2 V LVCMOS Wide Range[3] – Schmitt Trigger	1.2	0.47

Notes:

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

Table 2-14 **• Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range[3]	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS[4]	5	1.2	15.22
1.2 V LVCMOS Wide Range[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

***Table 2-21* • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-22 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[5]	10	10	15	15
1.2 V LVCMOS Wide Range[5]	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Applicable to IGLOO PLUS V2 devices operating at VCCI ³ VCC.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V

Table 2-24 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Detailed I/O DC Characteristics

Table 2-27 **• Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-28 **• I/O Output Buffer Maximum Resistances** [1]

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) [2]	$R_{PULL-UP}$ (Ω) [3]
3.3 V LVTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	157.5	163.8
1.2 V LVCMOS Wide Range[4]	100 µA	157.5	163.8

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC_I, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS model on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL-DOWN-MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL-UP-MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Applicable to IGLOO PLUS V2 devices operating at VCCI ≥ VCC.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-42 **• 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.97	5.85	0.18	1.18	1.64	0.66	5.86	5.05	2.57	2.57	ns
100 µA	6 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 µA	8 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 µA	12 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns
100 µA	16 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-6 on page 2-6* *for derating values.*

Table 2-43 **• 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.97	3.39	0.18	1.18	1.64	0.66	3.41	2.69	2.57	2.73	ns
100 µA	6 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 µA	8 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 µA	12 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
100 µA	16 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-6 on page 2-6* *for derating values.*
3. *Software default selection highlighted in gray.*

Input Register

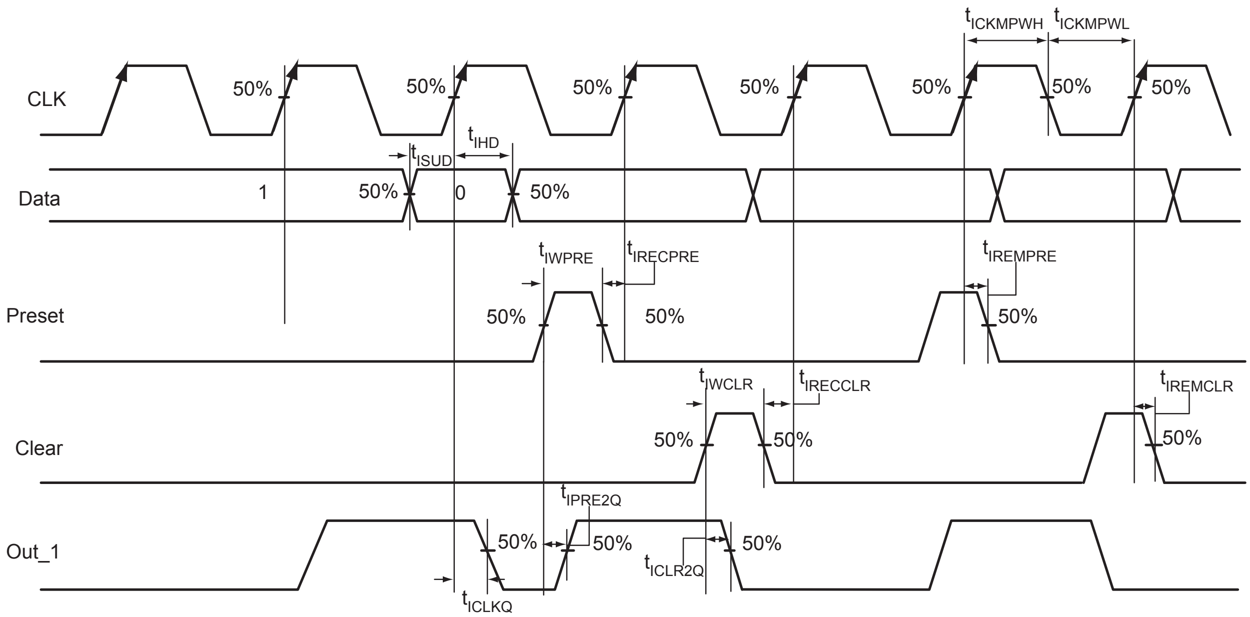


Figure 2-14 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.41	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-88 **• AGLP060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.43	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-89 **• AGLP125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-90 **• IGLOO PLUS CCC/PLL Specification**
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.20%
50 MHz to 250 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support a PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate, VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide.*

Timing Waveforms

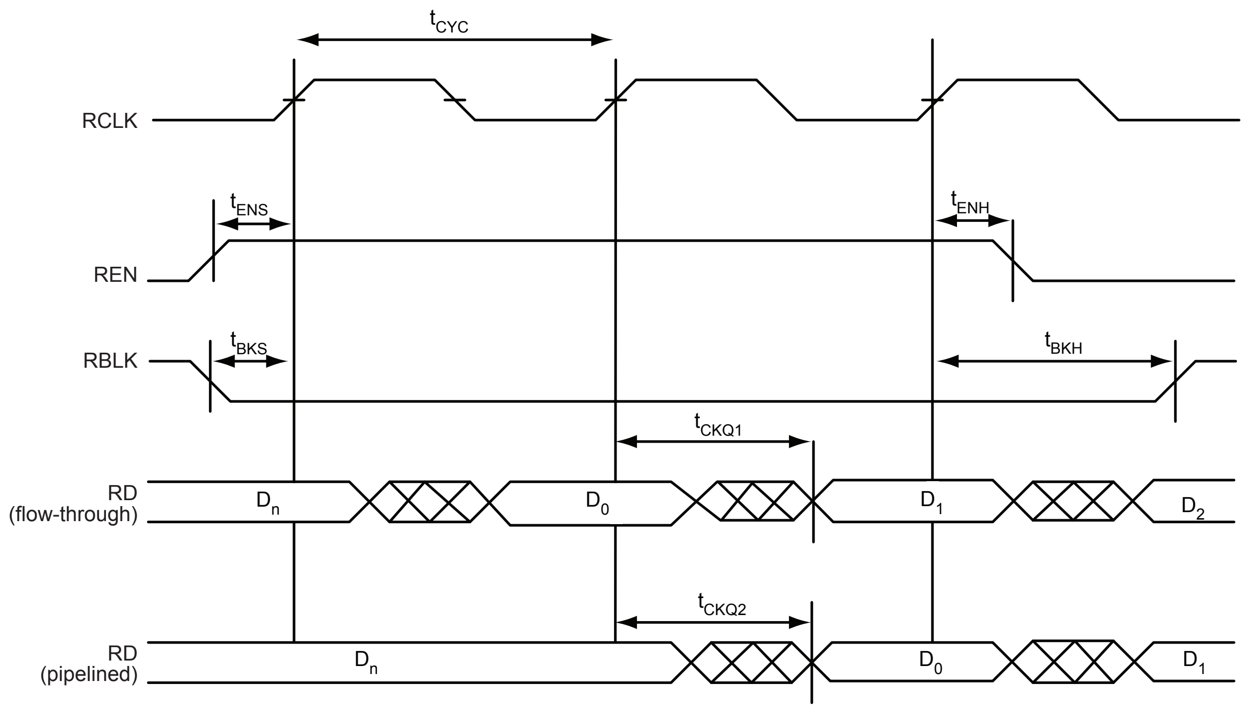


Figure 2-30 • **FIFO Read**

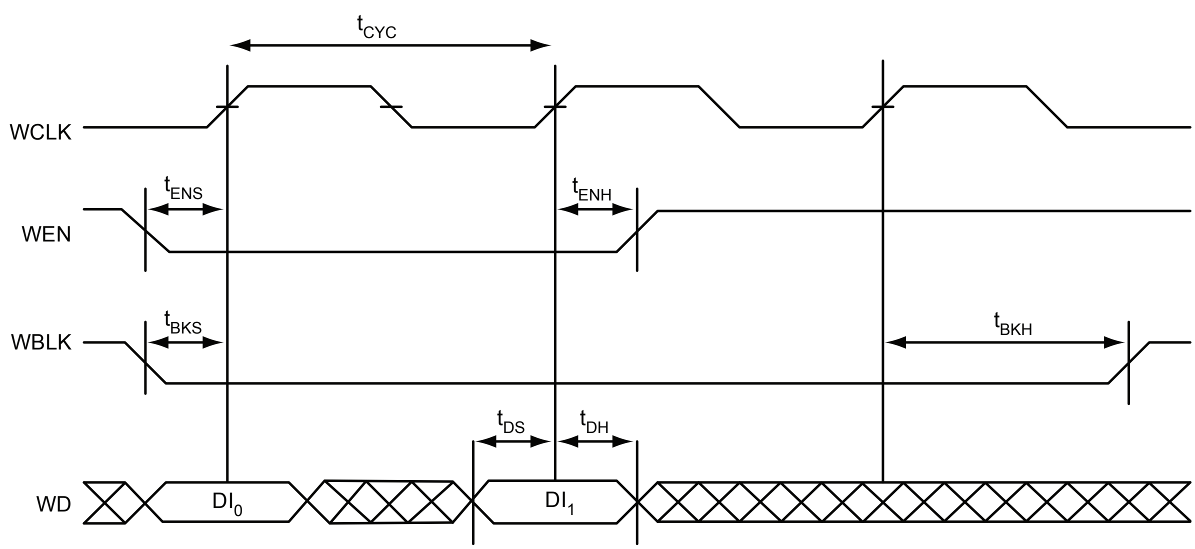


Figure 2-31 • **FIFO Write**

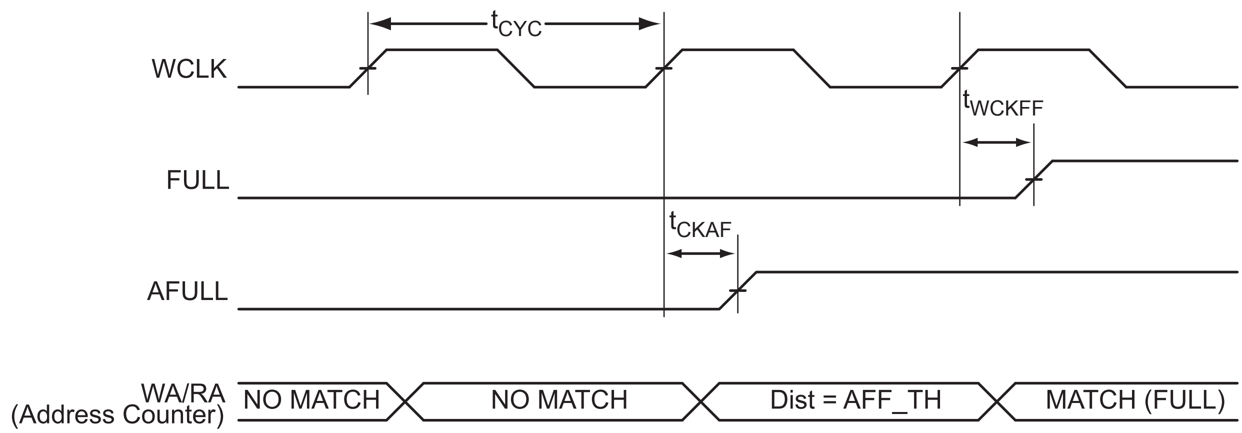


Figure 2-34 • **FIFO FULL Flag and AFULL Flag Assertion**

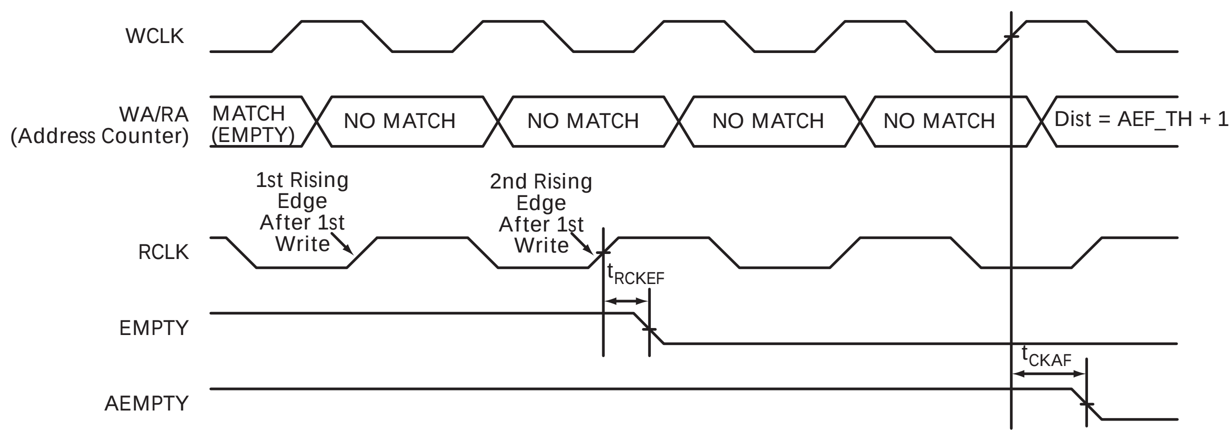


Figure 2-35 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

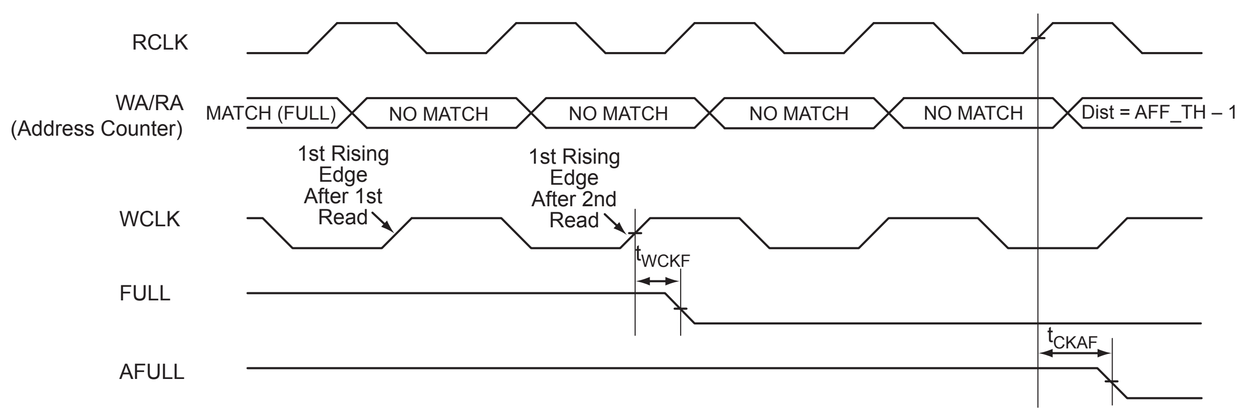
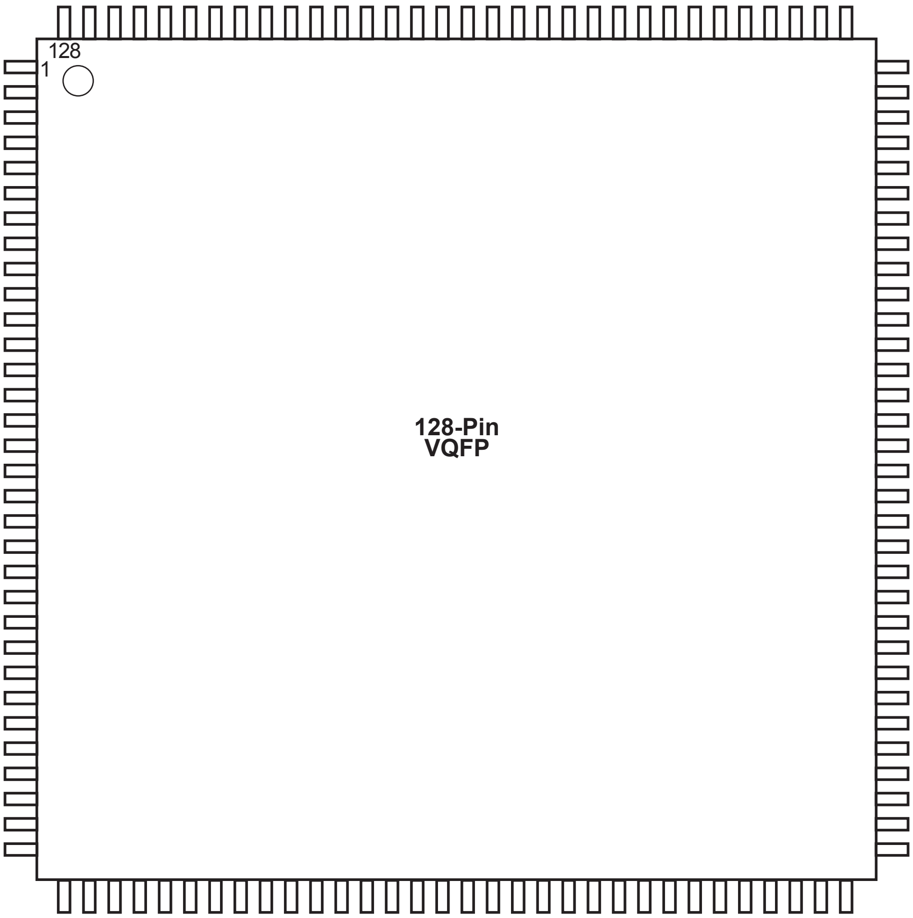


Figure 2-36 • **FIFO FULL Flag and AFULL Flag Deassertion**

4 – Package Pin Assignments

VQ128



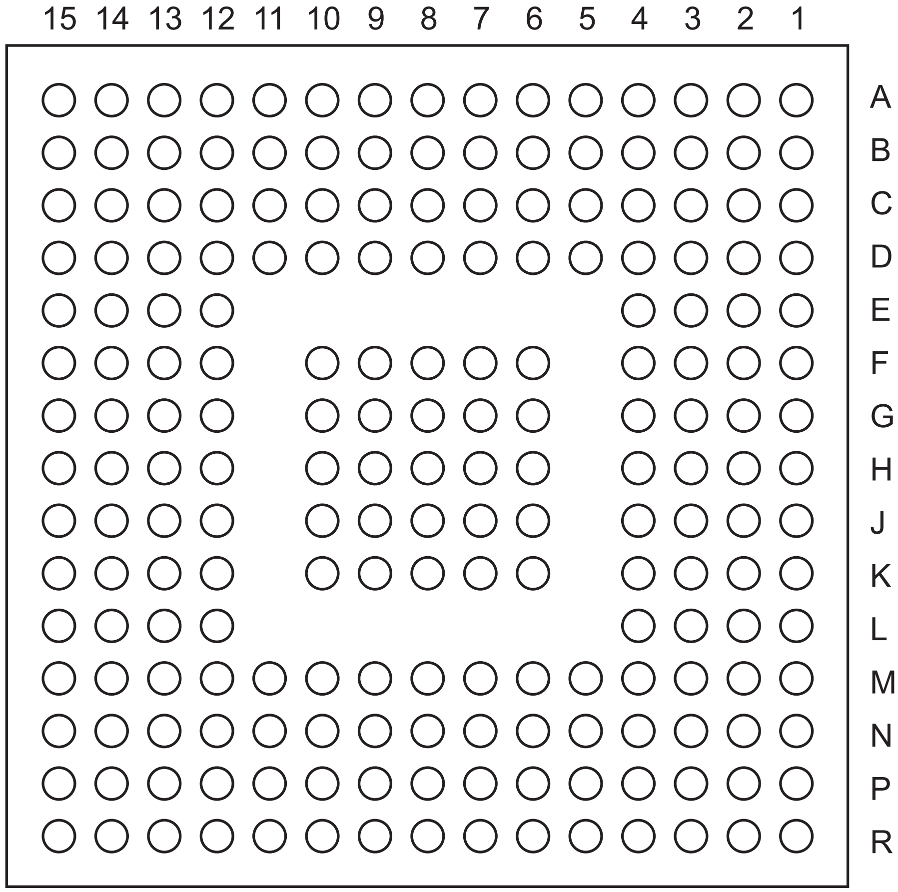
Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

CS201

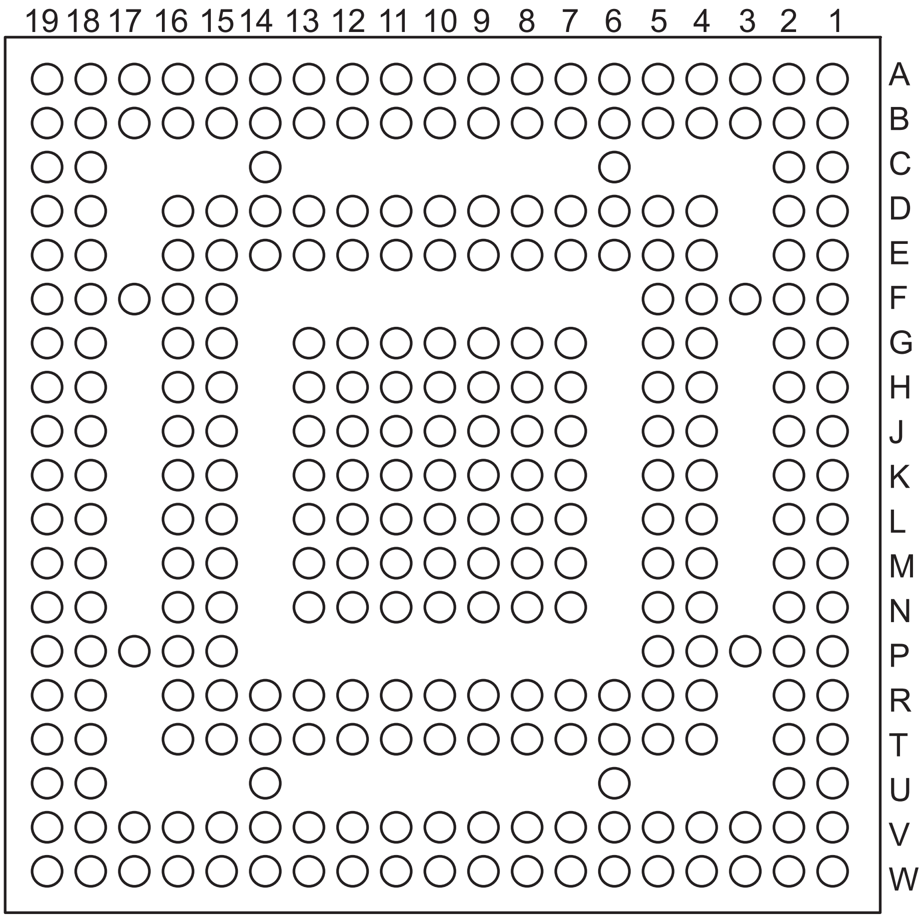


Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS281



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CS289	
Pin Number	AGLP030 Function
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0

CS289	
Pin Number	AGLP030 Function
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC

CS289	
Pin Number	AGLP030 Function
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

CS289	
Pin Number	AGLP125 Function
A1	GAB1/IO03RSB0
A2	IO11RSB0
A3	IO08RSB0
A4	GND
A5	IO19RSB0
A6	IO24RSB0
A7	IO26RSB0
A8	IO30RSB0
A9	GND
A10	IO35RSB0
A11	IO38RSB0
A12	IO40RSB0
A13	IO42RSB0
A14	GND
A15	IO48RSB0
A16	IO54RSB0
A17	GBC0/IO57RSB0
B1	GAA1/IO01RSB0
B2	GND
B3	IO06RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO21RSB0
B7	VCCIB0
B8	IO28RSB0
B9	IO31RSB0
B10	IO37RSB0
B11	IO39RSB0
B12	VCCIB0
B13	IO44RSB0
B14	IO46RSB0
B15	IO49RSB0
B16	GBC1/IO58RSB0
B17	GND
C1	IO210RSB3
C2	GAA0/IO00RSB0
C3	GAC0/IO04RSB0
C4	IO09RSB0

CS289	
Pin Number	AGLP125 Function
C5	VCCIB0
C6	IO17RSB0
C7	IO23RSB0
C8	IO27RSB0
C9	IO33RSB0
C10	GND
C11	IO43RSB0
C12	IO45RSB0
C13	IO50RSB0
C14	IO52RSB0
C15	GND
C16	GBA0/IO61RSB0
C17	IO68RSB1
D1	IO204RSB3
D2	IO205RSB3
D3	GND
D4	GAB0/IO02RSB0
D5	IO07RSB0
D6	IO10RSB0
D7	IO18RSB0
D8	GND
D9	IO34RSB0
D10	IO41RSB0
D11	IO47RSB0
D12	IO55RSB0
D13	GND
D14	GBB0/IO59RSB0
D15	GBA1/IO62RSB0
D16	IO66RSB1
D17	IO70RSB1
E1	VCCIB3
E2	IO200RSB3
E3	GAC2/IO207RSB3
E4	GAA2/IO211RSB3
E5	GAC1/IO05RSB0
E6	IO12RSB0
E7	IO16RSB0
E8	IO22RSB0

CS289	
Pin Number	AGLP125 Function
E9	IO32RSB0
E10	IO36RSB0
E11	VCCIB0
E12	IO56RSB0
E13	GBB1/IO60RSB0
E14	GBA2/IO63RSB1
E15	GBB2/IO65RSB1
E16	VCCIB1
E17	IO73RSB1
F1	GFC1/IO194RSB3
F2	IO196RSB3
F3	IO202RSB3
F4	VCCIB3
F5	GAB2/IO209RSB3
F6	IO208RSB3
F7	IO14RSB0
F8	IO20RSB0
F9	IO25RSB0
F10	IO29RSB0
F11	IO51RSB0
F12	IO53RSB0
F13	GBC2/IO67RSB1
F14	GND
F15	IO75RSB1
F16	IO71RSB1
F17	IO77RSB1
G1	GFC0/IO193RSB3
G2	GND
G3	IO198RSB3
G4	IO203RSB3
G5	IO201RSB3
G6	IO206RSB3
G7	GND
G8	GND
G9	VCC
G10	GND
G11	GND
G12	IO72RSB1