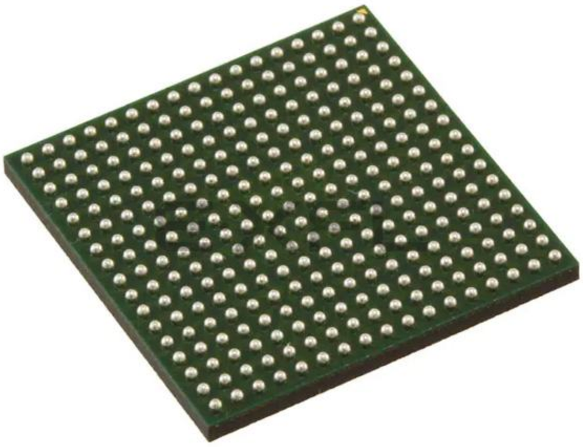


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	157
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v5-cs289

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode***

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	µA
	1.5 V	6	10	18	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode***

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	µA

*Note: *IDD = N_{BANKS} * ICCI*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	µA

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE}*PAC2 + N_{ROW}*PAC3 + N_{S\text{-}CELL}* PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

***Table 2-24* • I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Applies to 1.2 V DC Core Voltage

***Table 2-44* • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.98	6.68	0.19	1.32	1.92	0.67	6.68	5.74	3.13	3.47	ns
100 µA	6 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 µA	8 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 µA	12 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns
100 µA	16 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-45* • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.98	4.16	0.19	1.32	1.92	0.67	4.16	3.32	3.12	3.66	ns
100 µA	6 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 µA	8 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 µA	12 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
100 µA	16 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.89	0.18	1.00	1.43	0.66	6.01	5.43	1.78	1.30	ns
4 mA	STD	0.97	4.82	0.18	1.00	1.43	0.66	4.92	4.56	2.08	2.08	ns
6 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns
8 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.82	0.18	1.00	1.43	0.66	2.88	2.78	1.78	1.35	ns
4 mA	STD	0.97	2.30	0.18	1.00	1.43	0.66	2.35	2.11	2.08	2.15	ns
6 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
8 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.43	0.19	1.12	1.61	0.67	6.54	5.93	2.19	1.88	ns
4 mA	STD	0.98	5.33	0.19	1.12	1.61	0.67	5.41	5.03	2.50	2.68	ns
6 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns
8 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.30	0.19	1.12	1.61	0.67	3.34	3.21	2.19	1.93	ns
4 mA	STD	0.98	2.76	0.19	1.12	1.61	0.67	2.79	2.51	2.50	2.76	ns
6 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
8 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-64 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	μA[5]	μA[5]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

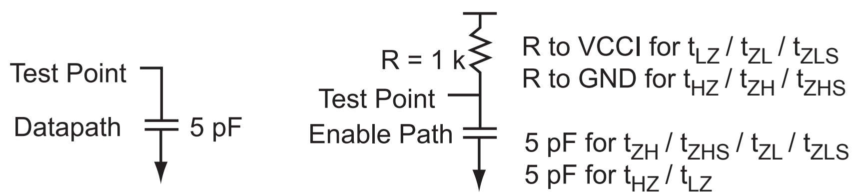


Figure 2-11 • **AC Loading**

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-66 • 1.2 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-67 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

***Table 2-70* • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-71* • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Global Resource Characteristics

AGLP125 Clock Tree Topology

Clock delays are device-specific. Figure 2-21 is an example of a global tree used for clock routing. The global tree presented in Figure 2-21 is driven by a CCC located on the west side of the AGLP125 device. It is used to drive all D-flip-flops in the device.

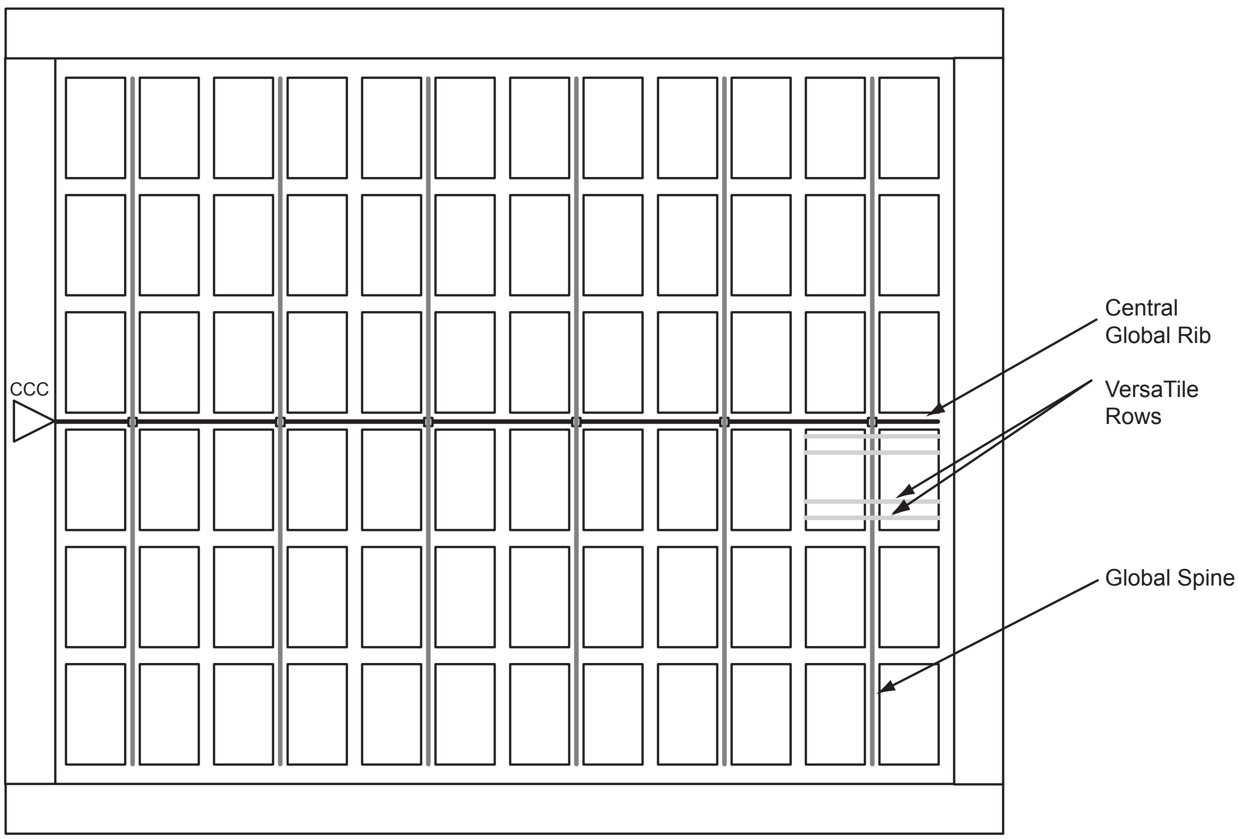


Figure 2-21 **• Example of Global Tree Use in an AGLP125 Device for Clock Routing**

Table 2-86 • **AGLP125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-87 • **AGLP030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns

Notes:

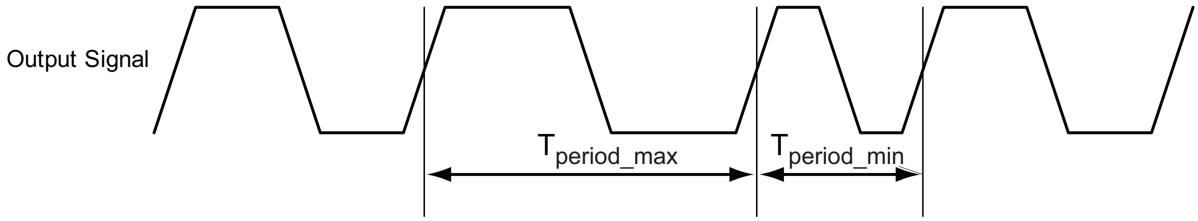
1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

***Table 2-91* • IGLOO PLUS CCC/PLL Specification**
For IGLOO PLUS V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			60	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			.25	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.863		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]		5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	1.20%	2.00%	3.00%
50 MHz to 160 MHz	2.50%	5.00%	7.00%	15.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the online help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions.For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements are done with LVTTL 3.3 V, 8 mA, I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain, and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-22 • **Peak-to-Peak Jitter Definition**

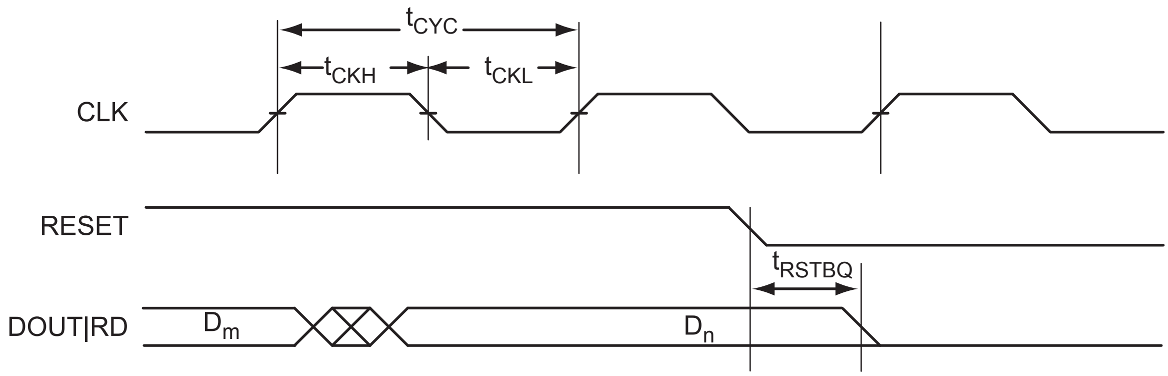
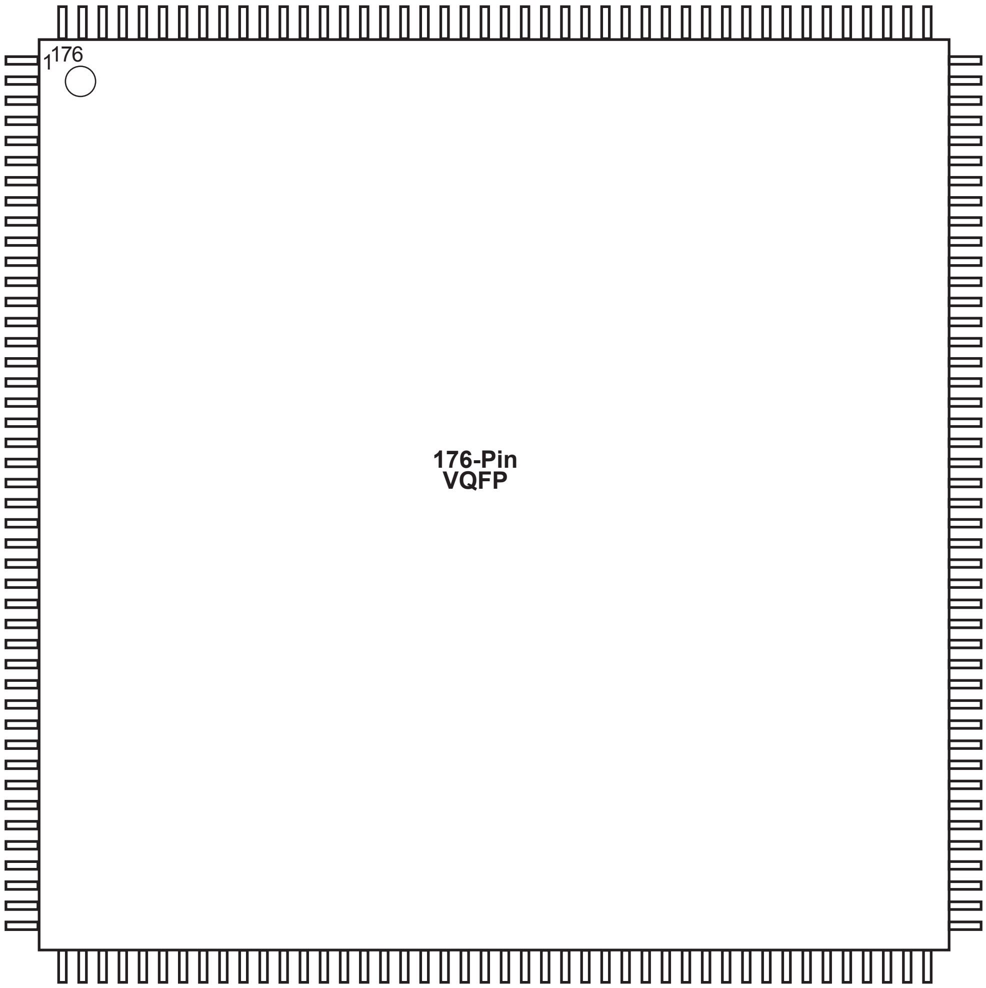


Figure 2-28 • **RAM Reset**

VQ176



Note: This is the bottom view of the package.

Note

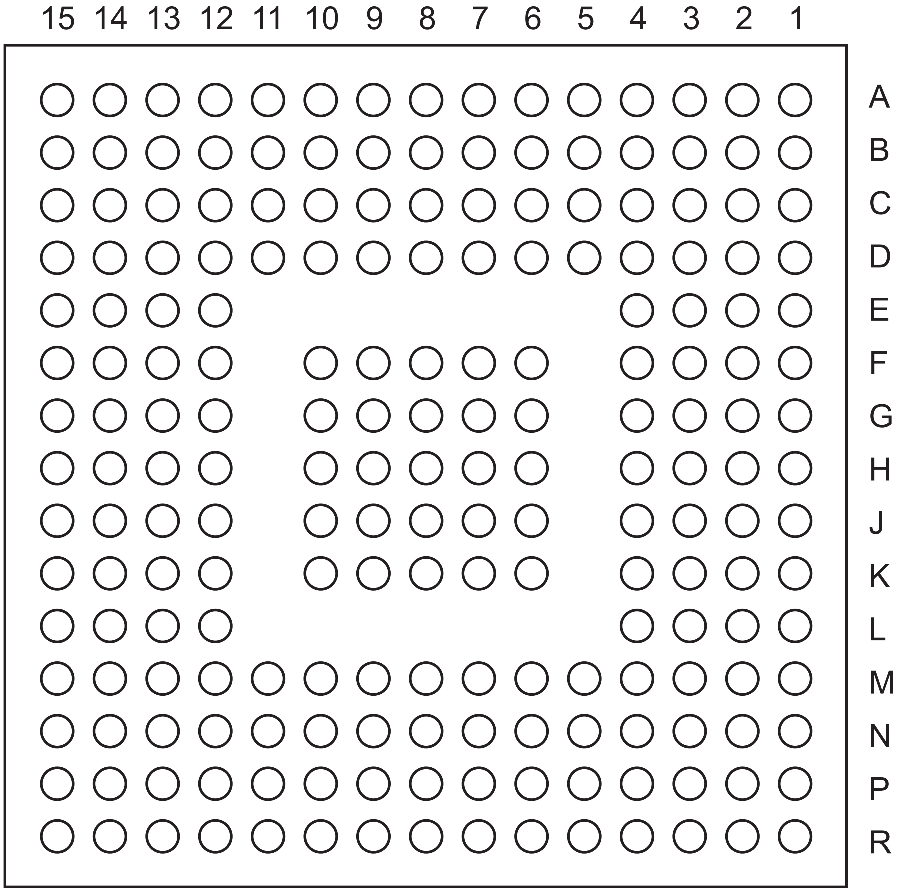
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ176	
Pin Number	AGLP060 Function
105	IO62RSB1
106	IO61RSB1
107	GCC2/IO60RSB1
108	GCB2/IO59RSB1
109	GCA2/IO58RSB1
110	GCA0/IO57RSB1
111	GCA1/IO56RSB1
112	VCCIB1
113	GND
114	GCB0/IO55RSB1
115	GCB1/IO54RSB1
116	GCC0/IO53RSB1
117	GCC1/IO52RSB1
118	IO51RSB1
119	IO50RSB1
120	VCC
121	IO48RSB1
122	IO47RSB1
123	IO45RSB1
124	IO44RSB1
125	IO43RSB1
126	VCCIB1
127	GND
128	GBC2/IO40RSB1
129	IO39RSB1
130	GBB2/IO38RSB1
131	IO37RSB1
132	GBA2/IO36RSB1
133	GBA1/IO35RSB0
134	NC
135	GBA0/IO34RSB0
136	NC
137	GBB1/IO33RSB0
138	NC
139	GBC1/IO31RSB0

VQ176	
Pin Number	AGLP060 Function
140	GBB0/IO32RSB0
141	GBC0/IO30RSB0
142	IO29RSB0
143	IO28RSB0
144	IO27RSB0
145	VCCIB0
146	GND
147	IO26RSB0
148	IO25RSB0
149	IO24RSB0
150	IO23RSB0
151	IO22RSB0
152	IO21RSB0
153	IO20RSB0
154	IO19RSB0
155	IO18RSB0
156	VCC
157	IO17RSB0
158	IO16RSB0
159	IO15RSB0
160	IO14RSB0
161	IO13RSB0
162	IO12RSB0
163	IO11RSB0
164	IO10RSB0
165	IO09RSB0
166	VCCIB0
167	GND
168	IO07RSB0
169	IO08RSB0
170	GAC1/IO05RSB0
171	IO06RSB0
172	GAB1/IO03RSB0
173	GAC0/IO04RSB0
174	GAB0/IO02RSB0

VQ176	
Pin Number	AGLP060 Function
175	GAA1/IO01RSB0
176	GAA0/IO00RSB0

CS201



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS281	
Pin Number	AGLP125 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO23RSB0
A9	IO25RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO41RSB0
A13	IO43RSB0
A14	IO46RSB0
A15	IO55RSB0
A16	IO56RSB0
A17	GBC1/IO58RSB0
A18	GBA0/IO61RSB0
A19	GND
B1	GAA2/IO211RSB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO11RSB0
B6	GND
B7	IO21RSB0
B8	IO22RSB0
B9	IO28RSB0
B10	IO32RSB0
B11	IO36RSB0
B12	IO39RSB0
B13	IO42RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO57RSB0
B17	GBA1/IO62RSB0

CS281	
Pin Number	AGLP125 Function
B18	VCCIB1
B19	IO64RSB1
C1	GAB2/IO209RSB3
C2	IO210RSB3
C6	IO12RSB0
C14	IO47RSB0
C18	IO54RSB0
C19	GBB2/IO65RSB1
D1	IO206RSB3
D2	IO208RSB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO10RSB0
D7	IO17RSB0
D8	IO24RSB0
D9	IO27RSB0
D10	GND
D11	IO31RSB0
D12	IO40RSB0
D13	IO49RSB0
D14	IO45RSB0
D15	GBB0/IO59RSB0
D16	GBA2/IO63RSB1
D18	GBC2/IO67RSB1
D19	IO66RSB1
E1	IO203RSB3
E2	IO205RSB3
E4	IO07RSB0
E5	IO06RSB0
E6	IO14RSB0
E7	IO20RSB0
E8	IO29RSB0
E9	IO34RSB0
E10	IO30RSB0
E11	IO37RSB0
E12	IO38RSB0

CS281	
Pin Number	AGLP125 Function
E13	IO48RSB0
E14	GBB1/IO60RSB0
E15	IO53RSB0
E16	IO69RSB1
E18	IO68RSB1
E19	IO71RSB1
F1	IO198RSB3
F2	GND
F3	IO201RSB3
F4	IO204RSB3
F5	IO16RSB0
F15	IO50RSB0
F16	IO74RSB1
F17	IO72RSB1
F18	GND
F19	IO73RSB1
G1	IO195RSB3
G2	IO200RSB3
G4	IO202RSB3
G5	IO08RSB0
G7	GAC2/IO207RSB3
G8	VCCIB0
G9	IO26RSB0
G10	IO35RSB0
G11	IO44RSB0
G12	VCCIB0
G13	IO51RSB0
G15	IO70RSB1
G16	IO75RSB1
G18	GCC0/IO80RSB1
G19	GCB1/IO81RSB1
H1	GFB0/IO191RSB3
H2	IO196RSB3
H4	GFC1/IO194RSB3
H5	GFB1/IO192RSB3
H7	VCCIB3

CS289	
Pin Number	AGLP030 Function
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0

CS289	
Pin Number	AGLP030 Function
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC

CS289	
Pin Number	AGLP030 Function
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

CS289	
Pin Number	AGLP030 Function
G10	GND
G11	GND
G12	IO40RSB1
G13	NC
G14	IO39RSB1
G15	IO44RSB1
G16	NC
G17	GND
H1	NC
H2	GEC0/IO108RSB3
H3	NC
H4	IO112RSB3
H5	NC
H6	IO109RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	NC
H13	NC
H14	IO45RSB1
H15	VCCIB1
H16	GDB0/IO48RSB1
H17	IO42RSB1
J1	NC
J2	GEA0/IO107RSB3
J3	VCCIB3
J4	IO105RSB3
J5	NC
J6	NC
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	IO50RSB1

CS289	
Pin Number	AGLP030 Function
J13	IO43RSB1
J14	IO51RSB1
J15	IO52RSB1
J16	GDC0/IO46RSB1
J17	GDA0/IO47RSB1
K1	GND
K2	GEB0/IO106RSB3
K3	IO102RSB3
K4	IO104RSB3
K5	IO99RSB3
K6	NC
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	NC
K13	NC
K14	NC
K15	IO53RSB1
K16	GND
K17	IO49RSB1
L1	IO103RSB3
L2	IO101RSB3
L3	NC
L4	GND
L5	NC
L6	NC
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	IO58RSB1
L13	IO54RSB1
L14	VCCIB1
L15	NC

CS289	
Pin Number	AGLP030 Function
L16	NC
L17	NC
M1	NC
M2	VCCIB3
M3	IO100RSB3
M4	IO98RSB3
M5	IO93RSB3
M6	IO97RSB3
M7	NC
M8	NC
M9	IO71RSB2
M10	NC
M11	IO63RSB2
M12	NC
M13	IO57RSB1
M14	NC
M15	NC
M16	NC
M17	VCCIB1
N1	NC
N2	NC
N3	IO95RSB3
N4	IO96RSB3
N5	GND
N6	NC
N7	IO85RSB2
N8	IO79RSB2
N9	IO77RSB2
N10	VCCIB2
N11	NC
N12	NC
N13	IO59RSB2
N14	NC
N15	GND
N16	IO56RSB1
N17	IO55RSB1
P1	IO94RSB3

Revision	Changes	Page
Revision 11 (continued)	The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying IIL and IIH were added. Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366). Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).	2-32
	The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.	2-45 through 2-56
	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM", "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-78

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.