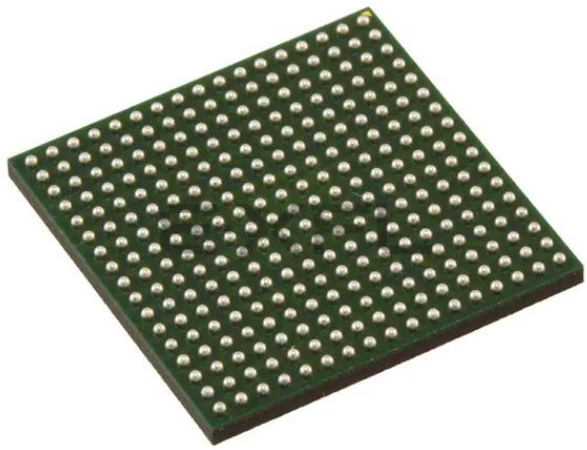

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	157
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v5-cs289i

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE}*PAC2 + N_{ROW}*PAC3 + $N_{S\text{-}CELL}$* PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

User I/O Characteristics

Timing Model

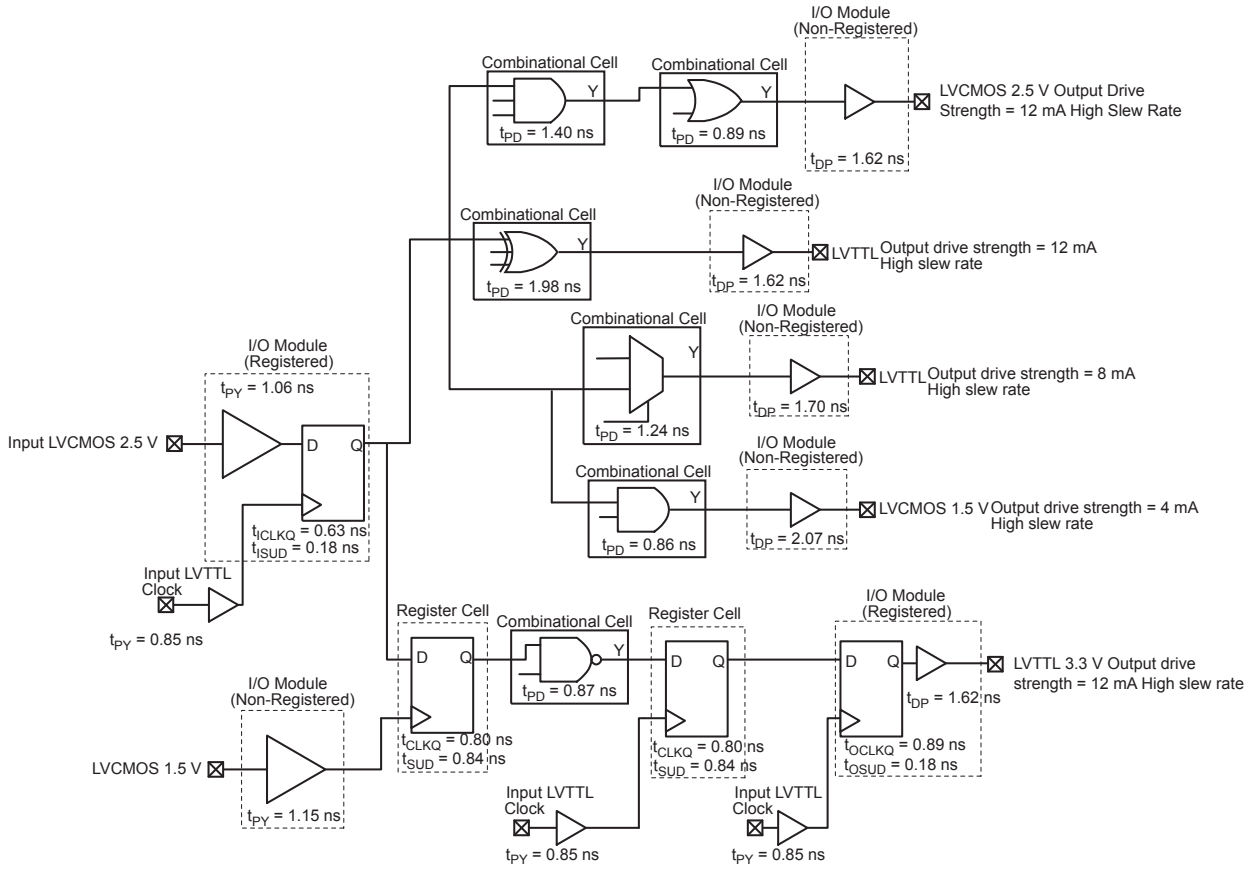

Figure 2-3 • **Timing Model**
Operating Conditions: STD Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Table 2-24 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

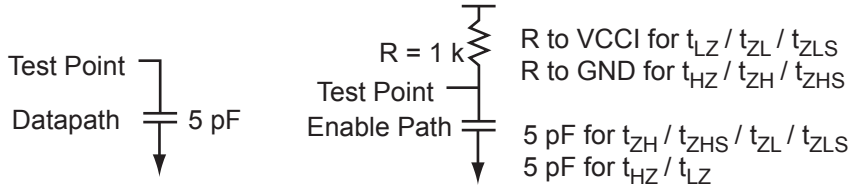

Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.89	0.18	1.00	1.43	0.66	6.01	5.43	1.78	1.30	ns
4 mA	STD	0.97	4.82	0.18	1.00	1.43	0.66	4.92	4.56	2.08	2.08	ns
6 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns
8 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.82	0.18	1.00	1.43	0.66	2.88	2.78	1.78	1.35	ns
4 mA	STD	0.97	2.30	0.18	1.00	1.43	0.66	2.35	2.11	2.08	2.15	ns
6 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
8 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.43	0.19	1.12	1.61	0.67	6.54	5.93	2.19	1.88	ns
4 mA	STD	0.98	5.33	0.19	1.12	1.61	0.67	5.41	5.03	2.50	2.68	ns
6 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns
8 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.30	0.19	1.12	1.61	0.67	3.34	3.21	2.19	1.93	ns
4 mA	STD	0.98	2.76	0.19	1.12	1.61	0.67	2.79	2.51	2.50	2.76	ns
6 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
8 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

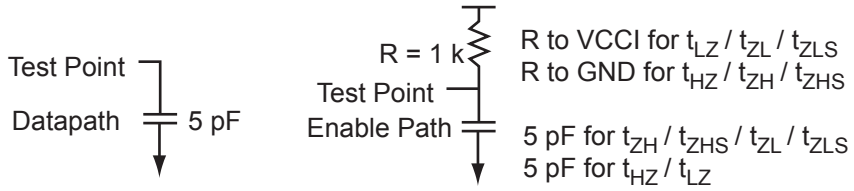

Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

I/O Register Specifications

Fully Registered I/O Buffers with Asynchronous Preset

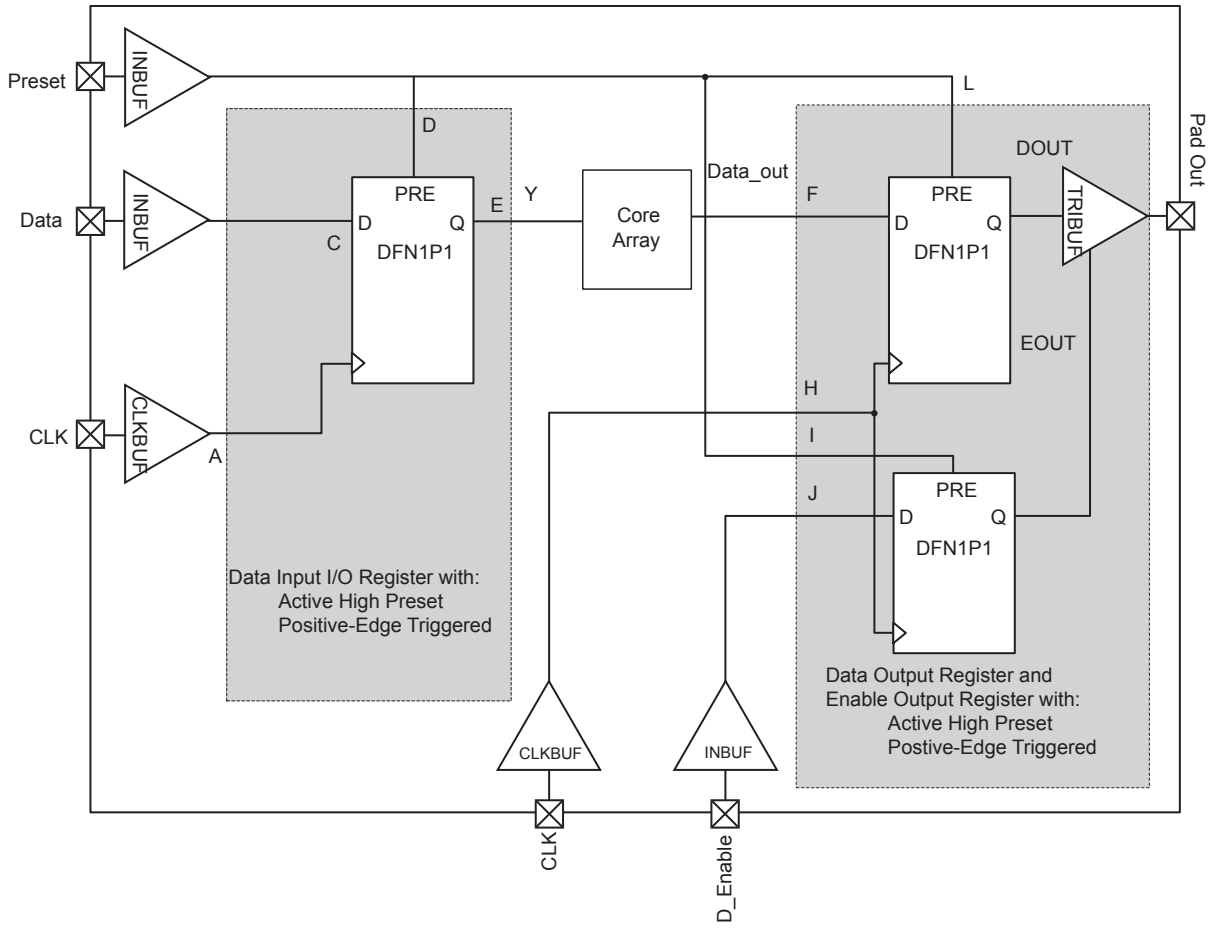

Figure 2-12 • **Timing Model of Registered I/O Buffers with Asynchronous Preset**

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

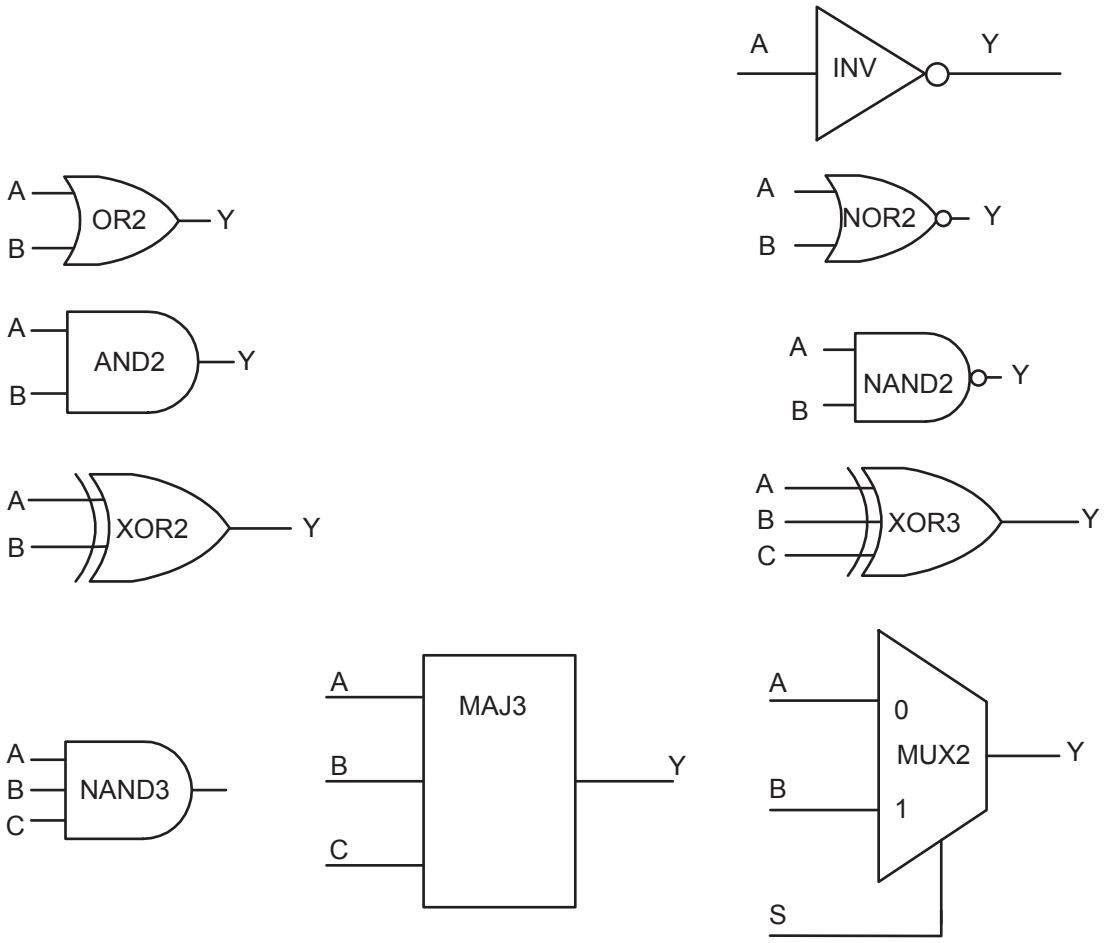

Figure 2-17 • **Sample of Combinatorial Cells**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.72	ns
AND2	Y = A · B	t_{PD}	0.86	ns
NAND2	Y = !(A · B)	t_{PD}	1.00	ns
OR2	Y = A + B	t_{PD}	1.26	ns
NOR2	Y = !(A + B)	t_{PD}	1.16	ns
XOR2	Y = A ⊕ B	t_{PD}	1.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.47	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	2.12	ns
MUX2	Y = A !S + B S	t_{PD}	1.24	ns
AND3	Y = A · B · C	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-81 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.26	ns
AND2	Y = A · B	t_{PD}	1.46	ns
NAND2	Y = !(A · B)	t_{PD}	1.78	ns
OR2	Y = A + B	t_{PD}	2.47	ns
NOR2	Y = !(A + B)	t_{PD}	2.17	ns
XOR2	Y = A ⊕ B	t_{PD}	2.62	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.66	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.77	ns
MUX2	Y = A !S + B S	t_{PD}	2.20	ns
AND3	Y = A · B · C	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

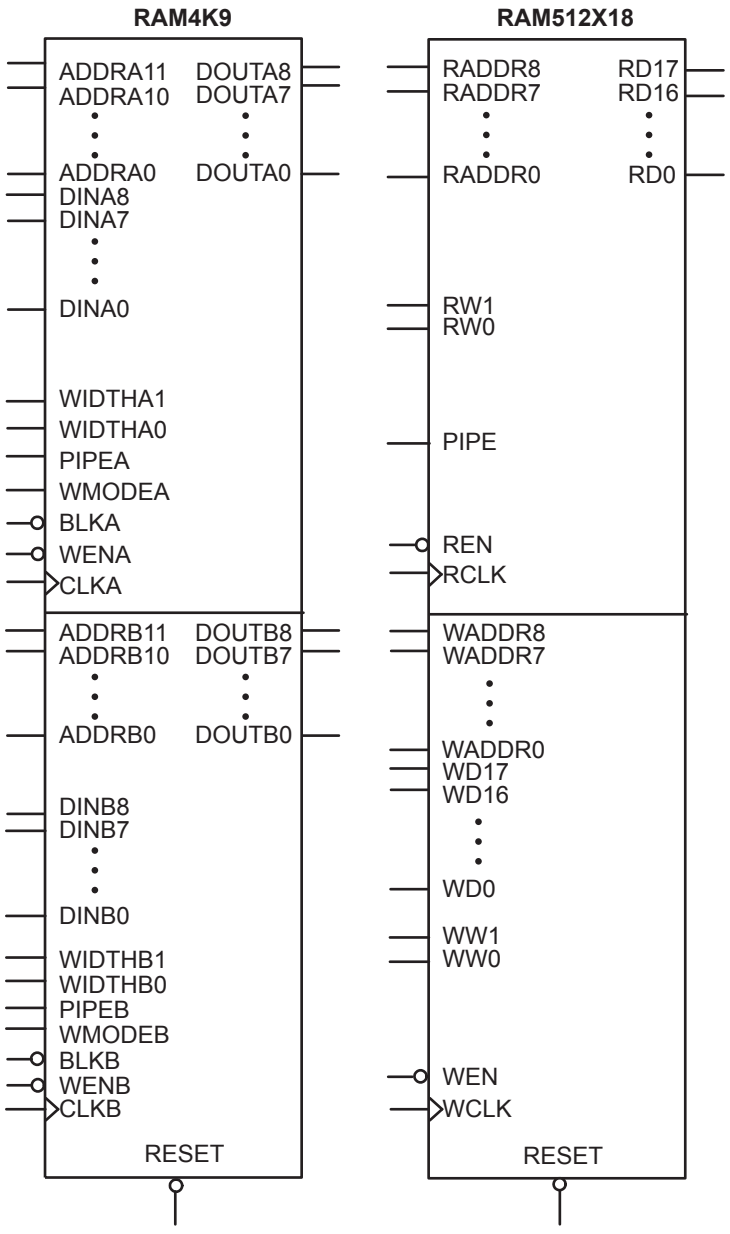

Figure 2-23 • **RAM Models**

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-100* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-101* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

IGLOO PLUS Device Family User's Guide

http://www.microsemi.com/soc/documents/IGLOOPLUS_UG.pdf

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are available at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ176	
Pin Number	AGLP060 Function
1	GAA2/IO156RSB3
2	IO155RSB3
3	GAB2/IO154RSB3
4	IO153RSB3
5	GAC2/IO152RSB3
6	GND
7	VCCIB3
8	IO149RSB3
9	IO147RSB3
10	IO145RSB3
11	IO144RSB3
12	IO143RSB3
13	VCC
14	IO141RSB3
15	GFC1/IO140RSB3
16	GFB1/IO138RSB3
17	GFB0/IO137RSB3
18	VCOMPLF
19	GFA1/IO136RSB3
20	VCCPLF
21	GFA0/IO135RSB3
22	GND
23	VCCIB3
24	GFA2/IO134RSB3
25	GFB2/IO133RSB3
26	GFC2/IO132RSB3
27	IO131RSB3
28	IO130RSB3
29	IO129RSB3
30	IO127RSB3
31	IO126RSB3
32	IO125RSB3
33	IO123RSB3
34	IO122RSB3
35	IO121RSB3

VQ176	
Pin Number	AGLP060 Function
36	IO119RSB3
37	GND
38	VCCIB3
39	GEC1/IO116RSB3
40	GEB1/IO114RSB3
41	GEC0/IO115RSB3
42	GEB0/IO113RSB3
43	GEA1/IO112RSB3
44	GEA0/IO111RSB3
45	GEA2/IO110RSB2
46	NC
47	FF/GEB2/IO109RSB2
48	GEC2/IO108RSB2
49	IO106RSB2
50	IO107RSB2
51	IO104RSB2
52	IO105RSB2
53	IO102RSB2
54	IO103RSB2
55	GND
56	VCCIB2
57	IO101RSB2
58	IO100RSB2
59	IO99RSB2
60	IO98RSB2
61	IO97RSB2
62	IO96RSB2
63	IO95RSB2
64	IO94RSB2
65	IO93RSB2
66	VCC
67	IO92RSB2
68	IO91RSB2
69	IO90RSB2

VQ176	
Pin Number	AGLP060 Function
70	IO89RSB2
71	IO88RSB2
72	IO87RSB2
73	IO86RSB2
74	IO85RSB2
75	IO84RSB2
76	GND
77	VCCIB2
78	IO83RSB2
79	IO82RSB2
80	GDC2/IO80RSB2
81	IO81RSB2
82	GDA2/IO78RSB2
83	GDB2/IO79RSB2
84	NC
85	NC
86	TCK
87	TDI
88	TMS
89	VPUMP
90	TDO
91	TRST
92	VJTAG
93	GDA1/IO76RSB1
94	GDC0/IO73RSB1
95	GDB1/IO74RSB1
96	GDC1/IO72RSB1
97	VCCIB1
98	GND
99	IO70RSB1
100	IO69RSB1
101	IO67RSB1
102	IO66RSB1
103	IO65RSB1
104	IO63RSB1

CS201	
Pin Number	AGLP030 Function
A1	NC
A2	IO04RSB0
A3	IO06RSB0
A4	IO09RSB0
A5	IO11RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO18RSB0
A9	IO24RSB0
A10	IO26RSB0
A11	IO27RSB0
A12	IO31RSB0
A13	NC
A14	NC
A15	NC
B1	NC
B2	NC
B3	IO08RSB0
B4	IO05RSB0
B5	IO07RSB0
B6	IO15RSB0
B7	IO14RSB0
B8	IO16RSB0
B9	IO20RSB0
B10	IO22RSB0
B11	IO34RSB0
B12	IO29RSB0
B13	NC
B14	NC
B15	NC
C1	NC
C2	NC
C3	GND
C4	IO00RSB0
C5	IO02RSB0

CS201	
Pin Number	AGLP030 Function
C6	IO12RSB0
C7	IO23RSB0
C8	IO19RSB0
C9	IO28RSB0
C10	IO32RSB0
C11	IO35RSB0
C12	NC
C13	GND
C14	IO41RSB1
C15	IO37RSB1
D1	IO117RSB3
D2	IO118RSB3
D3	NC
D4	GND
D5	IO01RSB0
D6	IO03RSB0
D7	IO10RSB0
D8	IO21RSB0
D9	IO25RSB0
D10	IO30RSB0
D11	IO33RSB0
D12	GND
D13	NC
D14	IO36RSB1
D15	IO39RSB1
E1	IO115RSB3
E2	IO114RSB3
E3	NC
E4	NC
E12	NC
E13	NC
E14	GDC0/IO46RSB1
E15	GDB0/IO48RSB1
F1	IO113RSB3
F2	IO116RSB3

CS201	
Pin Number	AGLP030 Function
F3	IO119RSB3
F4	IO111RSB3
F6	GND
F7	VCC
F8	VCCIB0
F9	VCCIB0
F10	VCCIB0
F12	NC
F13	NC
F14	IO40RSB1
F15	IO38RSB1
G1	NC
G2	IO112RSB3
G3	IO110RSB3
G4	IO109RSB3
G6	VCCIB3
G7	GND
G8	VCC
G9	GND
G10	GND
G12	NC
G13	NC
G14	IO42RSB1
G15	IO44RSB1
H1	NC
H2	GEB0/IO106RSB3
H3	GEC0/IO108RSB3
H4	NC
H6	VCCIB3
H7	GND
H8	VCC
H9	GND
H10	VCCIB1
H12	IO54RSB1
H13	GDA0/IO47RSB1

CS201	
Pin Number	AGLP060 Function
H14	IO64RSB1
H15	IO62RSB1
J1	GFA2/IO134RSB3
J2	GFA0/IO135RSB3
J3	GFB2/IO133RSB3
J4	IO131RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	IO61RSB1
J13	IO63RSB1
J14	IO68RSB1
J15	IO66RSB1
K1	IO130RSB3
K2	GFC2/IO132RSB3
K3	IO127RSB3
K4	IO129RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	IO65RSB1
K13	IO67RSB1
K14	IO69RSB1
K15	IO70RSB1
L1	IO126RSB3
L2	IO128RSB3
L3	IO121RSB3
L4	IO123RSB3
L12	GDB1/IO74RSB1
L13	GDC1/IO72RSB1
L14	IO71RSB1

CS201	
Pin Number	AGLP060 Function
L15	GDC0/IO73RSB1
M1	IO122RSB3
M2	IO124RSB3
M3	IO119RSB3
M4	GND
M5	IO125RSB3
M6	IO98RSB2
M7	IO96RSB2
M8	IO91RSB2
M9	IO89RSB2
M10	IO82RSB2
M11	GDA2/IO78RSB2
M12	GND
M13	GDA1/IO76RSB1
M14	GDA0/IO77RSB1
M15	GDB0/IO75RSB1
N1	IO117RSB3
N2	IO120RSB3
N3	GND
N4	GEB1/IO114RSB3
N5	IO107RSB2
N6	IO100RSB2
N7	IO94RSB2
N8	IO87RSB2
N9	IO85RSB2
N10	GDC2/IO80RSB2
N11	IO90RSB2
N12	IO84RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	GEC0/IO115RSB3
P2	GEC1/IO116RSB3
P3	GEA0/IO111RSB3
P4	GEA1/IO112RSB3

CS201	
Pin Number	AGLP060 Function
P5	IO106RSB2
P6	IO105RSB2
P7	IO103RSB2
P8	IO99RSB2
P9	IO93RSB2
P10	IO92RSB2
P11	IO95RSB2
P12	IO86RSB2
P13	IO83RSB2
P14	VPUMP
P15	TRST
R1	IO118RSB3
R2	GEB0/IO113RSB3
R3	GEA2/IO110RSB2
R4	FF/GEB2/IO109RSB2
R5	GEC2/IO108RSB2
R6	IO102RSB2
R7	IO101RSB2
R8	IO104RSB2
R9	IO97RSB2
R10	IO88RSB2
R11	IO81RSB2
R12	GDB2/IO79RSB2
R13	TMS
R14	TDI
R15	TCK

CS289	
Pin Number	AGLP060 Function
G13	IO41RSB1
G14	IO47RSB1
G15	IO49RSB1
G16	IO50RSB1
G17	GND
H1	VCOMPLF
H2	GFB0/IO137RSB3
H3	NC
H4	IO141RSB3
H5	IO143RSB3
H6	GFB1/IO138RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GCC1/IO52RSB1
H13	IO51RSB1
H14	GCA0/IO57RSB1
H15	VCCIB1
H16	GCA2/IO58RSB1
H17	GCC0/IO53RSB1
J1	VCCPLF
J2	GFA1/IO136RSB3
J3	VCCIB3
J4	IO131RSB3
J5	IO130RSB3
J6	IO129RSB3
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO59RSB1
J13	GCB1/IO54RSB1
J14	IO62RSB1
J15	IO63RSB1
J16	GCB0/IO55RSB1

CS289	
Pin Number	AGLP060 Function
J17	GCA1/IO56RSB1
K1	GND
K2	GFA0/IO135RSB3
K3	GFB2/IO133RSB3
K4	IO128RSB3
K5	IO123RSB3
K6	IO125RSB3
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO64RSB1
K13	IO61RSB1
K14	IO66RSB1
K15	IO65RSB1
K16	GND
K17	GCC2/IO60RSB1
L1	GFA2/IO134RSB3
L2	GFC2/IO132RSB3
L3	IO127RSB3
L4	GND
L5	IO121RSB3
L6	GEC1/IO116RSB3
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	GDC1/IO72RSB1
L13	GDB1/IO74RSB1
L14	VCCIB1
L15	IO70RSB1
L16	IO68RSB1
L17	IO67RSB1
M1	IO126RSB3
M2	VCCIB3
M3	IO124RSB3

CS289	
Pin Number	AGLP060 Function
M4	IO122RSB3
M5	GEB0/IO113RSB3
M6	GEB1/IO114RSB3
M7	NC
M8	NC
M9	IO90RSB2
M10	NC
M11	IO83RSB2
M12	NC
M13	GDA1/IO76RSB1
M14	GDA0/IO77RSB1
M15	IO71RSB1
M16	IO69RSB1
M17	VCCIB1
N1	IO119RSB3
N2	IO120RSB3
N3	GEC0/IO115RSB3
N4	GEA0/IO111RSB3
N5	GND
N6	NC
N7	IO104RSB2
N8	IO98RSB2
N9	IO96RSB2
N10	VCCIB2
N11	NC
N12	NC
N13	GDB2/IO79RSB2
N14	NC
N15	GND
N16	GDB0/IO75RSB1
N17	GDC0/IO73RSB1
P1	IO118RSB3
P2	IO117RSB3
P3	GND
P4	NC
P5	NC
P6	IO106RSB2
P7	IO99RSB2

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

Revision	Changes	Page
Revision 17 (December 2015)	Updated Commercial and Industrial temperature range to show junction temperature in "IGLOO PLUS Ordering Information" section and "Temperature Grade Offerings" section (SAR 73547).	1-III, 1-IV
	Removed Ambient temperature parameter in Table 2-2 • Recommended Operating Conditions[1,2] (SAR 73547).	2-2
	Table notes are added to Table 2-2 • Recommended Operating Conditions[1,2] stating that: • VMV pins must be connected to the corresponding VCCI pins. • Software default junction temperature range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial.	2-2
	Updated Table 2-5 • Package Thermal Resistivities (SAR 60078).	2-6
	Added 2 mA drive strength information in the following tables (SAR 57182): • Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage • Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage • Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage • Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-28, 2-28, 2-28, 2-29
	Fixed typo for "VQ128" section in "Package Pin Assignments" section	4-1
Revision 16 (December 2012)	The "IGLOO PLUS Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43175).	III
	The note in Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42566).	2-61, 2-62
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 15 (October 2012)	Values updated for IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage in Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices and for IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage in Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices (SAR 31988). Also added a new Note to the two tables.	2-10, 2-11
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40277).	N/A
Revision 14 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2

Revision	Changes	Page
Revision 11 (continued)	Table 2-2 • Recommended Operating Conditions[1,2] was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were revised.	2-6, 2-6
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
	VIH maximum values in tables were updated as needed to 3.6 V (SARs 20990, 79370).	N/A
	The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable. Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Table 2-22 • Summary of Maximum and Minimum DC Input Levels Table 2-23 • Summary of AC Measuring Points Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-28 • I/O Output Buffer Maximum Resistances [1]	2-9 2-9 2-19 2-20 2-20 2-22 2-23 2-24
	A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.	2-10, 2-11
	Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining $R_{WEAK\ PULL\text{-}UP\text{-}MAX}$ and $R_{WEAK\ PULLDOWN\text{-}MAX}$ were revised (SAR 21348).	2-25
	Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).	2-25
	Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).	2-26

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3