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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1584
Total RAM Bits	18432
Number of I/O	137
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	176-TQFP
Supplier Device Package	176-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp060v5-vq176i

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

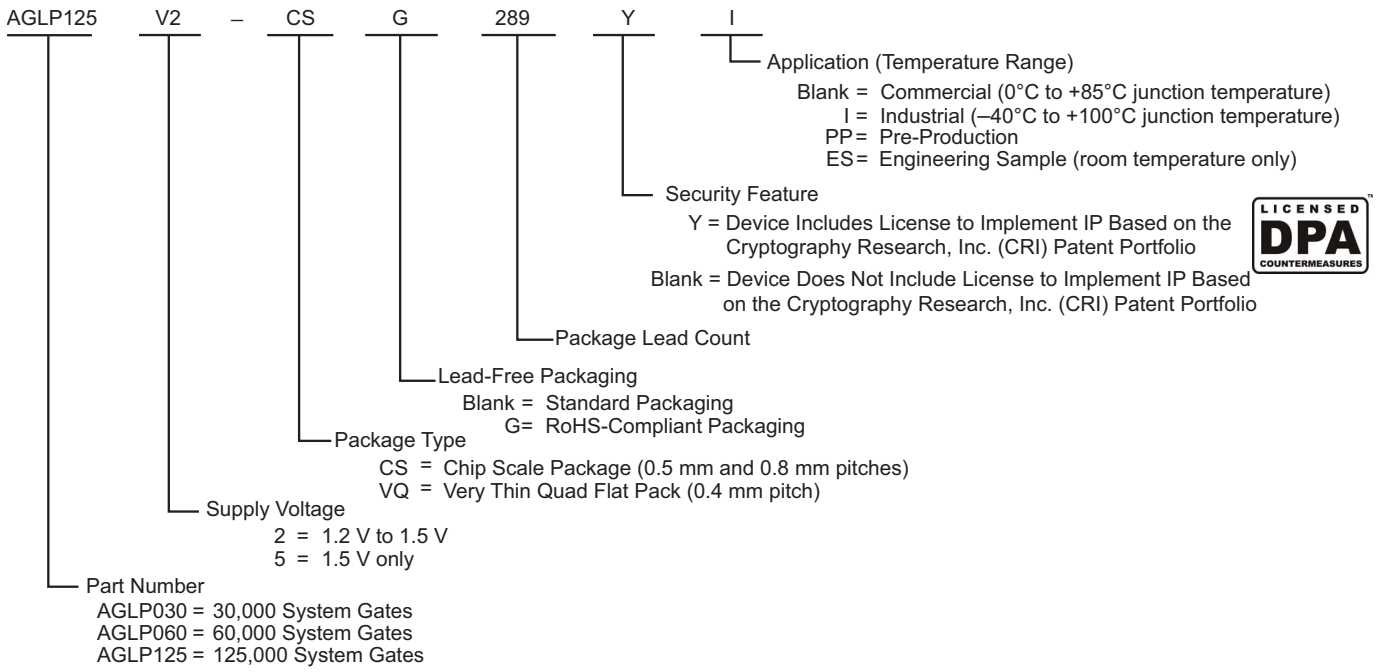
Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

IGLOO PLUS Ordering Information



1. *Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.*
2. *"G" indicates RoHS-compliant packages.*

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode***

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	µA
	1.5 V	6	10	18	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode***

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	µA

*Note: *IDD = N_{BANKS} * ICCI*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	µA

Power per I/O Pin

***Table 2-13* • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range[2]	3.3	16.26
3.3 V LVCMOS Wide Range[2] – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS[3]	1.2	0.55
1.2 V LVCMOS[3] – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range[3]	1.2	0.55
1.2 V LVCMOS Wide Range[3] – Schmitt Trigger	1.2	0.47

Notes:

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

***Table 2-14* • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range[3]	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS[4]	5	1.2	15.22
1.2 V LVCMOS Wide Range[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

Power Consumption of Various Internal Resources

***Table 2-15* • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	4.489	2.696	0.000[1]
PAC2	Clock contribution of a Global Spine	1.991	1.962	3.499
PAC3	Clock contribution of a VersaTile row	1.510	1.523	1.537
PAC4	Clock contribution of a VersaTile used as a sequential module	0.153	0.151	0.151
PAC5	First contribution of a VersaTile used as a sequential module	0.029	0.029	0.029
PAC6	Second contribution of a VersaTile used as a sequential module	0.323	0.323	0.323
PAC7	Contribution of a VersaTile used as a combinatorial module	0.280	0.300	0.278
PAC8	Average contribution of a routing net	1.097	1.081	1.130
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9.		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.70		

Note: 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

***Table 2-16* • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	1.84[1]		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. *This is the minimum contribution of the PLL when operating at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC software.*

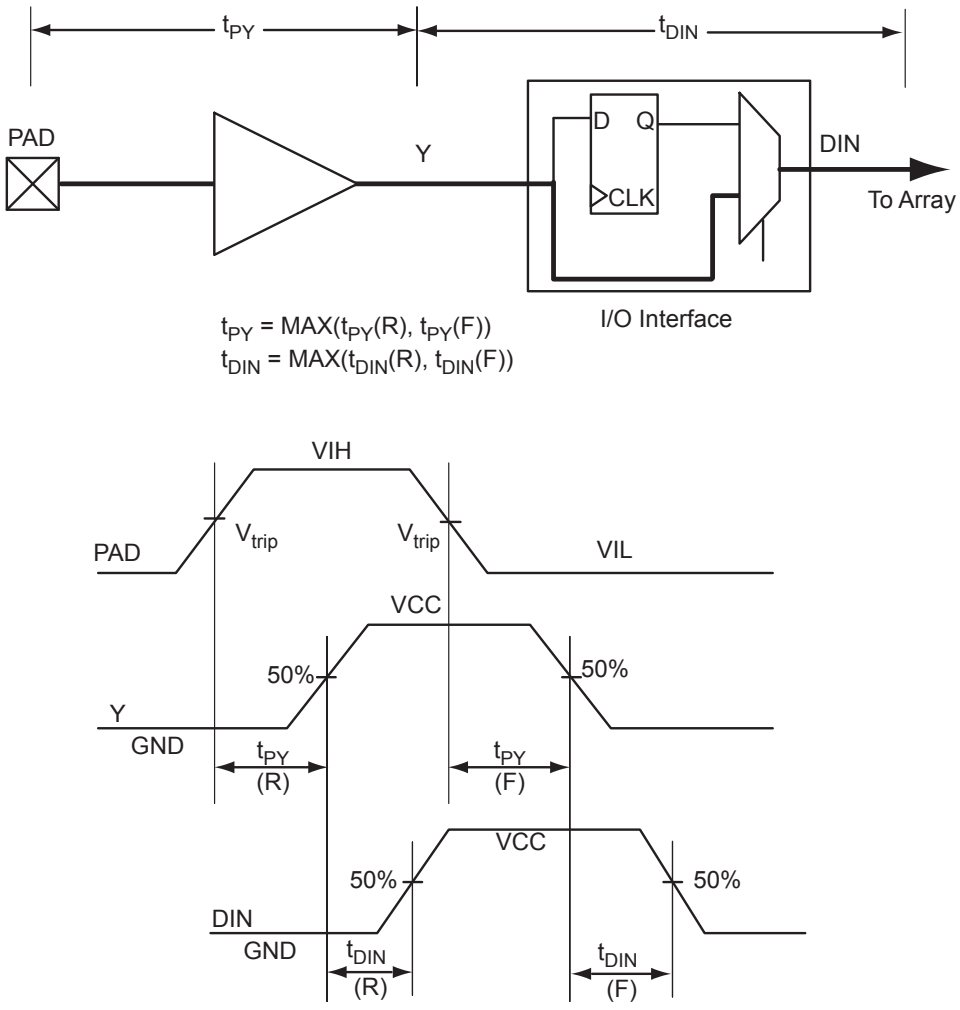


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.97	1.76	0.18	0.85	1.15	0.66	1.80	1.39	2.20	2.64	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	5 pF	–	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.97	1.77	0.18	1.06	1.22	0.66	1.81	1.51	2.22	2.56	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.97	2.29	0.18	1.16	1.62	0.66	2.33	2.00	2.37	2.57	ns

Notes:

1. *Note that 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-64 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

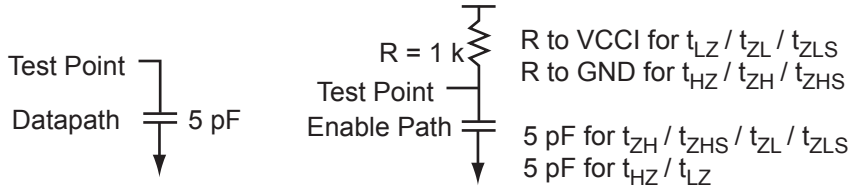


Figure 2-11 • AC Loading

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-66 • 1.2 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-67 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Output Register

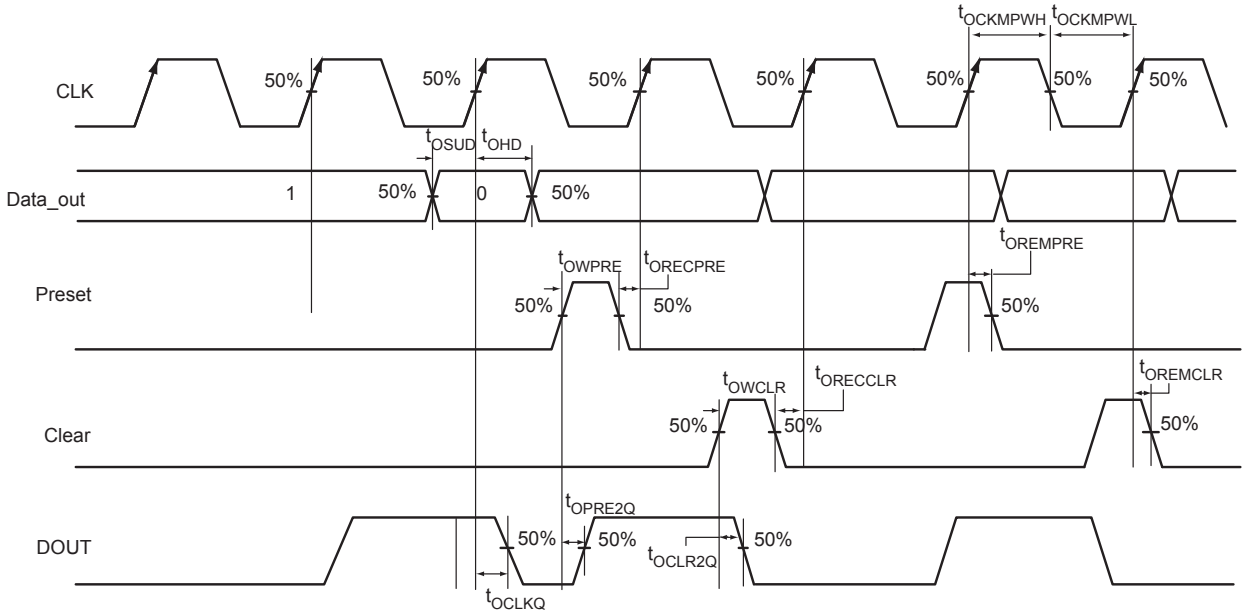


Figure 2-15 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-61. Table 2-84 to Table 2-89 on page 2-60 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-84* • AGLP030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-85* • AGLP060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.72	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-88 • AGLP060 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.43	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

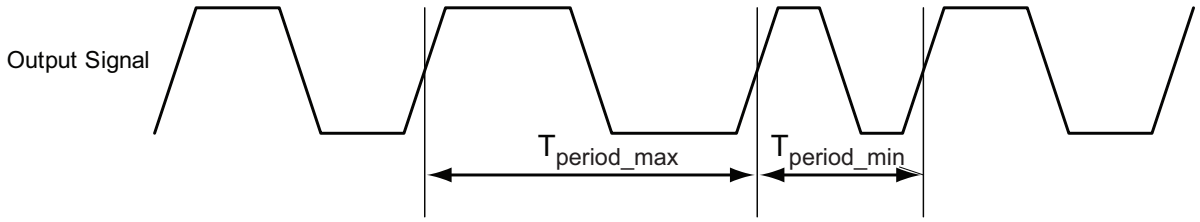
1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-89 • AGLP125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-22 • **Peak-to-Peak Jitter Definition**

Embedded FlashROM Characteristics

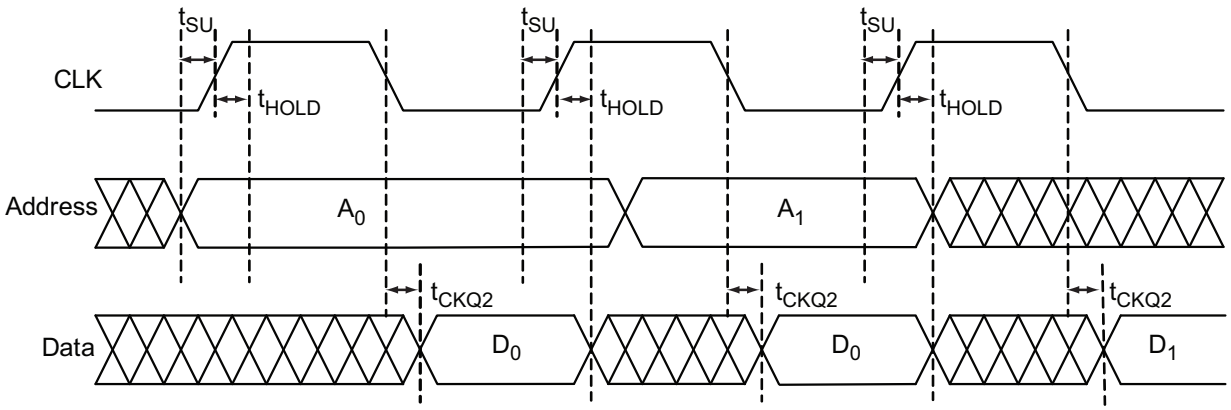


Figure 2-37 • **Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

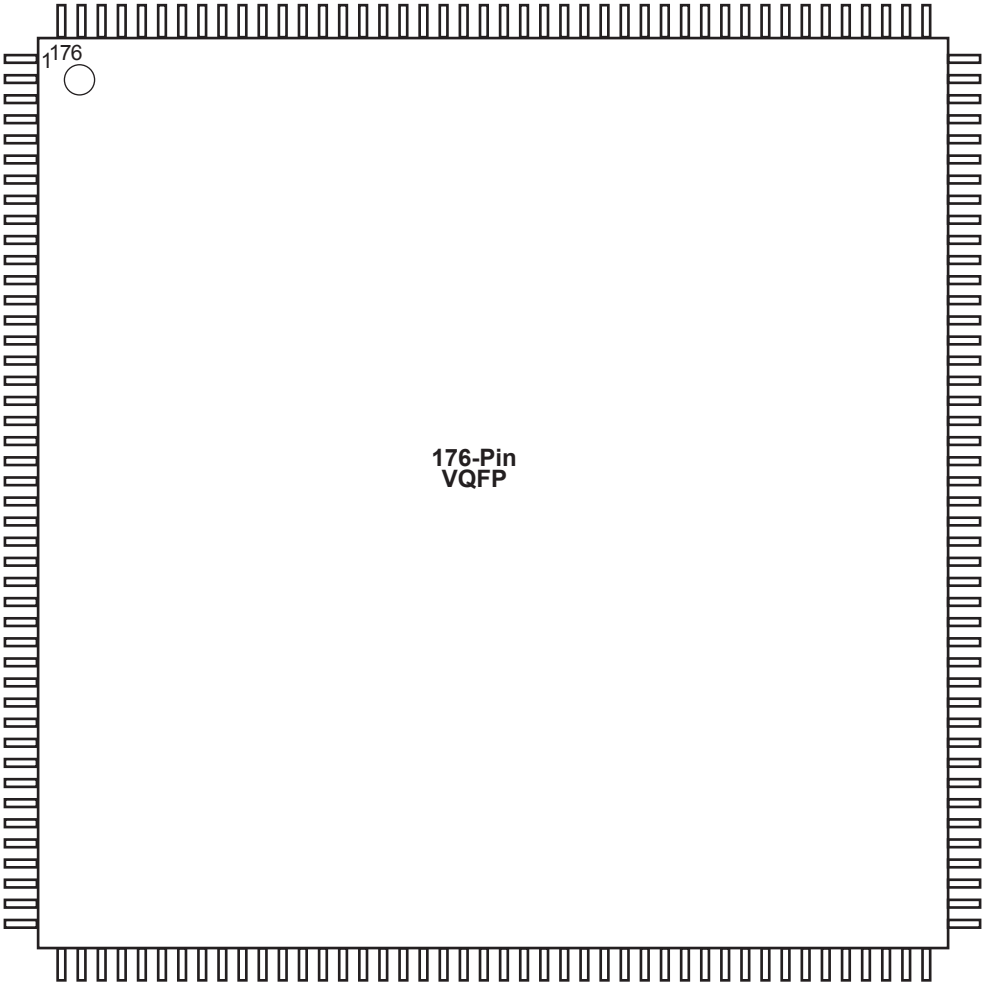
Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	17.58	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-99 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	30.94	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

VQ176



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS281	
Pin Number	AGLP125 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO77RSB1
H16	GCB0/IO82RSB1
H18	GCA1/IO83RSB1
H19	GCA2/IO85RSB1
J1	VCOMPLF
J2	GFA0/IO189RSB3
J4	VCCPLF
J5	GFC0/IO193RSB3
J7	GFA2/IO188RSB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO79RSB1
J15	GCA0/IO84RSB1
J16	GCB2/IO86RSB1
J18	IO76RSB1
J19	IO78RSB1
K1	VCCIB3
K2	GFA1/IO190RSB3
K4	GND
K5	IO19RSB0
K7	IO197RSB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO87RSB1

CS281	
Pin Number	AGLP125 Function
K15	IO89RSB1
K16	GND
K18	IO88RSB1
K19	VCCIB1
L1	GFB2/IO187RSB3
L2	IO185RSB3
L4	GFC2/IO186RSB3
L5	IO184RSB3
L7	IO199RSB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO95RSB1
L15	IO91RSB1
L16	NC
L18	IO90RSB1
L19	NC
M1	IO180RSB3
M2	IO179RSB3
M4	IO181RSB3
M5	IO183RSB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO122RSB2
M16	IO93RSB1
M18	IO92RSB1
M19	NC
N1	IO178RSB3
N2	IO175RSB3

CS281	
Pin Number	AGLP125 Function
N4	IO182RSB3
N5	IO161RSB2
N7	GEA2/IO164RSB2
N8	VCCIB2
N9	IO137RSB2
N10	IO135RSB2
N11	IO131RSB2
N12	VCCIB2
N13	VPUMP
N15	IO117RSB2
N16	IO96RSB1
N18	IO98RSB1
N19	IO94RSB1
P1	IO174RSB3
P2	GND
P3	IO176RSB3
P4	IO177RSB3
P5	GEA0/IO165RSB3
P15	IO111RSB2
P16	IO108RSB2
P17	GDC1/IO99RSB1
P18	GND
P19	IO97RSB1
R1	IO173RSB3
R2	IO172RSB3
R4	GEC1/IO170RSB3
R5	GEB1/IO168RSB3
R6	IO154RSB2
R7	IO149RSB2
R8	IO146RSB2
R9	IO138RSB2
R10	IO134RSB2
R11	IO132RSB2
R12	IO130RSB2
R13	IO118RSB2
R14	IO112RSB2

CS289	
Pin Number	AGLP030 Function
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0

CS289	
Pin Number	AGLP030 Function
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC

CS289	
Pin Number	AGLP030 Function
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

CS289	
Pin Number	**AGLP060 Function**
P8	GND
P9	IO91RSB2
P10	IO86RSB2
P11	IO81RSB2
P12	NC
P13	VCCIB2
P14	NC
P15	GDA2/IO78RSB2
P16	GDC2/IO80RSB2
P17	VJTAG
R1	GND
R2	GEA2/IO110RSB2
R3	NC
R4	NC
R5	NC
R6	VCCIB2
R7	IO102RSB2
R8	IO97RSB2
R9	IO93RSB2
R10	IO89RSB2
R11	GND
R12	NC
R13	NC
R14	NC
R15	NC
R16	TMS
R17	TRST
T1	GEA1/IO112RSB3
T2	GEC2/IO108RSB2
T3	NC
T4	GND
T5	NC
T6	IO103RSB2
T7	IO100RSB2
T8	IO95RSB2
T9	VCCIB2
T10	IO88RSB2
T11	IO84RSB2

CS289	
Pin Number	**AGLP060 Function**
T12	IO82RSB2
T13	NC
T14	GND
T15	NC
T16	TDI
T17	TDO
U1	FF/GEB2/IO109RSB2
U2	GND
U3	NC
U4	IO107RSB2
U5	IO105RSB2
U6	IO101RSB2
U7	GND
U8	IO94RSB2
U9	IO92RSB2
U10	IO87RSB2
U11	IO85RSB2
U12	GND
U13	NC
U14	NC
U15	NC
U16	TCK
U17	VPUMP

Revision	Changes	Page
Revision 13 (June 2012)	Figure 2-30 • FIFO Read and Figure 2-31 • FIFO Write have been added (SAR 34843).	2-73
	Updated the terminology used in Timing Characteristics in the following tables: Table 2-96 • FIFO and Table 2-97 • FIFO (SAR 38236).	2-76
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38320). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1
Revision 12 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34664).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOO PLUS Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34724).	III
	The "Specifying I/O States During Programming" section is new (SAR 34695).	1-7
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface" (SAR 34684).	1-3

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3

Revision	Changes	Page
Revision 3 (continued)	The table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode* to remove the sentence stating that values do not include I/O static contribution.	2-7
	The table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode* was updated to remove VJTAG and VCCI and the statement that values do not include I/O static contribution.	2-7
	The table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode was updated to remove the statement that values do not include I/O static contribution.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash*Freeze Mode 1 was updated to include VCCPLL. Table note 4 was deleted.	2-8
	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] were updated to remove static power. The table notes were updated to reflect that power was measured on VCC_I. Table note 2 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings.	2-9, 2-9
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices were updated to change the definition for P_{DC5} from bank static power to bank quiescent power. Table subtitles were added for Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices, Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices, and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices.	2-10, 2-11
	The "Total Static Power Consumption—P_{STAT}" section was revised.	2-12
	Table 2-32 • Schmitt Trigger Input Hysteresis is new.	2-26
Packaging v1.3	The "CS281" package drawing is new.	4-13
	The "CS281" table for the AGLP125 device is new.	4-13
Revision 3 (continued)	The "CS289" package drawing was incorrect. The graphic was showing the CS281 mechanical drawing and not the CS289 mechanical drawing. This has now been corrected.	4-17
Revision 2 (Jun 2008) Packaging v1.2	The "CS289" table for the AGLP030 device is new.	4-17
Revision 1 (Jun 2008) Packaging v1.1	The "CS289" table for the AGLP060 device is new.	4-20
	The "CS289" table for the AGLP125 device is new.	4-23