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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

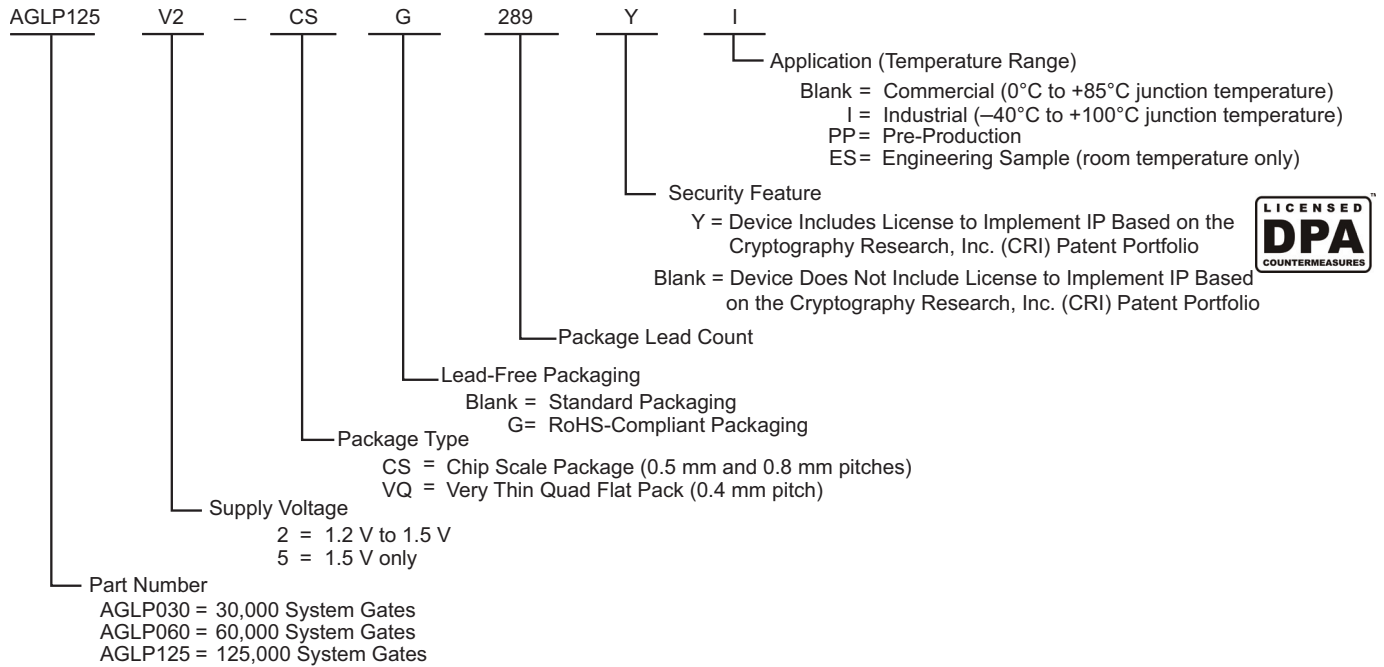
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3120
Total RAM Bits	36864
Number of I/O	212
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp125v2-cs281

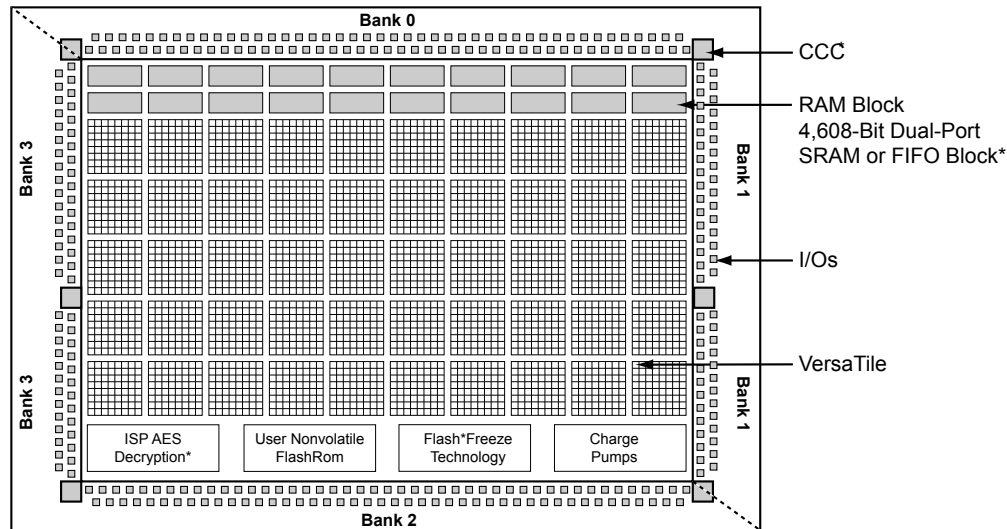
IGLOO PLUS Ordering Information



1. Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.
2. "G" indicates RoHS-compliant packages.

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Note: *Not supported by AGLP030 devices

Figure 1-1 • IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)

Flash*Freeze Technology

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 μ W in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to [Figure 1-2](#) for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

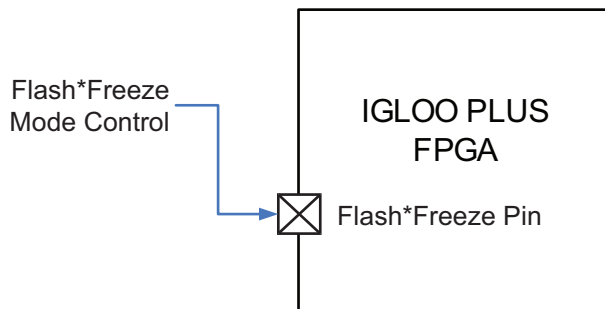


Figure 1-2 • IGLOO PLUS Flash*Freeze Mode

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^{\circ}\text{C)} - \text{Max. ambient temp. (}^{\circ}\text{C)}}{\theta_{ja} (^{\circ}\text{C/W)}} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{20.5^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{jb}	θ_{ja}			Unit
					Still Air	1 m/s	2.5 m/s	
Chip Scale Package (CSP)	AGLP030	CS201	-	-	46.3	-	-	C/W
	AGLP060	CS201	7.1	19.7	40.5	35.1	32.9	C/W
	AGLP060	CS289	13.9	34.1	48.7	43.5	41.9	C/W
	AGLP125	CS289	10.8	27.9	42.2	37.1	35.5	C/W
	AGLP125	CS281	11.3	17.6	-	-	-	C/W
Thin Quad Flat Package (VQ)	AGLP030	VQ128	18.0	50.0	56.0	49.0	47.0	C/W
	AGLP060	VQ176	21.0	55.0	58.0	52.0	50.0	C/W

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425 \text{ V}$)
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^{\circ}\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.5	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.14 \text{ V}$)
For IGLOO PLUS V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^{\circ}\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.963	0.975	0.989	1.000	1.007	1.011
1.2	0.853	0.865	0.877	0.893	0.893	0.897
1.26	0.781	0.792	0.803	0.813	0.819	0.822

Power Consumption of Various Internal Resources

Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	4.489	2.696	0.000 ¹
PAC2	Clock contribution of a Global Spine	1.991	1.962	3.499
PAC3	Clock contribution of a VersaTile row	1.510	1.523	1.537
PAC4	Clock contribution of a VersaTile used as a sequential module	0.153	0.151	0.151
PAC5	First contribution of a VersaTile used as a sequential module	0.029	0.029	0.029
PAC6	Second contribution of a VersaTile used as a sequential module	0.323	0.323	0.323
PAC7	Contribution of a VersaTile used as a combinatorial module	0.280	0.300	0.278
PAC8	Average contribution of a routing net	1.097	1.081	1.130
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9.		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.70		

Note: 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0μW/MHz.

Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	1.84 ¹		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. This is the minimum contribution of the PLL when operating at lowest frequency.
2. For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC software.

Applies to 1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	6.68	0.19	1.32	1.92	0.67	6.68	5.74	3.13	3.47	ns
100 μA	6 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	8 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	12 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns
100 μA	16 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	4.16	0.19	1.32	1.92	0.67	4.16	3.32	3.12	3.66	ns
100 μA	6 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	8 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	12 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
100 μA	16 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	−0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

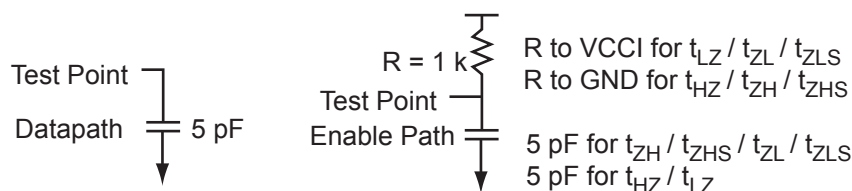


Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = V_{trip}. See [Table 2-23 on page 2-20](#) for a complete table of trip points.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ³	Max., mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	8	8	35	44	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

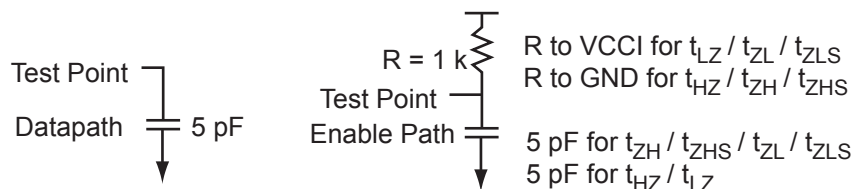


Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

Input Register

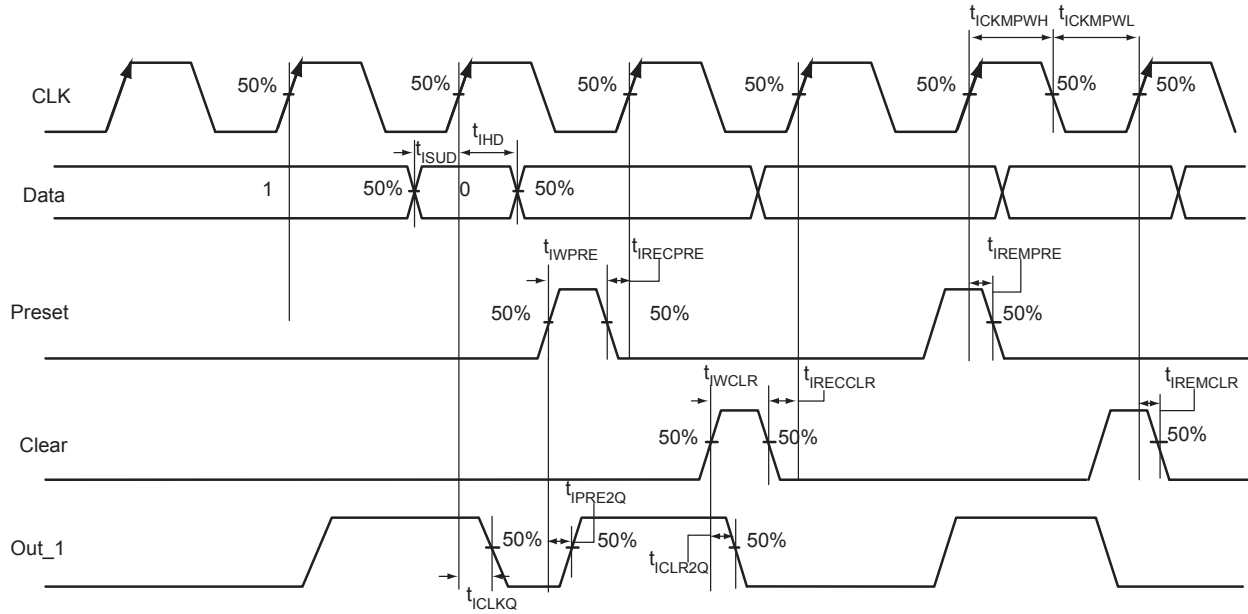


Figure 2-14 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.41	ns
t_{SUD}	Data Setup Time for the Input Data Register	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-79 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.06	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.52	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.25	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.36	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	0.72	ns
AND2	$Y = A \cdot B$	t_{PD}	0.86	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.00	ns
OR2	$Y = A + B$	t_{PD}	1.26	ns
NOR2	$Y = !(A + B)$	t_{PD}	1.16	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	1.47	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	2.12	ns
MUX2	$Y = A !S + B S$	t_{PD}	1.24	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-81 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	1.26	ns
AND2	$Y = A \cdot B$	t_{PD}	1.46	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.78	ns
OR2	$Y = A + B$	t_{PD}	2.47	ns
NOR2	$Y = !(A + B)$	t_{PD}	2.17	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.62	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	2.66	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.77	ns
MUX2	$Y = A !S + B S$	t_{PD}	2.20	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion](#), [IGLOO/e](#), and [ProASIC3/E Macro Library Guide](#).

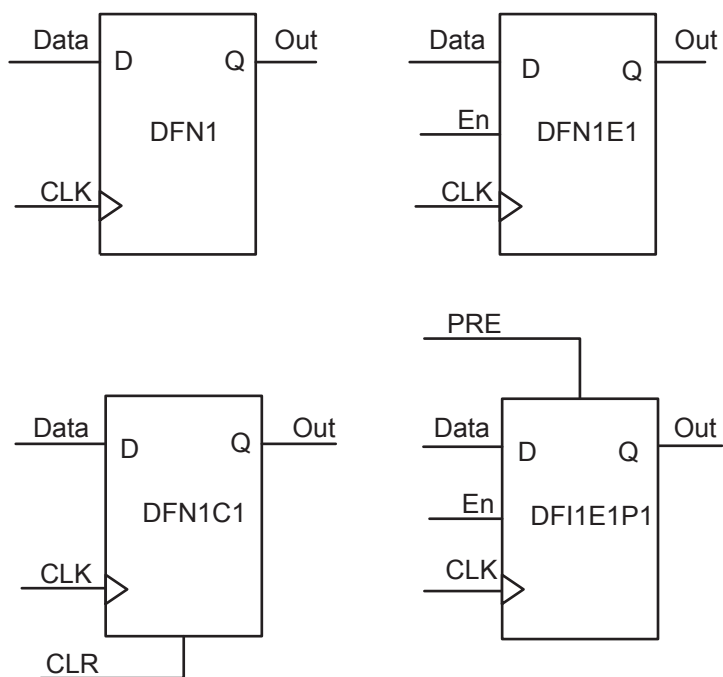


Figure 2-19 • Sample of Sequential Cells

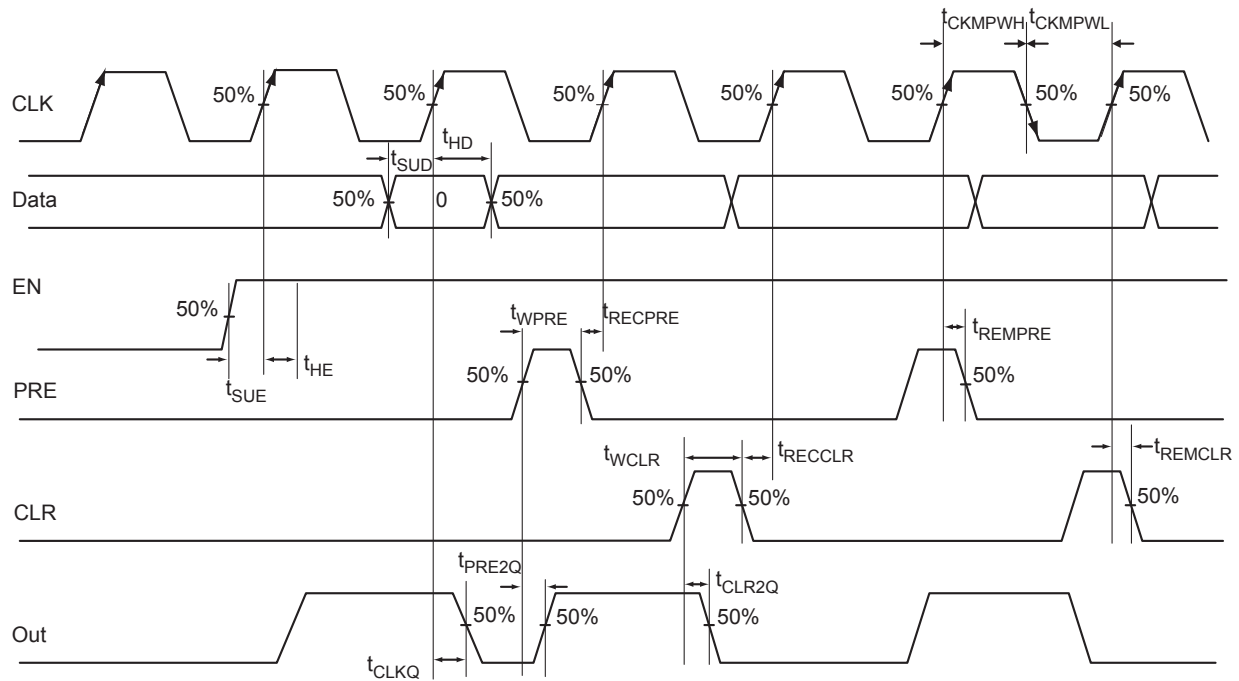


Figure 2-20 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • Register Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Embedded FlashROM Characteristics

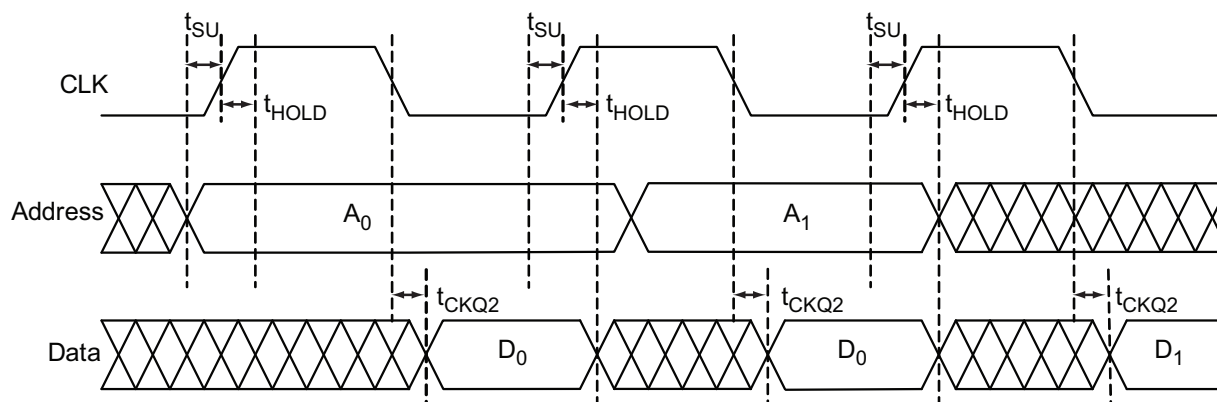


Figure 2-37 • Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	17.58	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-99 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	30.94	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

3 – Pin Descriptions and Packaging

Supply Pins

GND**Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ**Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC**Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO PLUS V5 devices, and 1.2 V or 1.5 V for IGLOO PLUS V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO PLUS V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx**I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are four I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx**I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F**PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOO PLUS V5 devices
- 1.2 V or 1.5 V for IGLOO PLUS V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed signal FPGAs" chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on IGLOO PLUS devices.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to [Table 3-2](#) for more information.

Table 3-2 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

1. Equivalent parallel resistance if more than one device is on the JTAG chain
2. The TCK pin can be pulled up/down.
3. The TRST pin is pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

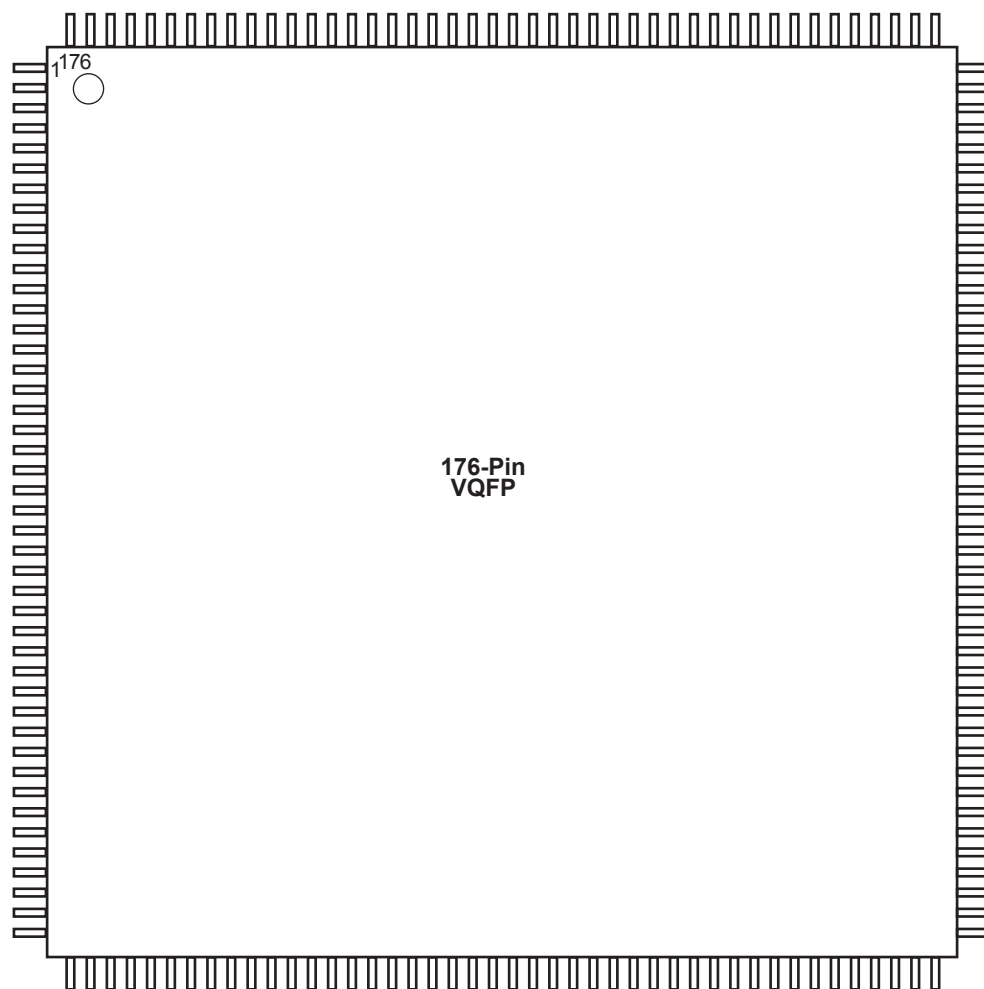
TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from [Table 3-2](#) and must satisfy the parallel resistance value requirement. The values in [Table 3-2](#) correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

VQ176



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

VQ176	
Pin Number	AGLP060 Function
105	IO62RSB1
106	IO61RSB1
107	GCC2/IO60RSB1
108	GCB2/IO59RSB1
109	GCA2/IO58RSB1
110	GCA0/IO57RSB1
111	GCA1/IO56RSB1
112	VCCIB1
113	GND
114	GCB0/IO55RSB1
115	GCB1/IO54RSB1
116	GCC0/IO53RSB1
117	GCC1/IO52RSB1
118	IO51RSB1
119	IO50RSB1
120	VCC
121	IO48RSB1
122	IO47RSB1
123	IO45RSB1
124	IO44RSB1
125	IO43RSB1
126	VCCIB1
127	GND
128	GBC2/IO40RSB1
129	IO39RSB1
130	GBB2/IO38RSB1
131	IO37RSB1
132	GBA2/IO36RSB1
133	GBA1/IO35RSB0
134	NC
135	GBA0/IO34RSB0
136	NC
137	GBB1/IO33RSB0
138	NC
139	GBC1/IO31RSB0

VQ176	
Pin Number	AGLP060 Function
140	GBB0/IO32RSB0
141	GBC0/IO30RSB0
142	IO29RSB0
143	IO28RSB0
144	IO27RSB0
145	VCCIB0
146	GND
147	IO26RSB0
148	IO25RSB0
149	IO24RSB0
150	IO23RSB0
151	IO22RSB0
152	IO21RSB0
153	IO20RSB0
154	IO19RSB0
155	IO18RSB0
156	VCC
157	IO17RSB0
158	IO16RSB0
159	IO15RSB0
160	IO14RSB0
161	IO13RSB0
162	IO12RSB0
163	IO11RSB0
164	IO10RSB0
165	IO09RSB0
166	VCCIB0
167	GND
168	IO07RSB0
169	IO08RSB0
170	GAC1/IO05RSB0
171	IO06RSB0
172	GAB1/IO03RSB0
173	GAC0/IO04RSB0
174	GAB0/IO02RSB0

VQ176	
Pin Number	AGLP060 Function
175	GAA1/IO01RSB0
176	GAA0/IO00RSB0

CS201		CS201		CS201	
Pin Number	AGLP030 Function	Pin Number	AGLP030 Function	Pin Number	AGLP030 Function
A1	NC	C6	IO12RSB0	F3	IO119RSB3
A2	IO04RSB0	C7	IO23RSB0	F4	IO111RSB3
A3	IO06RSB0	C8	IO19RSB0	F6	GND
A4	IO09RSB0	C9	IO28RSB0	F7	VCC
A5	IO11RSB0	C10	IO32RSB0	F8	VCCIB0
A6	IO13RSB0	C11	IO35RSB0	F9	VCCIB0
A7	IO17RSB0	C12	NC	F10	VCCIB0
A8	IO18RSB0	C13	GND	F12	NC
A9	IO24RSB0	C14	IO41RSB1	F13	NC
A10	IO26RSB0	C15	IO37RSB1	F14	IO40RSB1
A11	IO27RSB0	D1	IO117RSB3	F15	IO38RSB1
A12	IO31RSB0	D2	IO118RSB3	G1	NC
A13	NC	D3	NC	G2	IO112RSB3
A14	NC	D4	GND	G3	IO110RSB3
A15	NC	D5	IO01RSB0	G4	IO109RSB3
B1	NC	D6	IO03RSB0	G6	VCCIB3
B2	NC	D7	IO10RSB0	G7	GND
B3	IO08RSB0	D8	IO21RSB0	G8	VCC
B4	IO05RSB0	D9	IO25RSB0	G9	GND
B5	IO07RSB0	D10	IO30RSB0	G10	GND
B6	IO15RSB0	D11	IO33RSB0	G12	NC
B7	IO14RSB0	D12	GND	G13	NC
B8	IO16RSB0	D13	NC	G14	IO42RSB1
B9	IO20RSB0	D14	IO36RSB1	G15	IO44RSB1
B10	IO22RSB0	D15	IO39RSB1	H1	NC
B11	IO34RSB0	E1	IO115RSB3	H2	GEB0/IO106RSB3
B12	IO29RSB0	E2	IO114RSB3	H3	GEC0/IO108RSB3
B13	NC	E3	NC	H4	NC
B14	NC	E4	NC	H6	VCCIB3
B15	NC	E12	NC	H7	GND
C1	NC	E13	NC	H8	VCC
C2	NC	E14	GDC0/IO46RSB1	H9	GND
C3	GND	E15	GDB0/IO48RSB1	H10	VCCIB1
C4	IO00RSB0	F1	IO113RSB3	H12	IO54RSB1
C5	IO02RSB0	F2	IO116RSB3	H13	GDA0/IO47RSB1

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm ² .	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T _J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T _J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2 Packaging v1.4	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions ^{1,2} to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits ¹ was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3