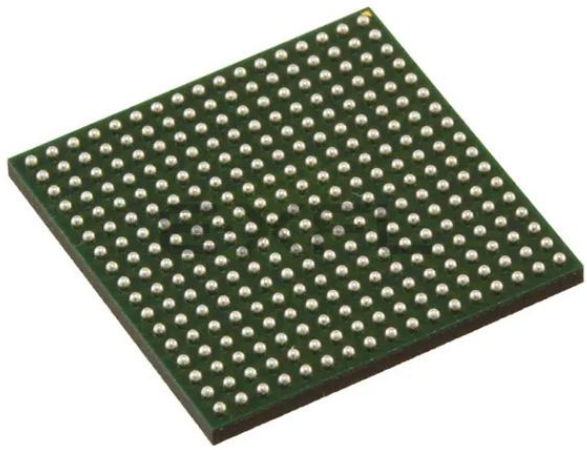

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3120
Total RAM Bits	36864
Number of I/O	212
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp125v2-cs289i

1 – IGLOO PLUS Device Family Overview

General Description

The IGLOO PLUS family of flash FPGAs, based on a 130 nm flash process, offers the lowest power FPGA, a single-chip solution, small-footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO PLUS devices enables entering and exiting an ultra-low power mode that consumes as little as 5 µW while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO PLUS device is completely functional in the system. This allows the IGLOO PLUS device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO PLUS devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOO PLUS is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO PLUS devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). IGLOO PLUS devices have up to 125 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 212 user I/Os. The AGLP030 devices have no PLL or RAM support.

Flash*Freeze Technology

The IGLOO PLUS device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO PLUS devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO PLUS V2 devices to support a wide range of core and I/O voltages (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, or set as HIGH or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high-pin-count packages, make IGLOO PLUS devices the best fit for portable electronics.

Flash Advantages

Low Power

IGLOO PLUS devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO PLUS devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO PLUS devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO PLUS device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO PLUS device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2 V or 1.5 V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

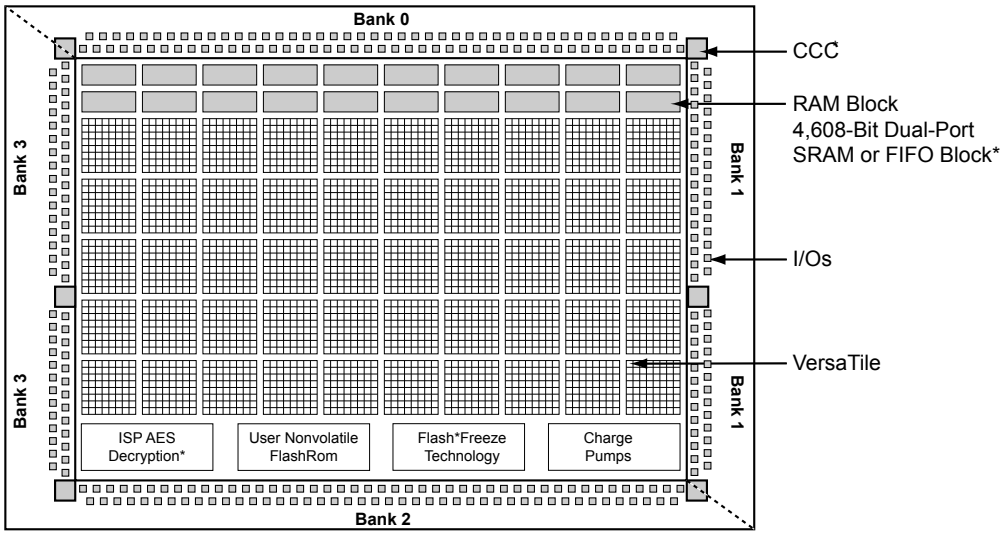
Instant On

Flash-based IGLOO PLUS devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm.



*Note: *Not supported by AGLP030 devices*

Figure 1-1 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

*Flash*Freeze Technology*

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

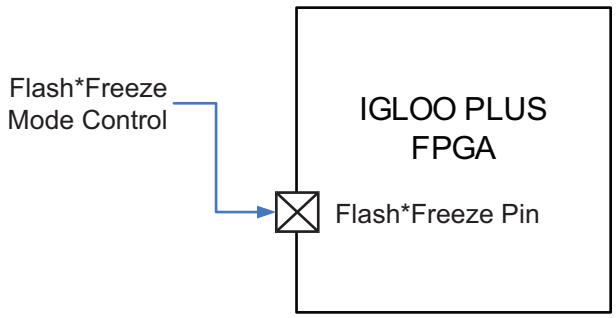


Figure 1-2 • **IGLOO PLUS Flash*Freeze Mode**

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-14.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-14.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC1_3 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

User I/O Characteristics

Timing Model

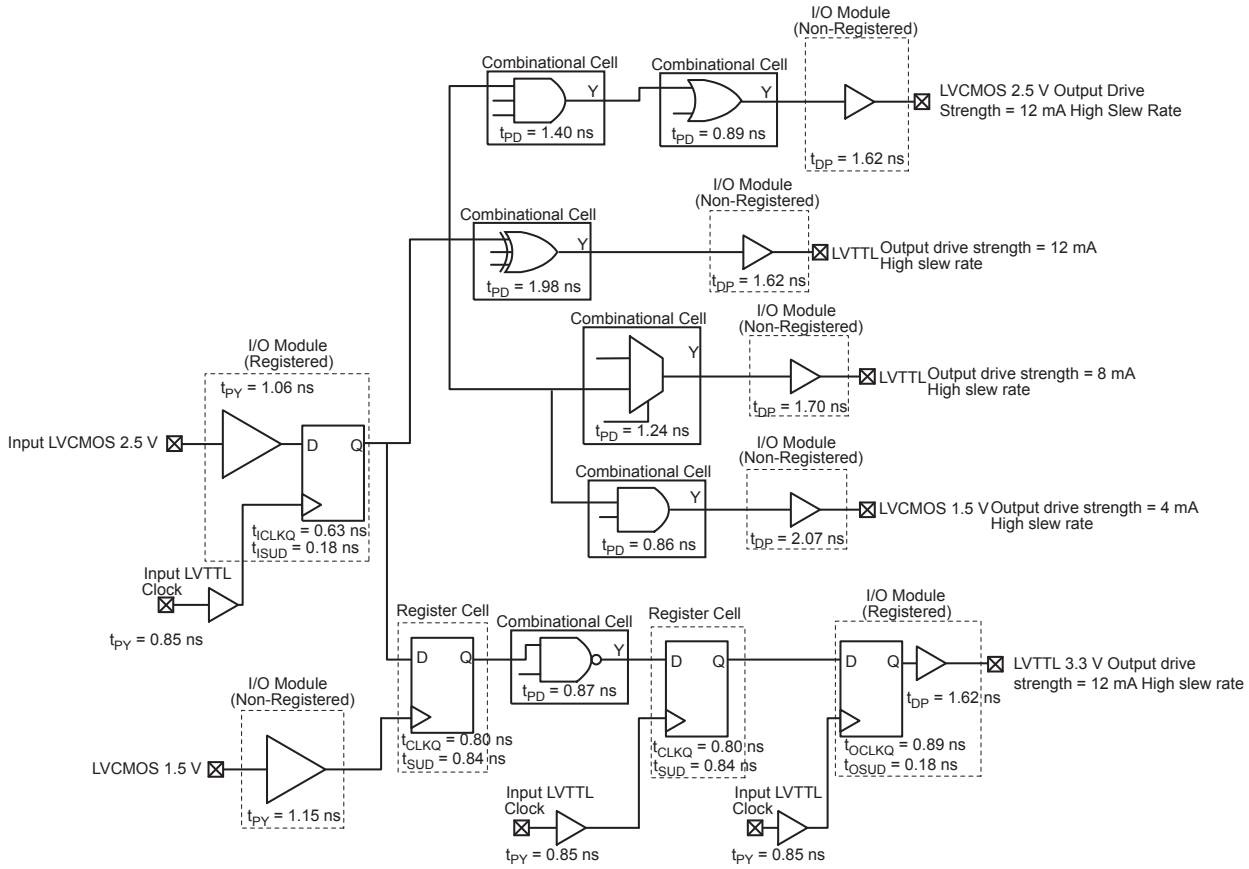


Figure 2-3 • **Timing Model**
Operating Conditions: STD Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY})	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	5 pF	–	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.29	0.19	1.19	1.40	0.67	2.32	1.94	2.65	3.27	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns
1.2 V LVCMOS	2 mA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns
1.2 V LVCMOS Wide Range[3]	100 µA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	**IOSL (mA)***	**IOSH (mA)***
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 µA	26	20

*Note: *T_J = 100°C*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[3]	Max., mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	35	44	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

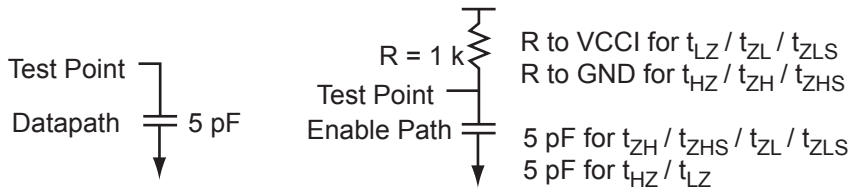


Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.89	0.18	1.00	1.43	0.66	6.01	5.43	1.78	1.30	ns
4 mA	STD	0.97	4.82	0.18	1.00	1.43	0.66	4.92	4.56	2.08	2.08	ns
6 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns
8 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.82	0.18	1.00	1.43	0.66	2.88	2.78	1.78	1.35	ns
4 mA	STD	0.97	2.30	0.18	1.00	1.43	0.66	2.35	2.11	2.08	2.15	ns
6 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
8 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.43	0.19	1.12	1.61	0.67	6.54	5.93	2.19	1.88	ns
4 mA	STD	0.98	5.33	0.19	1.12	1.61	0.67	5.41	5.03	2.50	2.68	ns
6 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns
8 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.30	0.19	1.12	1.61	0.67	3.34	3.21	2.19	1.93	ns
4 mA	STD	0.98	2.76	0.19	1.12	1.61	0.67	2.79	2.51	2.50	2.76	ns
6 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
8 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[3]	IIH[4]
Drive Strength	Equivalent Software Default Drive Strength Option[2]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[5]	Max mA[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to V2 devices only.*
2. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

1.2 V DC Core Voltage

Table 2-79 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.06	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.52	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.25	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.36	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-93 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.61	ns
t_{ENH}	REN, WEN hold time	0.07	ns
t_{DS}	Input data (WD) setup time	0.59	ns
t_{DH}	Input data (WD) hold time	0.30	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	3.51	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.43	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.21	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.25	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.72	ns
	RESET Low to data out Low on RD (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

***Table 2-97* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.30	ns
t_{DH}	Input Data (WD) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	3.41	ns
	RESET Low to Data Out Low on RD (pipelined)	3.41	ns
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-100* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-101* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO PLUS devices.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOO PLUS devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

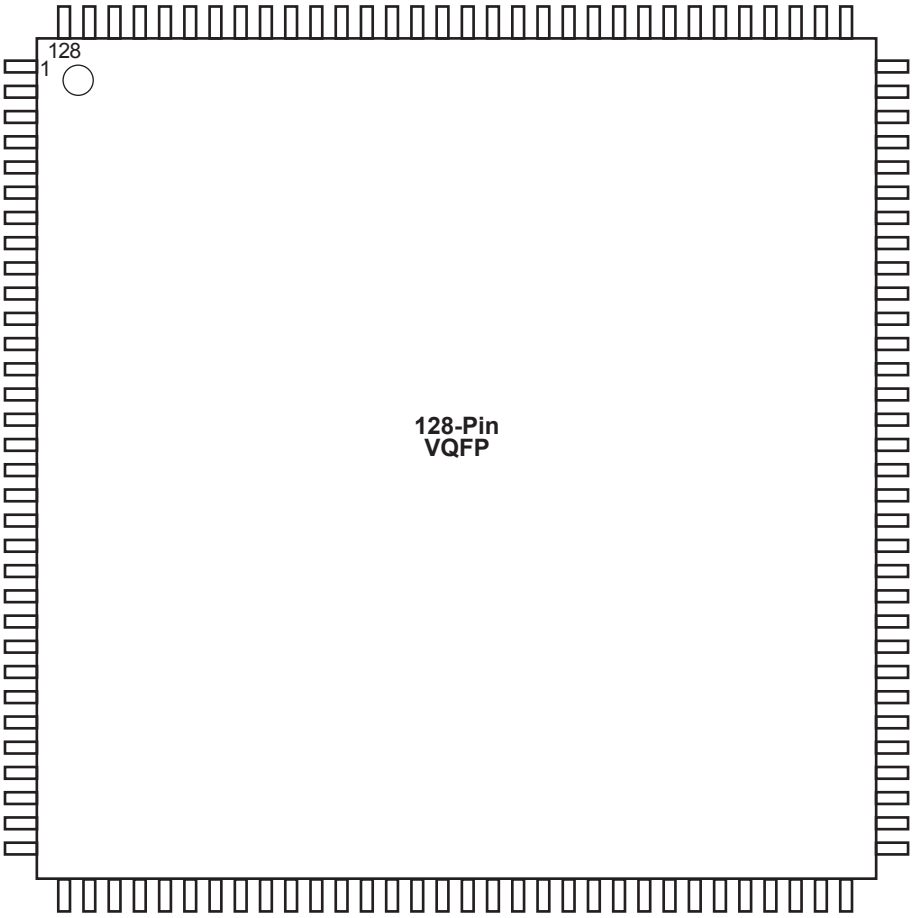
GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for an explanation of the naming of global pins.

4 – Package Pin Assignments

VQ128



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

CS281	
Pin Number	AGLP125 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO23RSB0
A9	IO25RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO41RSB0
A13	IO43RSB0
A14	IO46RSB0
A15	IO55RSB0
A16	IO56RSB0
A17	GBC1/IO58RSB0
A18	GBA0/IO61RSB0
A19	GND
B1	GAA2/IO211RSB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO11RSB0
B6	GND
B7	IO21RSB0
B8	IO22RSB0
B9	IO28RSB0
B10	IO32RSB0
B11	IO36RSB0
B12	IO39RSB0
B13	IO42RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO57RSB0
B17	GBA1/IO62RSB0

CS281	
Pin Number	AGLP125 Function
B18	VCCIB1
B19	IO64RSB1
C1	GAB2/IO209RSB3
C2	IO210RSB3
C6	IO12RSB0
C14	IO47RSB0
C18	IO54RSB0
C19	GBB2/IO65RSB1
D1	IO206RSB3
D2	IO208RSB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO10RSB0
D7	IO17RSB0
D8	IO24RSB0
D9	IO27RSB0
D10	GND
D11	IO31RSB0
D12	IO40RSB0
D13	IO49RSB0
D14	IO45RSB0
D15	GBB0/IO59RSB0
D16	GBA2/IO63RSB1
D18	GBC2/IO67RSB1
D19	IO66RSB1
E1	IO203RSB3
E2	IO205RSB3
E4	IO07RSB0
E5	IO06RSB0
E6	IO14RSB0
E7	IO20RSB0
E8	IO29RSB0
E9	IO34RSB0
E10	IO30RSB0
E11	IO37RSB0
E12	IO38RSB0

CS281	
Pin Number	AGLP125 Function
E13	IO48RSB0
E14	GBB1/IO60RSB0
E15	IO53RSB0
E16	IO69RSB1
E18	IO68RSB1
E19	IO71RSB1
F1	IO198RSB3
F2	GND
F3	IO201RSB3
F4	IO204RSB3
F5	IO16RSB0
F15	IO50RSB0
F16	IO74RSB1
F17	IO72RSB1
F18	GND
F19	IO73RSB1
G1	IO195RSB3
G2	IO200RSB3
G4	IO202RSB3
G5	IO08RSB0
G7	GAC2/IO207RSB3
G8	VCCIB0
G9	IO26RSB0
G10	IO35RSB0
G11	IO44RSB0
G12	VCCIB0
G13	IO51RSB0
G15	IO70RSB1
G16	IO75RSB1
G18	GCC0/IO80RSB1
G19	GCB1/IO81RSB1
H1	GFB0/IO191RSB3
H2	IO196RSB3
H4	GFC1/IO194RSB3
H5	GFB1/IO192RSB3
H7	VCCIB3

CS289	
Pin Number	AGLP125 Function
A1	GAB1/IO03RSB0
A2	IO11RSB0
A3	IO08RSB0
A4	GND
A5	IO19RSB0
A6	IO24RSB0
A7	IO26RSB0
A8	IO30RSB0
A9	GND
A10	IO35RSB0
A11	IO38RSB0
A12	IO40RSB0
A13	IO42RSB0
A14	GND
A15	IO48RSB0
A16	IO54RSB0
A17	GBC0/IO57RSB0
B1	GAA1/IO01RSB0
B2	GND
B3	IO06RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO21RSB0
B7	VCCIB0
B8	IO28RSB0
B9	IO31RSB0
B10	IO37RSB0
B11	IO39RSB0
B12	VCCIB0
B13	IO44RSB0
B14	IO46RSB0
B15	IO49RSB0
B16	GBC1/IO58RSB0
B17	GND
C1	IO210RSB3
C2	GAA0/IO00RSB0
C3	GAC0/IO04RSB0
C4	IO09RSB0

CS289	
Pin Number	AGLP125 Function
C5	VCCIB0
C6	IO17RSB0
C7	IO23RSB0
C8	IO27RSB0
C9	IO33RSB0
C10	GND
C11	IO43RSB0
C12	IO45RSB0
C13	IO50RSB0
C14	IO52RSB0
C15	GND
C16	GBA0/IO61RSB0
C17	IO68RSB1
D1	IO204RSB3
D2	IO205RSB3
D3	GND
D4	GAB0/IO02RSB0
D5	IO07RSB0
D6	IO10RSB0
D7	IO18RSB0
D8	GND
D9	IO34RSB0
D10	IO41RSB0
D11	IO47RSB0
D12	IO55RSB0
D13	GND
D14	GBB0/IO59RSB0
D15	GBA1/IO62RSB0
D16	IO66RSB1
D17	IO70RSB1
E1	VCCIB3
E2	IO200RSB3
E3	GAC2/IO207RSB3
E4	GAA2/IO211RSB3
E5	GAC1/IO05RSB0
E6	IO12RSB0
E7	IO16RSB0
E8	IO22RSB0

CS289	
Pin Number	AGLP125 Function
E9	IO32RSB0
E10	IO36RSB0
E11	VCCIB0
E12	IO56RSB0
E13	GBB1/IO60RSB0
E14	GBA2/IO63RSB1
E15	GBB2/IO65RSB1
E16	VCCIB1
E17	IO73RSB1
F1	GFC1/IO194RSB3
F2	IO196RSB3
F3	IO202RSB3
F4	VCCIB3
F5	GAB2/IO209RSB3
F6	IO208RSB3
F7	IO14RSB0
F8	IO20RSB0
F9	IO25RSB0
F10	IO29RSB0
F11	IO51RSB0
F12	IO53RSB0
F13	GBC2/IO67RSB1
F14	GND
F15	IO75RSB1
F16	IO71RSB1
F17	IO77RSB1
G1	GFC0/IO193RSB3
G2	GND
G3	IO198RSB3
G4	IO203RSB3
G5	IO201RSB3
G6	IO206RSB3
G7	GND
G8	GND
G9	VCC
G10	GND
G11	GND
G12	IO72RSB1

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3