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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3120
Total RAM Bits	36864
Number of I/O	212
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp125v2-csg281

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

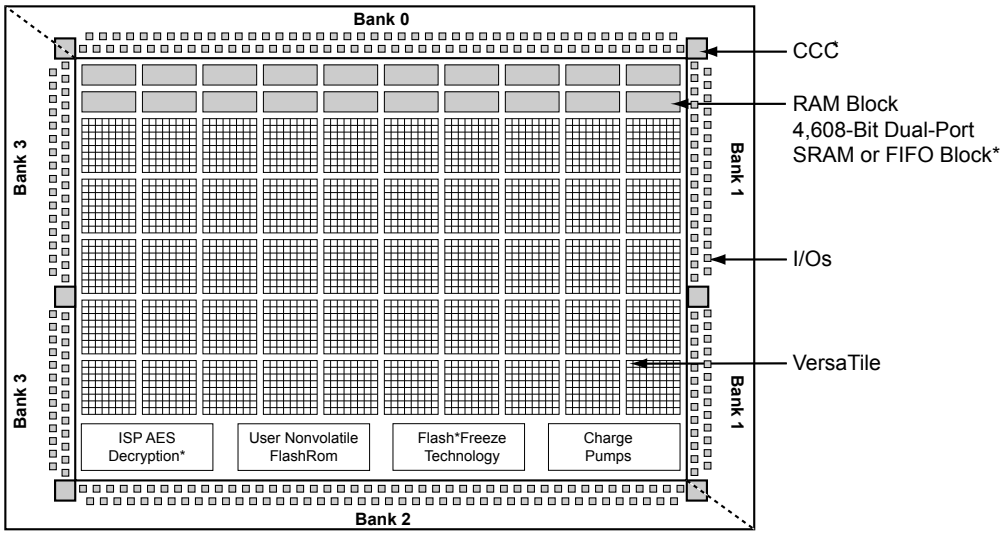
*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production



*Note: *Not supported by AGLP030 devices*

Figure 1-1 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

*Flash*Freeze Technology*

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

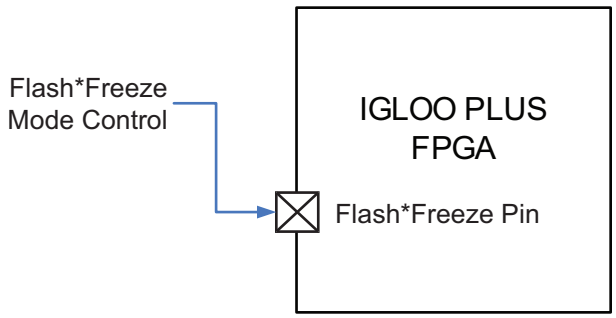


Figure 1-2 • **IGLOO PLUS Flash*Freeze Mode**

2 – IGLOO PLUS DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
V_I[1]	I/O input voltage	–0.3 V to 3.6 V	V
T_{STG}[2]	Storage temperature	–65 to +150	°C
T_J[2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature [1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.46\text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{jb}	θ_{ja}			Unit
					Still Air	1 m/s	2.5 m/s	
Chip Scale Package (CSP)	AGLP030	CS201	-	-	46.3	-	-	C/W
	AGLP060	CS201	7.1	19.7	40.5	35.1	32.9	C/W
	AGLP060	CS289	13.9	34.1	48.7	43.5	41.9	C/W
	AGLP125	CS289	10.8	27.9	42.2	37.1	35.5	C/W
	AGLP125	CS281	11.3	17.6	-	-	-	C/W
Thin Quad Flat Package (VQ)	AGLP030	VQ128	18.0	50.0	56.0	49.0	47.0	C/W
	AGLP060	VQ176	21.0	55.0	58.0	52.0	50.0	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.5	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V)**
For IGLOO PLUS V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.963	0.975	0.989	1.000	1.007	1.011
1.2	0.853	0.865	.0877	0.893	0.893	0.897
1.26	0.781	0.792	0.803	0.813	0.819	0.822

Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	2.874	1.727	0.000[1]
PAC2	Clock contribution of a Global Spine	1.264	1.244	2.241
PAC3	Clock contribution of a VersaTile row	0.963	0.975	0.981
PAC4	Clock contribution of a VersaTile used as a sequential module	0.098	0.096	0.096
PAC5	First contribution of a VersaTile used as a sequential module	0.018	0.018	0.018
PAC6	Second contribution of a VersaTile used as a sequential module	0.203	0.203	0.203
PAC7	Contribution of a VersaTile used as a combinatorial module	0.160	0.170	0.158
PAC8	Average contribution of a routing net	0.679	0.686	0.748
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.10		

Note: 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	0.90[1]		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. *This is the minimum contribution of the PLL when operating at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC software.*

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-14.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-14.

PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC1_3 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

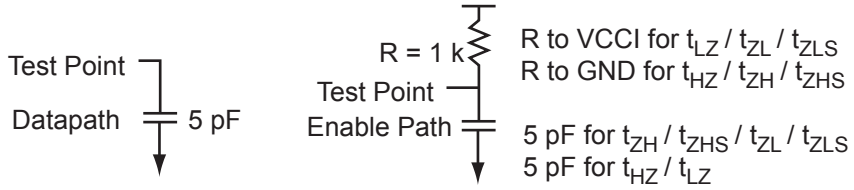


Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.89	0.18	1.00	1.43	0.66	6.01	5.43	1.78	1.30	ns
4 mA	STD	0.97	4.82	0.18	1.00	1.43	0.66	4.92	4.56	2.08	2.08	ns
6 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns
8 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.82	0.18	1.00	1.43	0.66	2.88	2.78	1.78	1.35	ns
4 mA	STD	0.97	2.30	0.18	1.00	1.43	0.66	2.35	2.11	2.08	2.15	ns
6 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
8 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.43	0.19	1.12	1.61	0.67	6.54	5.93	2.19	1.88	ns
4 mA	STD	0.98	5.33	0.19	1.12	1.61	0.67	5.41	5.03	2.50	2.68	ns
6 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns
8 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.30	0.19	1.12	1.61	0.67	3.34	3.21	2.19	1.93	ns
4 mA	STD	0.98	2.76	0.19	1.12	1.61	0.67	2.79	2.51	2.50	2.76	ns
6 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
8 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.72	ns
AND2	Y = A · B	t_{PD}	0.86	ns
NAND2	Y = !(A · B)	t_{PD}	1.00	ns
OR2	Y = A + B	t_{PD}	1.26	ns
NOR2	Y = !(A + B)	t_{PD}	1.16	ns
XOR2	Y = A ⊕ B	t_{PD}	1.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.47	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	2.12	ns
MUX2	Y = A !S + B S	t_{PD}	1.24	ns
AND3	Y = A · B · C	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-81 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.26	ns
AND2	Y = A · B	t_{PD}	1.46	ns
NAND2	Y = !(A · B)	t_{PD}	1.78	ns
OR2	Y = A + B	t_{PD}	2.47	ns
NOR2	Y = !(A + B)	t_{PD}	2.17	ns
XOR2	Y = A ⊕ B	t_{PD}	2.62	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.66	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.77	ns
MUX2	Y = A !S + B S	t_{PD}	2.20	ns
AND3	Y = A · B · C	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

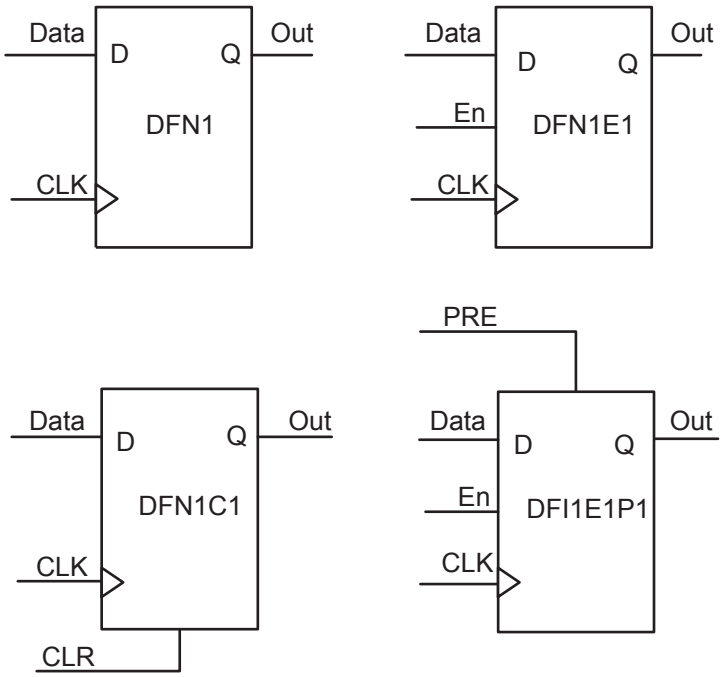


Figure 2-19 • **Sample of Sequential Cells**

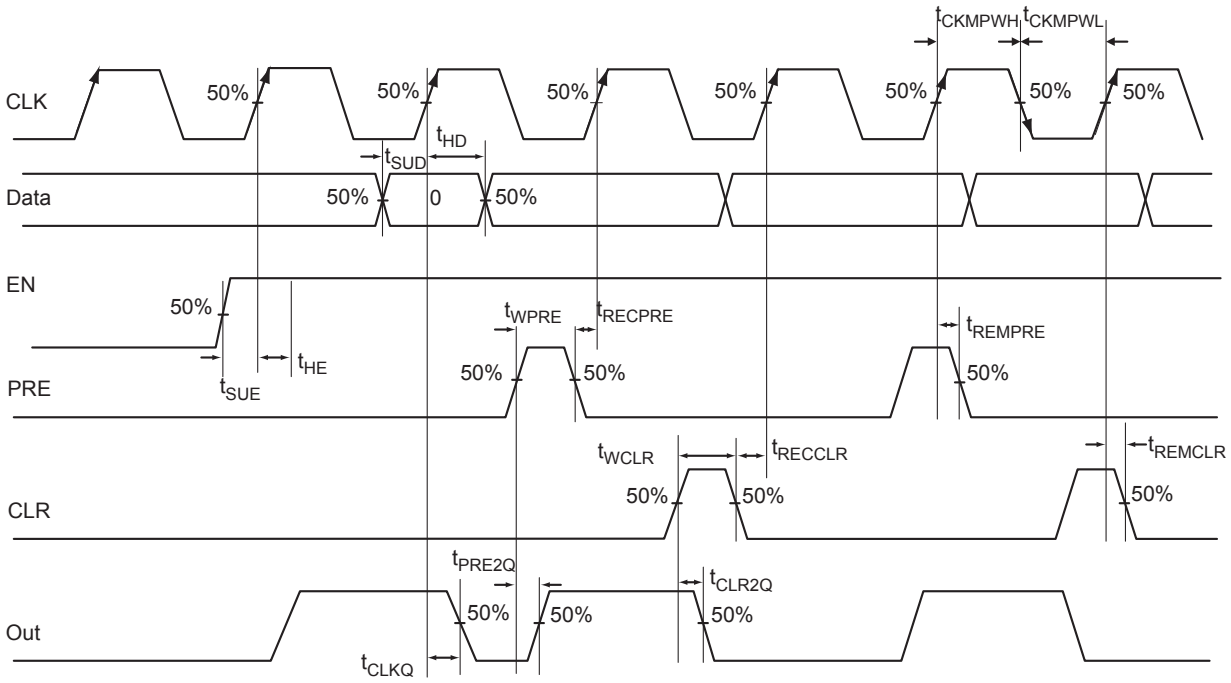


Figure 2-20 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Global Resource Characteristics

AGLP125 Clock Tree Topology

Clock delays are device-specific. Figure 2-21 is an example of a global tree used for clock routing. The global tree presented in Figure 2-21 is driven by a CCC located on the west side of the AGLP125 device. It is used to drive all D-flip-flops in the device.

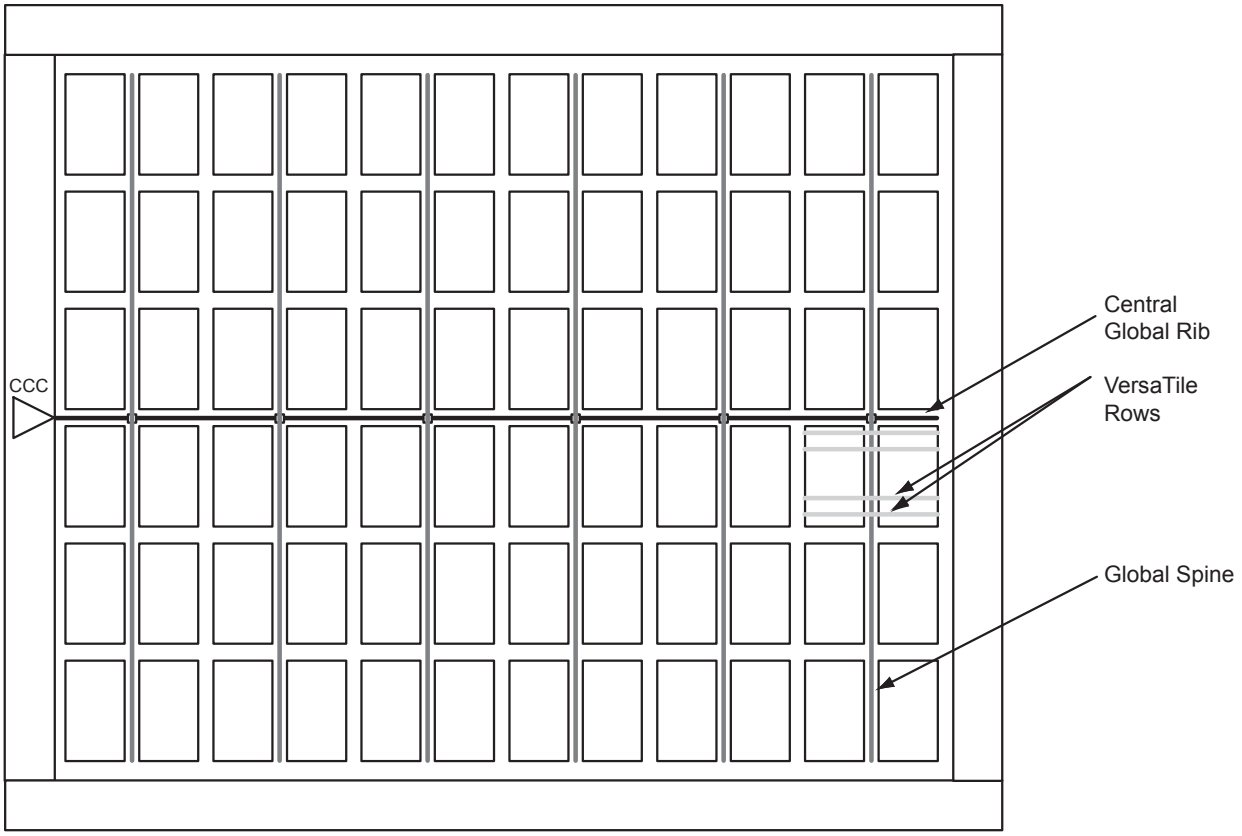


***Figure 2-21* • Example of Global Tree Use in an AGLP125 Device for Clock Routing**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-96 • FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.68	ns
	RESET Low to Data Out Low on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

***Table 3-2* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

IGLOO PLUS Device Family User's Guide

http://www.microsemi.com/soc/documents/IGLOOPLUS_UG.pdf

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are available at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ176	
Pin Number	AGLP060 Function
1	GAA2/IO156RSB3
2	IO155RSB3
3	GAB2/IO154RSB3
4	IO153RSB3
5	GAC2/IO152RSB3
6	GND
7	VCCIB3
8	IO149RSB3
9	IO147RSB3
10	IO145RSB3
11	IO144RSB3
12	IO143RSB3
13	VCC
14	IO141RSB3
15	GFC1/IO140RSB3
16	GFB1/IO138RSB3
17	GFB0/IO137RSB3
18	VCOMPLF
19	GFA1/IO136RSB3
20	VCCPLF
21	GFA0/IO135RSB3
22	GND
23	VCCIB3
24	GFA2/IO134RSB3
25	GFB2/IO133RSB3
26	GFC2/IO132RSB3
27	IO131RSB3
28	IO130RSB3
29	IO129RSB3
30	IO127RSB3
31	IO126RSB3
32	IO125RSB3
33	IO123RSB3
34	IO122RSB3
35	IO121RSB3

VQ176	
Pin Number	AGLP060 Function
36	IO119RSB3
37	GND
38	VCCIB3
39	GEC1/IO116RSB3
40	GEB1/IO114RSB3
41	GEC0/IO115RSB3
42	GEB0/IO113RSB3
43	GEA1/IO112RSB3
44	GEA0/IO111RSB3
45	GEA2/IO110RSB2
46	NC
47	FF/GEB2/IO109RSB2
48	GEC2/IO108RSB2
49	IO106RSB2
50	IO107RSB2
51	IO104RSB2
52	IO105RSB2
53	IO102RSB2
54	IO103RSB2
55	GND
56	VCCIB2
57	IO101RSB2
58	IO100RSB2
59	IO99RSB2
60	IO98RSB2
61	IO97RSB2
62	IO96RSB2
63	IO95RSB2
64	IO94RSB2
65	IO93RSB2
66	VCC
67	IO92RSB2
68	IO91RSB2
69	IO90RSB2

VQ176	
Pin Number	AGLP060 Function
70	IO89RSB2
71	IO88RSB2
72	IO87RSB2
73	IO86RSB2
74	IO85RSB2
75	IO84RSB2
76	GND
77	VCCIB2
78	IO83RSB2
79	IO82RSB2
80	GDC2/IO80RSB2
81	IO81RSB2
82	GDA2/IO78RSB2
83	GDB2/IO79RSB2
84	NC
85	NC
86	TCK
87	TDI
88	TMS
89	VPUMP
90	TDO
91	TRST
92	VJTAG
93	GDA1/IO76RSB1
94	GDC0/IO73RSB1
95	GDB1/IO74RSB1
96	GDC1/IO72RSB1
97	VCCIB1
98	GND
99	IO70RSB1
100	IO69RSB1
101	IO67RSB1
102	IO66RSB1
103	IO65RSB1
104	IO63RSB1

CS201	
Pin Number	AGLP030 Function
A1	NC
A2	IO04RSB0
A3	IO06RSB0
A4	IO09RSB0
A5	IO11RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO18RSB0
A9	IO24RSB0
A10	IO26RSB0
A11	IO27RSB0
A12	IO31RSB0
A13	NC
A14	NC
A15	NC
B1	NC
B2	NC
B3	IO08RSB0
B4	IO05RSB0
B5	IO07RSB0
B6	IO15RSB0
B7	IO14RSB0
B8	IO16RSB0
B9	IO20RSB0
B10	IO22RSB0
B11	IO34RSB0
B12	IO29RSB0
B13	NC
B14	NC
B15	NC
C1	NC
C2	NC
C3	GND
C4	IO00RSB0
C5	IO02RSB0

CS201	
Pin Number	AGLP030 Function
C6	IO12RSB0
C7	IO23RSB0
C8	IO19RSB0
C9	IO28RSB0
C10	IO32RSB0
C11	IO35RSB0
C12	NC
C13	GND
C14	IO41RSB1
C15	IO37RSB1
D1	IO117RSB3
D2	IO118RSB3
D3	NC
D4	GND
D5	IO01RSB0
D6	IO03RSB0
D7	IO10RSB0
D8	IO21RSB0
D9	IO25RSB0
D10	IO30RSB0
D11	IO33RSB0
D12	GND
D13	NC
D14	IO36RSB1
D15	IO39RSB1
E1	IO115RSB3
E2	IO114RSB3
E3	NC
E4	NC
E12	NC
E13	NC
E14	GDC0/IO46RSB1
E15	GDB0/IO48RSB1
F1	IO113RSB3
F2	IO116RSB3

CS201	
Pin Number	AGLP030 Function
F3	IO119RSB3
F4	IO111RSB3
F6	GND
F7	VCC
F8	VCCIB0
F9	VCCIB0
F10	VCCIB0
F12	NC
F13	NC
F14	IO40RSB1
F15	IO38RSB1
G1	NC
G2	IO112RSB3
G3	IO110RSB3
G4	IO109RSB3
G6	VCCIB3
G7	GND
G8	VCC
G9	GND
G10	GND
G12	NC
G13	NC
G14	IO42RSB1
G15	IO44RSB1
H1	NC
H2	GEB0/IO106RSB3
H3	GEC0/IO108RSB3
H4	NC
H6	VCCIB3
H7	GND
H8	VCC
H9	GND
H10	VCCIB1
H12	IO54RSB1
H13	GDA0/IO47RSB1

Revision	Changes	Page
Revision 11 (continued)	Table 2-2 • Recommended Operating Conditions[1,2] was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were revised.	2-6, 2-6
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
	VIH maximum values in tables were updated as needed to 3.6 V (SARs 20990, 79370).	N/A
	The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable. Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Table 2-22 • Summary of Maximum and Minimum DC Input Levels Table 2-23 • Summary of AC Measuring Points Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-28 • I/O Output Buffer Maximum Resistances [1]	2-9 2-9 2-19 2-20 2-20 2-22 2-23 2-24
	A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.	2-10, 2-11
	Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining $R_{WEAK\ PULL\text{-}UP\text{-}MAX}$ and $R_{WEAK\ PULLDOWN\text{-}MAX}$ were revised (SAR 21348).	2-25
	Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).	2-25
	Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).	2-26

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3