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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

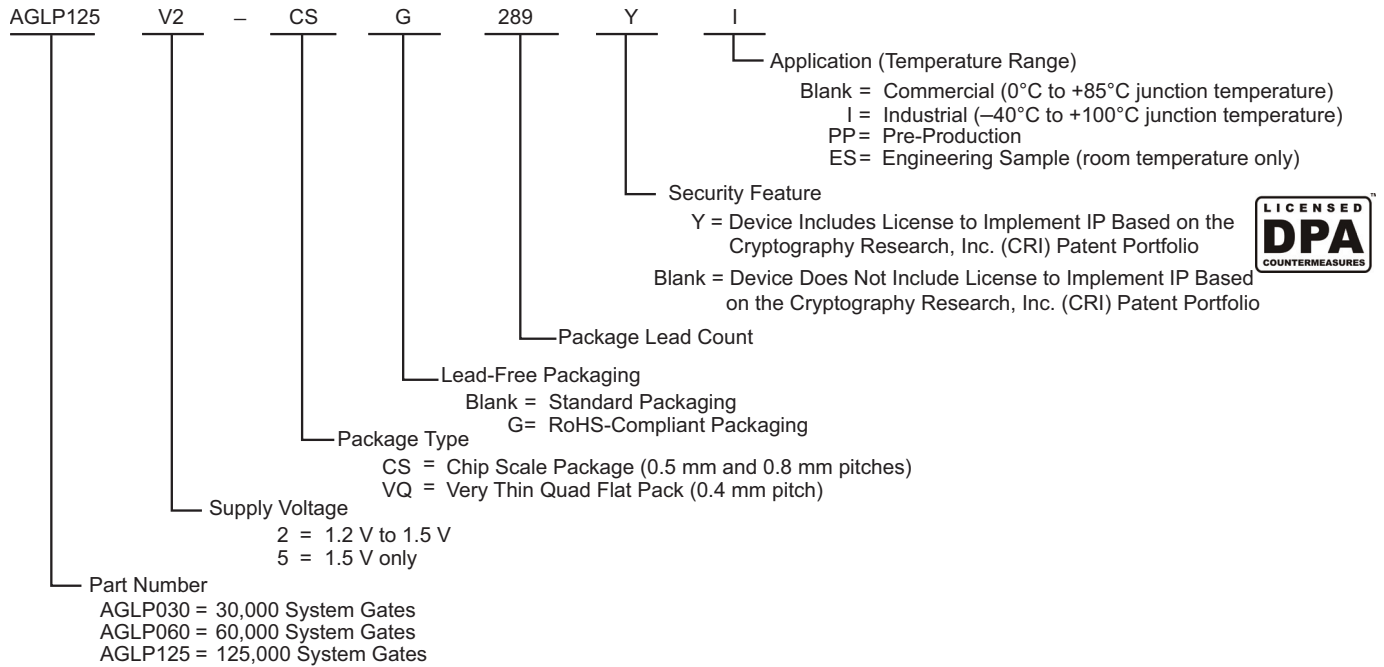
### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3120
Total RAM Bits	36864
Number of I/O	212
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/aglp125v2-csg281i">https://www.e-xfl.com/product-detail/microchip-technology/aglp125v2-csg281i</a>

## IGLOO PLUS Ordering Information



1. Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.
2. "G" indicates RoHS-compliant packages.

## **Security**

Nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO PLUS device provides the best available security for programmable logic designs.

## **Single Chip**

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2 V or 1.5 V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

## **Instant On**

Flash-based IGLOO PLUS devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash\*Freeze mode. This is done almost instantly (within 1  $\mu$ s), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

## **Reduced Cost of Ownership**

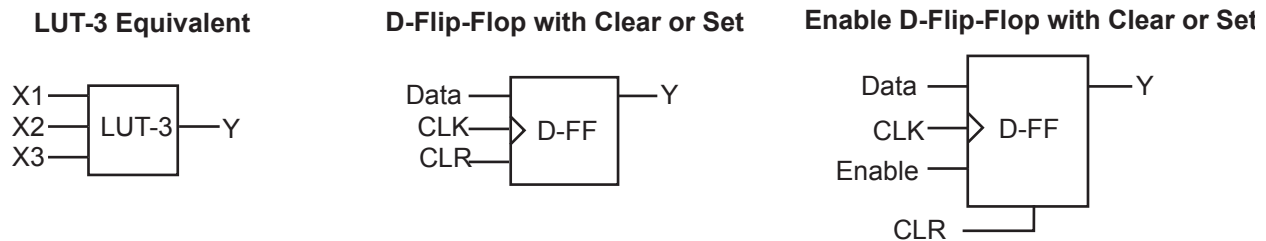
Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm.

## VersaTiles

The IGLOO PLUS core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The IGLOO PLUS VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.



**Figure 1-3 • VersaTile Configurations**

## User Nonvolatile FlashROM

IGLOO PLUS devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO PLUS IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in AGLP030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO PLUS development software solutions, Libero<sup>®</sup> System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

**Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash\*Freeze Mode <sup>1</sup>**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
<b>ICCA Current <sup>2</sup></b>					
Typical (25°C)	1.2 V	6	10	13	μA
	1.5 V	16	20	28	μA
<b>ICCI or JTAG Current</b>					
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	μA

**Notes:**

1.  $IDD = N_{BANKS} * ICCI + ICCA$ . JTAG counts as one bank when powered.
2. Includes VCC, VCCPLL, and VPUMP currents.

## Power per I/O Pin

**Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (μW/MHz) <sup>1</sup>
<b>Single-Ended</b>		
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range <sup>2</sup>	3.3	16.26
3.3 V LVCMOS Wide Range <sup>2</sup> – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS <sup>3</sup>	1.2	0.55
1.2 V LVCMOS <sup>3</sup> – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range <sup>3</sup>	1.2	0.55
1.2 V LVCMOS Wide Range <sup>3</sup> – Schmitt Trigger	1.2	0.47

**Notes:**

1. PAC9 is the total dynamic power measured on VCCI.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

**Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings<sup>1</sup>**

	C <sub>LOAD</sub> (pF)	VCCI (V)	Dynamic Power PAC10 (μW/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range <sup>3</sup>	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS <sup>4</sup>	5	1.2	15.22
1.2 V LVCMOS Wide Range <sup>4</sup>	5	1.2	15.22

**Notes:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PAC10 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade**  
**Commercial-Case Conditions:  $T_J = 70^{\circ}\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI} = 3.0\text{ V}$**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12 mA	High	5 pF	–	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.29	0.19	1.19	1.40	0.67	2.32	1.94	2.65	3.27	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns
1.2 V LVCMOS	2 mA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns
1.2 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## Single-Ended I/O Characteristics

### 3.3 V LVTTTL / 3.3 V LVCMOS

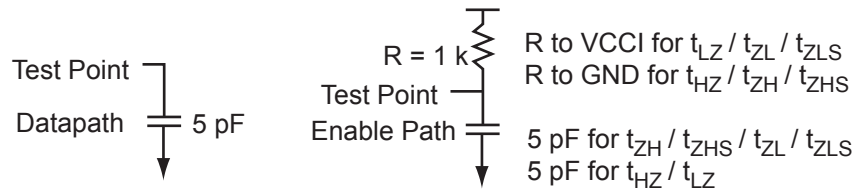
Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

**Table 2-34 • Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

**Notes:**

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-7 • AC Loading**

**Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	5

**Note:** \*Measuring point = Vtrip. See [Table 2-23 on page 2-20](#) for a complete table of trip points.



## Timing Characteristics

*Applies to 1.5 V DC Core Voltage*

**Table 2-42 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	4 mA	STD	0.97	5.85	0.18	1.18	1.64	0.66	5.86	5.05	2.57	2.57	ns
100 $\mu\text{A}$	6 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 $\mu\text{A}$	8 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 $\mu\text{A}$	12 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns
100 $\mu\text{A}$	16 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns

### Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-43 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	4 mA	STD	0.97	3.39	0.18	1.18	1.64	0.66	3.41	2.69	2.57	2.73	ns
100 $\mu\text{A}$	6 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 $\mu\text{A}$	8 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 $\mu\text{A}$	12 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
100 $\mu\text{A}$	16 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns

### Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

## 1.2 V LVCMOS (JESD8-12A)

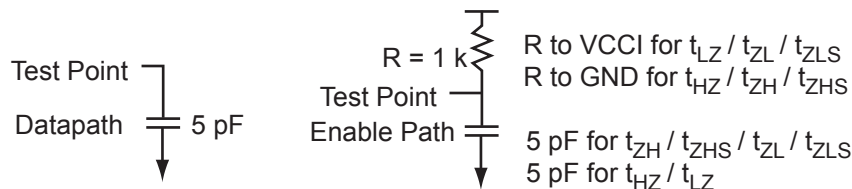
Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

**Table 2-64 • Minimum and Maximum DC Input and Output Levels**

1.2 V LVCMOS <sup>1</sup>	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. Applicable to IGLOO nano V2 devices operating at  $VCCI \geq VCC$ .
2. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < V_{IN} < V_{IL}$ .
3. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.



**Figure 2-11 • AC Loading**

**Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.2	0.6	5

Note: \*Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

## Timing Characteristics

Applies to 1.2 V DC Core Voltage

**Table 2-66 • 1.2 V LVCMOS Low Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-67 • 1.2 V LVCMOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

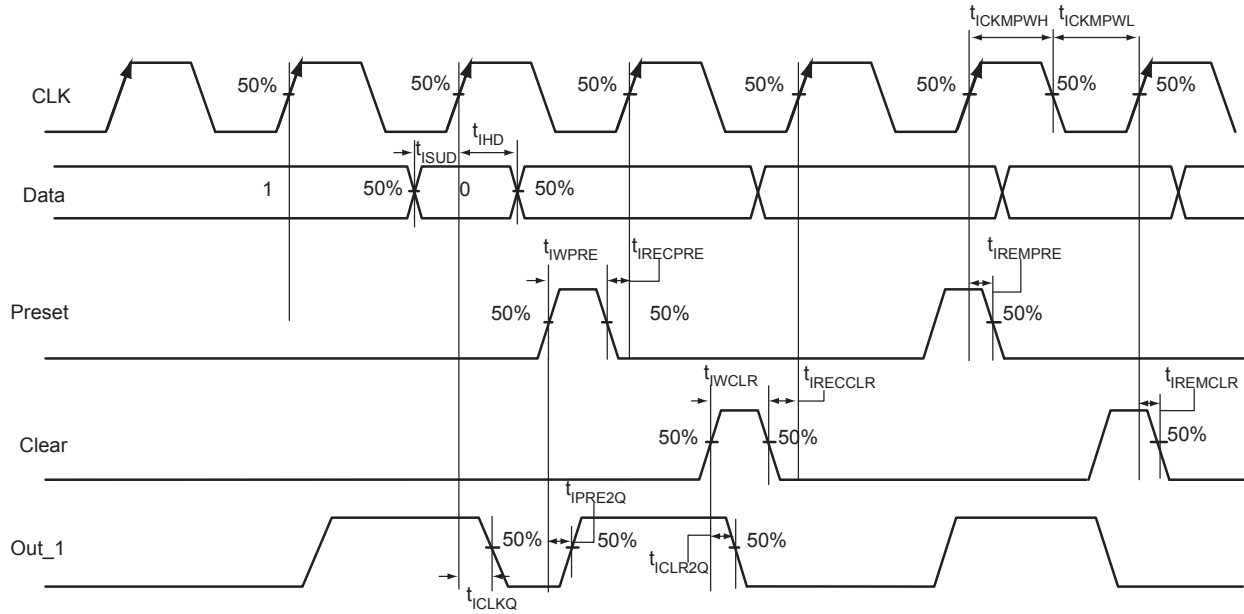
1. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
2. Software default selection highlighted in gray.

**Table 2-72 • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	H, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	F, H
$t_{OHD}$	Data Hold Time for the Output Data Register	F, H
$t_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	H, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	J, H
$t_{OEHD}$	Data Hold Time for the Output Enable Register	J, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
$t_{iCLKQ}$	Clock-to-Q of the Input Data Register	A, E
$t_{iSUD}$	Data Setup Time for the Input Data Register	C, A
$t_{iHD}$	Data Hold Time for the Input Data Register	C, A
$t_{iPRE2Q}$	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note:* \*See Figure 2-12 on page 2-41 for more information.

## Input Register



**Figure 2-14 • Input Register Timing Diagram**

### Timing Characteristics

1.5 V DC Core Voltage

**Table 2-74 • Input Data Register Propagation Delays**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Input Data Register	0.41	ns
$t_{\text{SUD}}$	Data Setup Time for the Input Data Register	0.32	ns
$t_{\text{IHD}}$	Data Hold Time for the Input Data Register	0.00	ns
$t_{\text{CLR2Q}}$	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
$t_{\text{PRE2Q}}$	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
$t_{\text{REMCLR}}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECCLR}}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{\text{REMPRE}}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECPRE}}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
$t_{\text{WCLR}}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{WPRE}}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{CKMPWH}}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{\text{CKMPWL}}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

### 1.2 V DC Core Voltage

**Table 2-75 • Input Data Register Propagation Delays**

Commercial-Case Conditions:  $T_J = 70^{\circ}\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Input Data Register	0.66	ns
$t_{\text{SUD}}$	Data Setup Time for the Input Data Register	0.43	ns
$t_{\text{IHD}}$	Data Hold Time for the Input Data Register	0.00	ns
$t_{\text{CLR2Q}}$	Asynchronous Clear-to-Q of the Input Data Register	0.86	ns
$t_{\text{PRE2Q}}$	Asynchronous Preset-to-Q of the Input Data Register	0.86	ns
$t_{\text{REMCLR}}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECCLR}}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{\text{REMPRE}}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECPRE}}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
$t_{\text{WCLR}}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{WPRE}}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{CKMPWH}}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{\text{CKMPWL}}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

## 1.2 V DC Core Voltage

**Table 2-83 • Register Delays**

Commercial-Case Conditions:  $T_J = 70^{\circ}\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	1.61	ns
$t_{SUD}$	Data Setup Time for the Core Register	1.17	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	1.29	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.87	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.89	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	ns
$t_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width High for the Core Register	0.95	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

**Table 2-95 • RAM512X18**

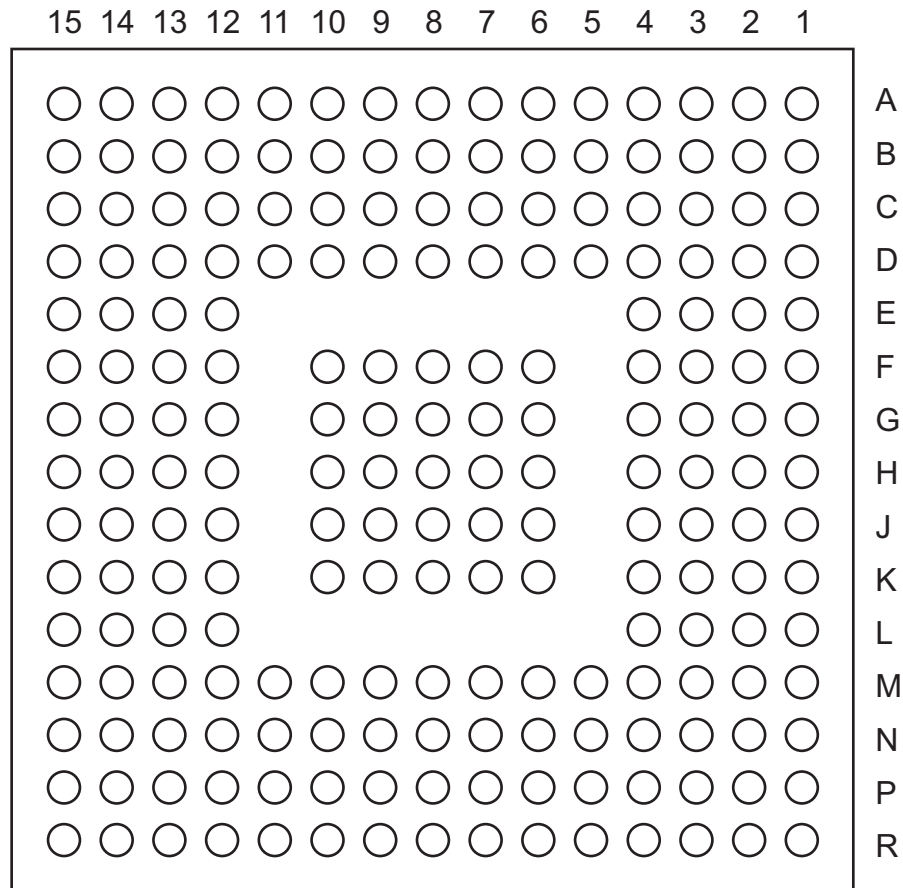
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
$t_{AS}$	Address setup time	1.28	ns
$t_{AH}$	Address hold time	0.25	ns
$t_{ENS}$	REN, WEN setup time	1.13	ns
$t_{ENH}$	REN, WEN hold time	0.13	ns
$t_{DS}$	Input data (WD) setup time	1.10	ns
$t_{DH}$	Input data (WD) hold time	0.55	ns
$t_{CKQ1}$	Clock High to new data valid on RD (output retained)	6.56	ns
$t_{CKQ2}$	Clock High to new data valid on RD (pipelined)	2.67	ns
$t_{C2CRWH}^1$	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.29	ns
$t_{C2CWRH}^1$	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.36	ns
$t_{RSTBQ}$	RESET Low to data out Low on RD (flow through)	3.21	ns
	RESET Low to data out Low on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
$t_{CYC}$	Clock cycle time	10.90	ns
$F_{MAX}$	Maximum frequency	92	MHz

**Notes:**

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## CS201



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.



CS201		CS201		CS201	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
A1	IO150RSB3	C6	IO07RSB0	F3	IO145RSB3
A2	GAA0/IO00RSB0	C7	IO16RSB0	F4	IO147RSB3
A3	GAC0/IO04RSB0	C8	IO21RSB0	F6	GND
A4	IO08RSB0	C9	IO28RSB0	F7	VCC
A5	IO11RSB0	C10	GBB1/IO33RSB0	F8	VCCIB0
A6	IO15RSB0	C11	GBA1/IO35RSB0	F9	VCCIB0
A7	IO17RSB0	C12	GBB2/IO38RSB1	F10	VCCIB0
A8	IO18RSB0	C13	GND	F12	IO47RSB1
A9	IO22RSB0	C14	IO48RSB1	F13	IO45RSB1
A10	IO26RSB0	C15	IO39RSB1	F14	GCC1/IO52RSB1
A11	IO29RSB0	D1	IO146RSB3	F15	GCA1/IO56RSB1
A12	GBC1/IO31RSB0	D2	IO144RSB3	G1*	VCOMPLF
A13	GBA2/IO36RSB1	D3	IO148RSB3	G2	GFB0/IO137RSB3
A14	IO41RSB1	D4	GND	G3	GFC0/IO139RSB3
A15	NC	D5	GAB0/IO02RSB0	G4	IO143RSB3
B1	IO151RSB3	D6	GAC1/IO05RSB0	G6	VCCIB3
B2	GAB2/IO154RSB3	D7	IO14RSB0	G7	GND
B3	IO06RSB0	D8	IO19RSB0	G8	VCC
B4	IO09RSB0	D9	GBC0/IO30RSB0	G9	GND
B5	IO13RSB0	D10	GBB0/IO32RSB0	G10	GND
B6	IO10RSB0	D11	GBA0/IO34RSB0	G12	IO50RSB1
B7	IO12RSB0	D12	GND	G13	GCB1/IO54RSB1
B8	IO20RSB0	D13	GBC2/IO40RSB1	G14	GCC2/IO60RSB1
B9	IO23RSB0	D14	IO51RSB1	G15	GCA2/IO58RSB1
B10	IO25RSB0	D15	IO44RSB1	H1*	VCCPLF
B11	IO24RSB0	E1	IO142RSB3	H2	GFA1/IO136RSB3
B12	IO27RSB0	E2	IO149RSB3	H3	GFB1/IO138RSB3
B13	IO37RSB1	E3	IO153RSB3	H4	NC
B14	IO46RSB1	E4	GAC2/IO152RSB3	H6	VCCIB3
B15	IO42RSB1	E12	IO43RSB1	H7	GND
C1	IO155RSB3	E13	IO49RSB1	H8	VCC
C2	GAA2/IO156RSB3	E14	GCC0/IO53RSB1	H9	GND
C3	GND	E15	GCB0/IO55RSB1	H10	VCCIB1
C4	GAA1/IO01RSB0	F1	IO141RSB3	H12	GCB2/IO59RSB1
C5	GAB1/IO03RSB0	F2	GFC1/IO140RSB3	H13	GCA0/IO57RSB1

**Note:** \*Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.

CS281	
Pin Number	AGLP125 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO23RSB0
A9	IO25RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO41RSB0
A13	IO43RSB0
A14	IO46RSB0
A15	IO55RSB0
A16	IO56RSB0
A17	GBC1/IO58RSB0
A18	GBA0/IO61RSB0
A19	GND
B1	GAA2/IO211RSB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO11RSB0
B6	GND
B7	IO21RSB0
B8	IO22RSB0
B9	IO28RSB0
B10	IO32RSB0
B11	IO36RSB0
B12	IO39RSB0
B13	IO42RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO57RSB0
B17	GBA1/IO62RSB0

CS281	
Pin Number	AGLP125 Function
B18	VCCIB1
B19	IO64RSB1
C1	GAB2/IO209RSB3
C2	IO210RSB3
C6	IO12RSB0
C14	IO47RSB0
C18	IO54RSB0
C19	GBB2/IO65RSB1
D1	IO206RSB3
D2	IO208RSB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO10RSB0
D7	IO17RSB0
D8	IO24RSB0
D9	IO27RSB0
D10	GND
D11	IO31RSB0
D12	IO40RSB0
D13	IO49RSB0
D14	IO45RSB0
D15	GBB0/IO59RSB0
D16	GBA2/IO63RSB1
D18	GBC2/IO67RSB1
D19	IO66RSB1
E1	IO203RSB3
E2	IO205RSB3
E4	IO07RSB0
E5	IO06RSB0
E6	IO14RSB0
E7	IO20RSB0
E8	IO29RSB0
E9	IO34RSB0
E10	IO30RSB0
E11	IO37RSB0
E12	IO38RSB0

CS281	
Pin Number	AGLP125 Function
E13	IO48RSB0
E14	GBB1/IO60RSB0
E15	IO53RSB0
E16	IO69RSB1
E18	IO68RSB1
E19	IO71RSB1
F1	IO198RSB3
F2	GND
F3	IO201RSB3
F4	IO204RSB3
F5	IO16RSB0
F15	IO50RSB0
F16	IO74RSB1
F17	IO72RSB1
F18	GND
F19	IO73RSB1
G1	IO195RSB3
G2	IO200RSB3
G4	IO202RSB3
G5	IO08RSB0
G7	GAC2/IO207RSB3
G8	VCCIB0
G9	IO26RSB0
G10	IO35RSB0
G11	IO44RSB0
G12	VCCIB0
G13	IO51RSB0
G15	IO70RSB1
G16	IO75RSB1
G18	GCC0/IO80RSB1
G19	GCB1/IO81RSB1
H1	GFB0/IO191RSB3
H2	IO196RSB3
H4	GFC1/IO194RSB3
H5	GFB1/IO192RSB3
H7	VCCIB3

Revision	Changes	Page
Revision 11 (continued)	Table 2-2 • Recommended Operating Conditions <sup>1,2</sup> was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T <sub>J</sub> = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T <sub>J</sub> = 70°C, VCC = 1.14 V) were revised.	2-6, 2-6
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
	VIH maximum values in tables were updated as needed to 3.6 V (SARs 20990, 79370).	N/A
	The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable.	
	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings	2-9
	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings <sup>1</sup>	2-9
	Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings	2-19
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels	2-20
	Table 2-23 • Summary of AC Measuring Points	2-20
	Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T <sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V	2-22
	Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T <sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V	2-23
	Table 2-28 • I/O Output Buffer Maximum Resistances <sup>1</sup>	2-24
	A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.	2-10, 2-11
	Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining R <sub>WEAK PULL-UP-MAX</sub> and R <sub>WEAK PULLDOWN-MAX</sub> were revised (SAR 21348).	2-25
	Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).	2-25
	Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).	2-26

Revision	Changes	Page
<b>Revision 10 (Apr 2009)</b> Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
<b>Revision 9 (Feb 2009)</b> Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
<b>Revision 8 (Jan 2009)</b> Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
<b>Revision 7 (Dec 2008)</b> Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm <sup>2</sup> .	II
<b>Revision 6 (Oct 2008)</b> DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T <sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T <sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
<b>Revision 5 (Aug 2008)</b> Product Brief v1.2  Packaging v1.4	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
<b>Revision 4 (Jul 2008)</b> Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
<b>Revision 3 (Jun 2008)</b> DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions <sup>1,2</sup> to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits <sup>1</sup> was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3

## Datasheet Categories

### **Categories**

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### **Advance**

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### **Preliminary**

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### **Production**

This version contains information that is considered to be final.

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