Microchip Technology - AGLP125V5-CSG281I Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3120
Total RAM Bits	36864
Number of I/O	212
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp125v5-csg281i

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	Single-Ended I/Os		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

---

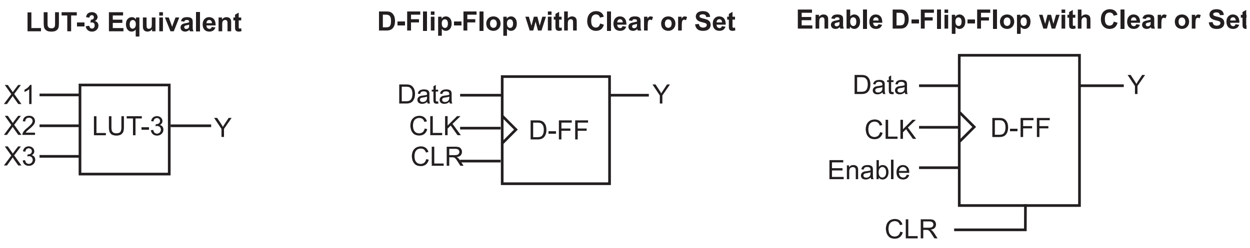
† The AGLP030 device does not support PLL or SRAM.

VersaTiles

The IGLOO PLUS core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{PLUS®}$ core tiles. The IGLOO PLUS VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.


LUT-3 Equivalent

D-Flip-Flop with Clear or Set

Enable D-Flip-Flop with Clear or Set

Figure 1-3 • **VersaTile Configurations**

User Nonvolatile FlashROM

IGLOO PLUS devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO PLUS IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in AGLP030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO PLUS development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

Table 2-3 • **Flash Programming Limits – Retention, Storage, and Operating Temperature** [1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits** [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Power per I/O Pin

Table 2-13 **• Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range[2]	3.3	16.26
3.3 V LVCMOS Wide Range[2] – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS[3]	1.2	0.55
1.2 V LVCMOS[3] – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range[3]	1.2	0.55
1.2 V LVCMOS Wide Range[3] – Schmitt Trigger	1.2	0.47

Notes:

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

Table 2-14 **• Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range[3]	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS[4]	5	1.2	15.22
1.2 V LVCMOS Wide Range[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 µA	26	20

Note: *T_J = 100°C

Table 2-72 **• Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-12 on page 2-41 for more information.

***Table 2-73* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-13 on page 2-43 for more information.

1.2 V DC Core Voltage

Table 2-75 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.66	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.43	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.86	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.86	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

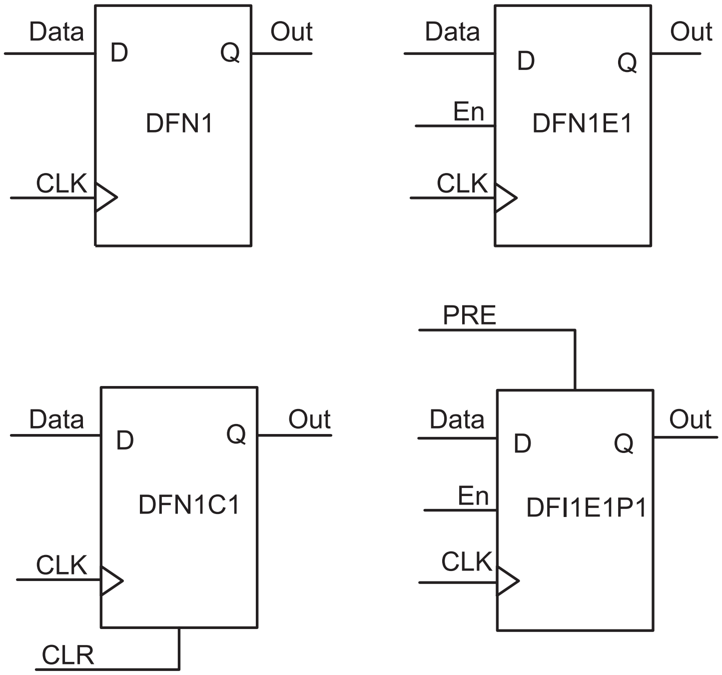


***Figure 2-19* • Sample of Sequential Cells**

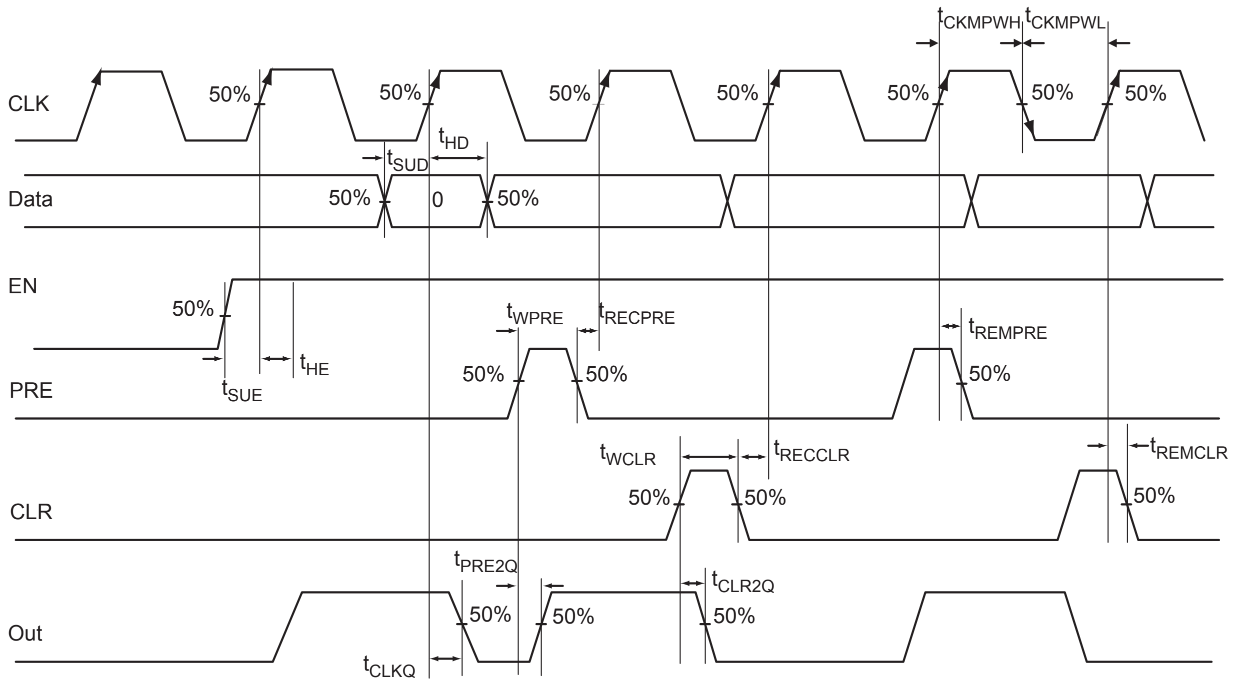


Figure 2-20 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • **Register Delays**

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-83 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

***Table 2-91* • IGLOO PLUS CCC/PLL Specification**
For IGLOO PLUS V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			60	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			.25	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.863		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]		5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	1.20%	2.00%	3.00%
50 MHz to 160 MHz	2.50%	5.00%	7.00%	15.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the online help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions.For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements are done with LVTTL 3.3 V, 8 mA, I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain, and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide*

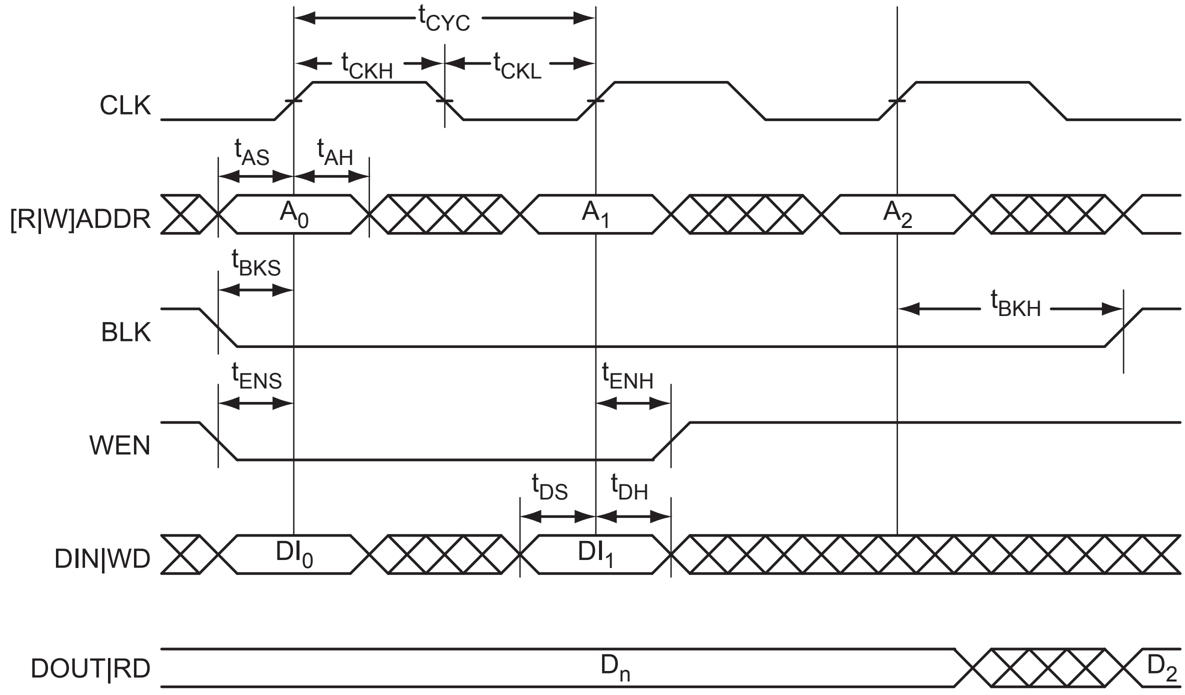


Figure 2-26 **• RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

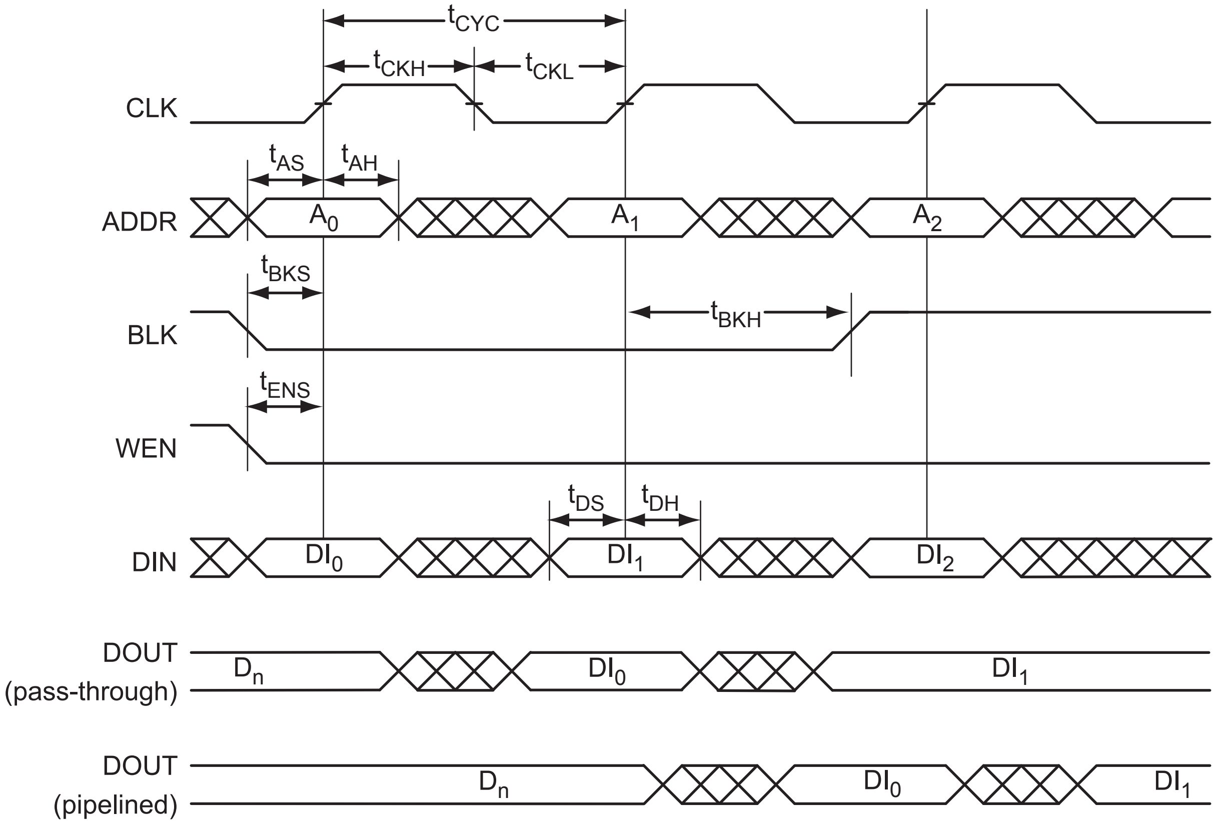


Figure 2-27 **• RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

FF Flash*Freeze Mode Activation Pin

The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO and ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS Device Family User's Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1* • Flash*Freeze Pin Location in IGLOO PLUS Devices**

Package	Flash*Freeze Pin
CS281	W2
CS201	R4
CS289	U1
VQ128	34
VQ176	47

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 **• Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

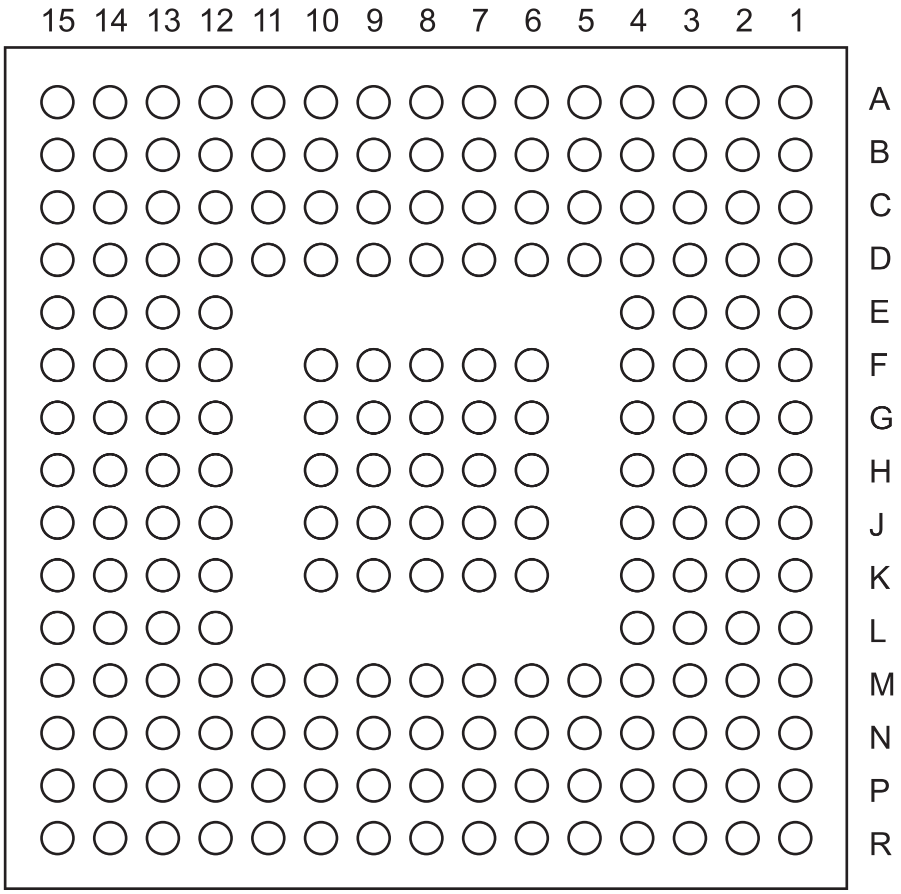
TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

CS201



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS281	
Pin Number	**AGLP125 Function**
R15	IO109RSB2
R16	GDA1/IO103RSB1
R18	GDB0/IO102RSB1
R19	GDC0/IO100RSB1
T1	IO171RSB3
T2	GEC0/IO169RSB3
T4	GEB0/IO167RSB3
T5	IO157RSB2
T6	IO158RSB2
T7	IO148RSB2
T8	IO145RSB2
T9	IO143RSB2
T10	GND
T11	IO129RSB2
T12	IO126RSB2
T13	IO125RSB2
T14	IO116RSB2
T15	GDC2/IO107RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO101RSB1
U1	IO160RSB2
U2	GEA1/IO166RSB3
U6	IO151RSB2
U14	IO121RSB2
U18	TRST
U19	GDA0/IO104RSB1
V1	IO159RSB2
V2	VCCIB3
V3	GEC2/IO162RSB2
V4	IO156RSB2
V5	IO153RSB2
V6	GND
V7	IO144RSB2
V8	IO141RSB2
V9	IO140RSB2

CS281	
Pin Number	**AGLP125 Function**
V10	IO133RSB2
V11	IO127RSB2
V12	IO123RSB2
V13	IO120RSB2
V14	GND
V15	IO113RSB2
V16	GDA2/IO105RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO163RSB2
W3	IO155RSB2
W4	IO152RSB2
W5	IO150RSB2
W6	IO147RSB2
W7	IO142RSB2
W8	IO139RSB2
W9	IO136RSB2
W10	VCCIB2
W11	IO128RSB2
W12	IO124RSB2
W13	IO119RSB2
W14	IO115RSB2
W15	IO114RSB2
W16	IO110RSB2
W17	GDB2/IO106RSB2
W18	TCK
W19	GND

Revision	Changes	Page
Revision 11 (continued)	Table 2-2 • Recommended Operating Conditions[1,2] was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were revised.	2-6, 2-6
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
	VIH maximum values in tables were updated as needed to 3.6 V (SARs 20990, 79370).	N/A
	The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable. Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Table 2-22 • Summary of Maximum and Minimum DC Input Levels Table 2-23 • Summary of AC Measuring Points Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-28 • I/O Output Buffer Maximum Resistances [1]	 2-9 2-9 2-19 2-20 2-20 2-22 2-23 2-24
	A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.	2-10, 2-11
	Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining $R_{\text{WEAK PULL-UP-MAX}}$ and $R_{\text{WEAK PULLDOWN-MAX}}$ were revised (SAR 21348).	2-25
	Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).	2-25
	Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).	2-26