Renesas Electronics America Inc - R7FS3A77C2A01CBJ#AC1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 26x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-LFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c2a01cbj-ac1

1. Overview

The S3A7 MCU comprises multiple series of software- and pin-compatible ARM-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

This MCU provides an optimal combination of low-power, high-performance ARM® Cortex®-M4 core running up to 48 MHz with the following features:

- Up to 1-MB code flash memory
- 192-KB SRAM
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit ADC
- 12-bit DAC
- Security features.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 48 MHz • ARM Cortex-M4: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single Precision Floating Point Unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 1 MB code flash memory. See section 48, Flash Memory in User's Manual.
Data flash memory	16 KB data flash memory. See section 48, Flash Memory in User's Manual.
Option-Setting Memory	The Option-Setting Memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the desired application image load address in code flash memory to the application image link address in the unused memory 23-bit space (memory mirror space addresses). The user application code is developed and linked to run from this MMF destination address. The user application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	This MCU has an on-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). There is an area in SRAM0 that provides error correction capability using ECC. See section 47, SRAM in User's Manual.

Table 1.3 System (2/2)

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset this MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 26, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The independent watchdog timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset this MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning this MCU to a known state as a fail safe mechanism when the system runs out of control. The watchdog timer can be triggered automatically on reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 27, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Interrupt control

Feature	Functional description
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.

Table 1.5 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.6 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	This MCU incorporates a Data Transfer Controller (DTC) that performs data transfers when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	This MCU incorporates an 4-channel DMA Controller (DMAC) module that can transfer data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.7 External bus interface

Feature	Functional description
External bus	• CS area: Connected to the external devices (external memory interface) • QSPI area: Connected to the QSPI (external device interface)

Table 1.8 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 10 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms for controlling brushless DC motors can be generated. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 24, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 25, Realtime Clock (RTC) in User's Manual.

Table 1.9 Communication interfaces (1/2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 29, Serial Communications Interface (SCI) in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 30, IrDA Interface in User's Manual.
I^2C Bus Interface (IIC)	This MCU has a three-channel I^2C bus interface (IIC). The IIC module conforms with and provides a subset of the NXP I^2C bus (Inter-Integrated Circuit bus) interface functions. See section 31, I^2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	This MCU includes two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 33, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface (SSI)	The Serial Sound Interface (SSI) peripheral provides functionality to interface digital audio devices for transmitting PCM audio data over a serial bus with this MCU. The SSI supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver/transmitter/transceiver to suit various applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 36, Serial Sound Interface (SSI) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 34, Quad Serial Peripheral Interface (QSPI) in User's Manual.

1.2 Block Diagram

Figure 1.1 shows the block diagram of this MCU superset. Individual devices within the group may have a subset of the features.

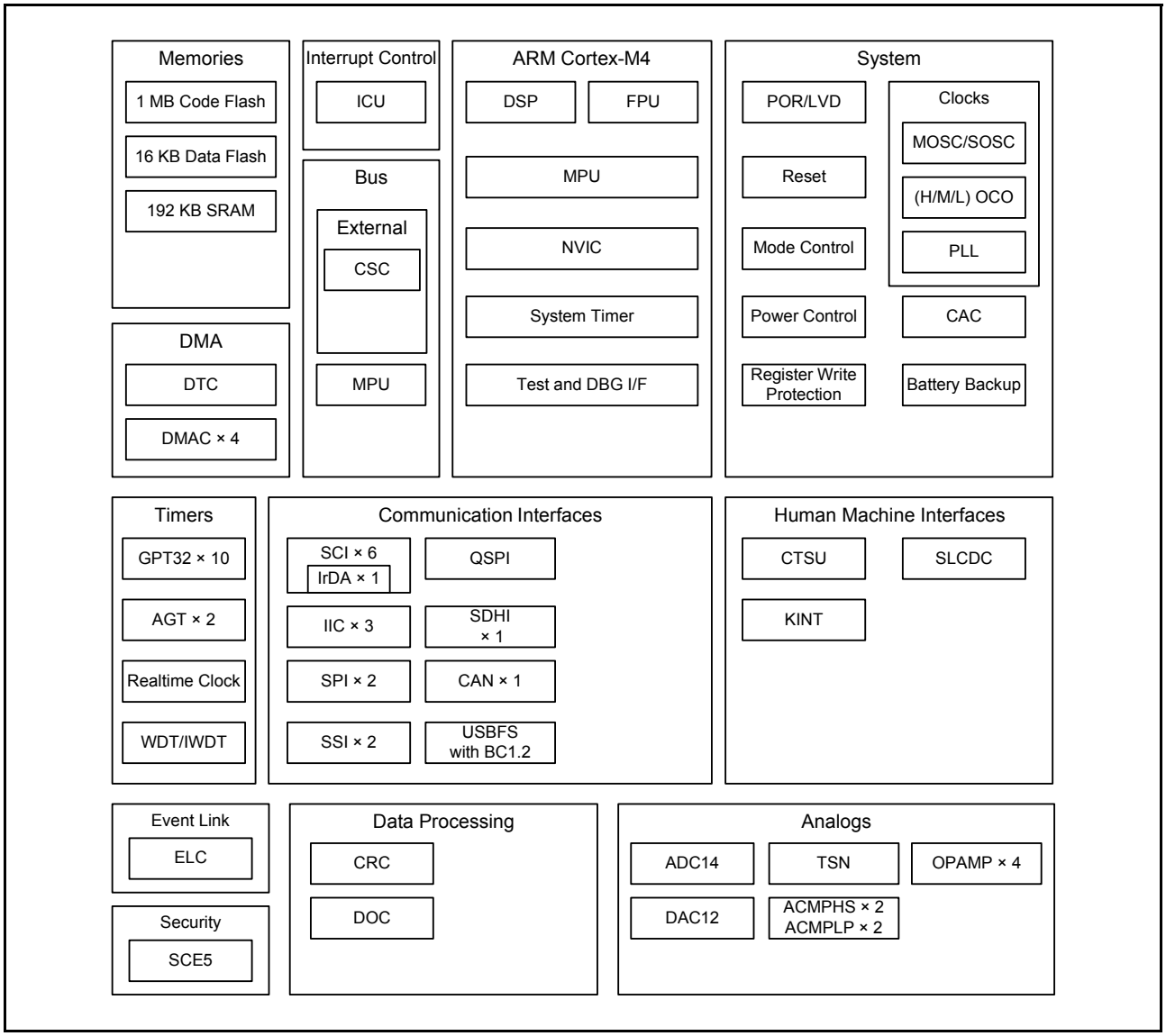


Figure 1.1 Block diagram

1.3 Part Numbering

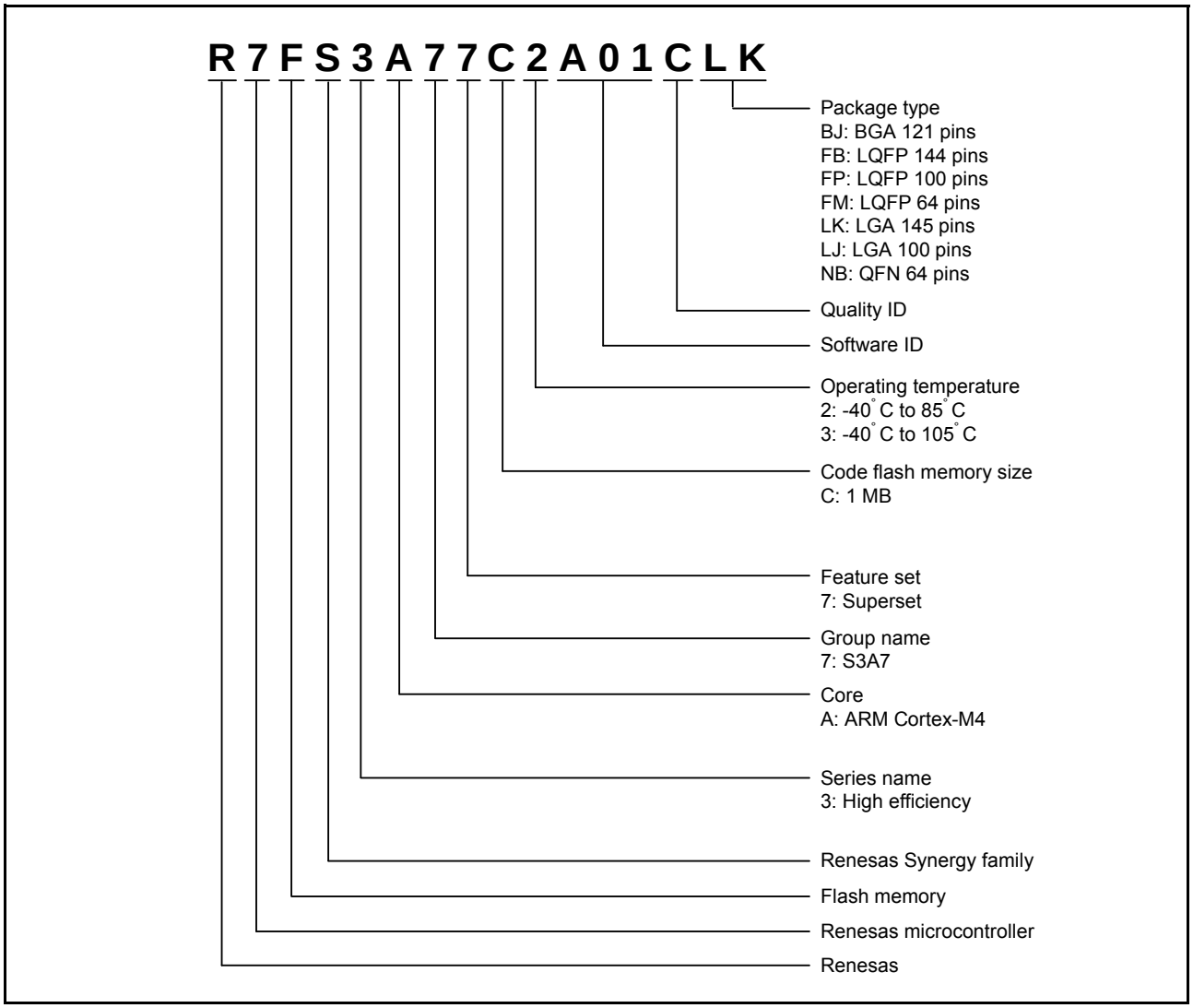


Figure 1.2 Part numbering scheme

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1, SSLA2, SSLA3, SSLB1, SSLB2, SSLB3	Output	Output pin for slave selection.
QSPI	QSPCLK	Output	QSPI clock output pin.
	QSSL	Output	QSPI slave output pin.
	QIO0	I/O	Master transmit data/data 0.
	QIO1	I/O	Master input data/data 1.
	QIO2, QIO3	I/O	Data 2, Data 3.
CAN	CRX0	Input	Receive data.
	CTX0	Output	Transmit data.
USBFS	VSS_USB	Input	Ground pins.
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator.
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	External overcurrent detection signals should be connected to these pins. VBUS comparator signals should be connected to these pins when the OTG power supply chip is connected.
	USB_ID	Input	MicroAB connector ID input signal should be connected to this pin during operation in OTG mode.
SDHI	SD0CLK	Output	SD clock output pin.
	SD0CMD	I/O	SD command output, response input signal pin.
	SD0DAT0 to SD0DAT7	I/O	SD data bus pins.
	SD0WP	Input	SD write-protect signal.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the analog. Connect this pin to VCC.
	AVSS0	Input	Analog ground pin. Connect this pin to VSS.
	VREFH0	Input	Analog reference voltage supply pin for the A/D converter. Connect this pin to VCC when not using the A/D converter.
	VREFL0	Input	Analog reference ground pin for the A/D converter. Connect this pin to VSS when not using the A/D converter.
	VREFH	Input	Analog reference voltage supply pin for D/A converter.
	VREFL	Input	Analog reference ground pin for D/A converter.
ADC14	AN000 to AN027	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active LOW.
DAC12	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
Comparator output	VCOUT	Output	Comparator output pin.
ACMPHS	IVREF0 to IVREF5	Input	Reference voltage input pin.
	IVCMP0 to IVCMP5	Input	Analog voltage input pin.
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pin.
	CMPIN0, CMPIN1	Input	Analog voltage input pins.

R7FS3A77C2A01CBJ

	A	B	C	D	E	F	G	H	J	K	L	
11	P407	P408	P411	P414	P212/ EXTAL	P215/ XCIN	VCL	P406	P403	P401	P400	11
10	USB_DM	USB_DP	P410	P415	P213/ XTAL	P214/ XCOUT	VBATT	P405	P402	P511	P512	10
9	VCC_ USB	VSS_ USB	P409	P412	P708	VCC	VSS	P404	P002	P001	P000	9
8	P205	VCC_ USB_ LDO	P206	P204	P413	P710	P702	P006	P004	P003	P005	8
7	P203	P202	P313	P314	P315	P709	P701	P007	AVSS0	P011/ VREFL0	P010/ VREFH0	7
6	VSS	VCC	RES	P201/MD	P200	NC	P700	P008	AVCC0	P013/ VREFL	P012/ VREFH	6
5	P308	P309	P307	P302	P304	P612	P601	P506	P505	P015	P014	5
4	P305	P306	P808	P114	P611	P603	P600	P504	P503	VSS	VCC	4
3	P809	P303	P110/TDI	P111	P609	P604	P106	P104	P502	P500	P501	3
2	P301	P108/ TMS/ SWDIO	P113	P608	P613	P605	P602	P105	P102	P801	P800	2
1	P300/ TCK/ SWCLK	P109/ TDO/ SWO	P112	P115	P610	VCC	VSS	P107	P103	P101	P100	1
	A	B	C	D	E	F	G	H	J	K	L	

Figure 1.5 Pin assignment for BGA 121-pin (Upper perspective view)

1.7 Pin Lists

Pin number							Power, System, Clock, Debug, CAC, VBATT	I/O ports	External bus	Timers				Communication interfaces						Analogs			HMI		
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64				AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSI	SDHI	ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	SLCDC	CTSU	Interrupt
N13	1	L11	1	J10	1	1		P400				GTIOC6A_A			SCK4_B	SCL0_A		AUDIO_CLK						TS20	IRQ0
L11	2	K11	2	J9	2	2		P401			GTETRGA_B	GTIOC6B_A		CTX0_B	CTS4_RTS4_B/SS4_B	SDA0_A								TS19	IRQ5
M13	3	J10	3	F6	3	3	VBATWIO0	P402		AGTIO0_B/AGTIO1_B			RTCIC0	CRX0_B										TS18	IRQ4
K11	4	J11	4	H10			VBATWIO1	P403		AGTIO0_C/AGTIO1_C		GTIOC3A_B	RTCIC1					SSISCK0_A						TS17	
L12	5	H9	5	G8			VBATWIO2	P404				GTIOC3B_B	RTCIC2					SSIWS0_A						TS16	
L13	6	H10	6	H9				P405				GTIOC1A_B						SSITXD0_A						TS15	
J10	7	H11	7	F7				P406				GTIOC1B_B						SSIRXD0_A						TS14	
H10	8	G6						P700				GTIOC5A_B												TS32	
K12	9	G7						P701				GTIOC5B_B												TS33	
K13	10	G8						P702				GTIOC6A_B												TS34	
J11	11							P703				GTIOC6B_B													
H11	12							P704																	
G11	13							P705																	
J12	14	G10	8	G9	4	4	VBATT																		
J13	15	G11	9	G10	5	5	VCL																		
H13	16	F11	10	F10	6	6	XCIN	P215																	
H12	17	F10	11	F9	7	7	XCOUT	P214																	
F12	18	G9	12	D9	8	8	VSS																		
G12	19	E10	13	E9	9	9	XTAL	P213			GTETRGC_A				TXD1_A/MOSI1_A/SDA1_A										IRQ2
G13	20	E11	14	E10	10	10	EXTAL	P212		AGTEE1	GTETRGD_A				RXD1_A/MISO1_A/SCL1_A										IRQ3
F13	21	F9	15	D10	11	11	VCC																		
G10	22							P713				GTIOC2A_B													
F11	23							P712				GTIOC2B_B													
E13	24							P711							CTS1_RTS1_B/SS1_B										
E12	25	F8						P710							SCK1_B									TS35	
F10	26	F7						P709							TXD1_B/MOSI1_B/SDA1_B									TS13	IRQ10
D13	27	E9	16	F8			CACREF_B	P708							RXD1_B/MISO1_B/SCL1_B			SSLA3_B						TS12	IRQ11
E11	28	D10	17	E8				P415										SSLA2_B						TS11	
D12	29	D11	18	E7				P414										SSLA1_B		SD0WP				TS10	
E10	30	E8	19	C9				P413			GTOUUP_B				CTS0_RTS0_B/SS0_B			SSLA0_B		SD0CLK				TS09	
C13	31	D9	20	C10				P412			GTOULO_B				SCK0_B		RSPCKA_B			SD0CMD				TS08	

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.5 to +6.5	V
Input voltage	5V-tolerant ports*1	V_{in}	–0.3 to +6.5	V
	P000 to P015	V_{in}	–0.3 to AVCC0 + 0.3	V
	Others	V_{in}	–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to +6.5	V
		VREFH		V
VBATT power supply voltage		VBATT	–0.5 to +6.5	V
Analog power supply voltage		AVCC0	–0.5 to +6.5	V
USB power supply voltage		VCC_USB	–0.5 to +6.5	V
		VCC_USB_LDO	–0.5 to +6.5	V
Analog input voltage	When AN000 to AN015 are used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN027 are used		–0.3 to VCC + 0.3	V
LCD voltage	VL1 voltage	V_{L1}	–0.3 to +2.8	V
	VL2 voltage	V_{L2}	–0.3 to +6.5	V
	VL3 voltage	V_{L3}	–0.3 to +6.5	V
	VL4 voltage	V_{L4}	–0.3 to +6.5	V
Operating temperature*2 *3		T_{opr}	–40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. The capacitor must be placed close to the pin.

Note 1. Ports P205, P206, P400 to P404, P407, P511, P512 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. See section 2.2.1, Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Table 2.2 Recommended operating conditions

Item	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB_LDO	-	5.5	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
VBATT power supply voltage	VBATT	When the battery backup function is not used	-	VCC	-	V
		When the battery backup function is used	1.6	-	3.6	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V
	VREFH	When used as DAC12 Reference	1.6	-	AVCC0	V
	VREFL		-	0	-	V

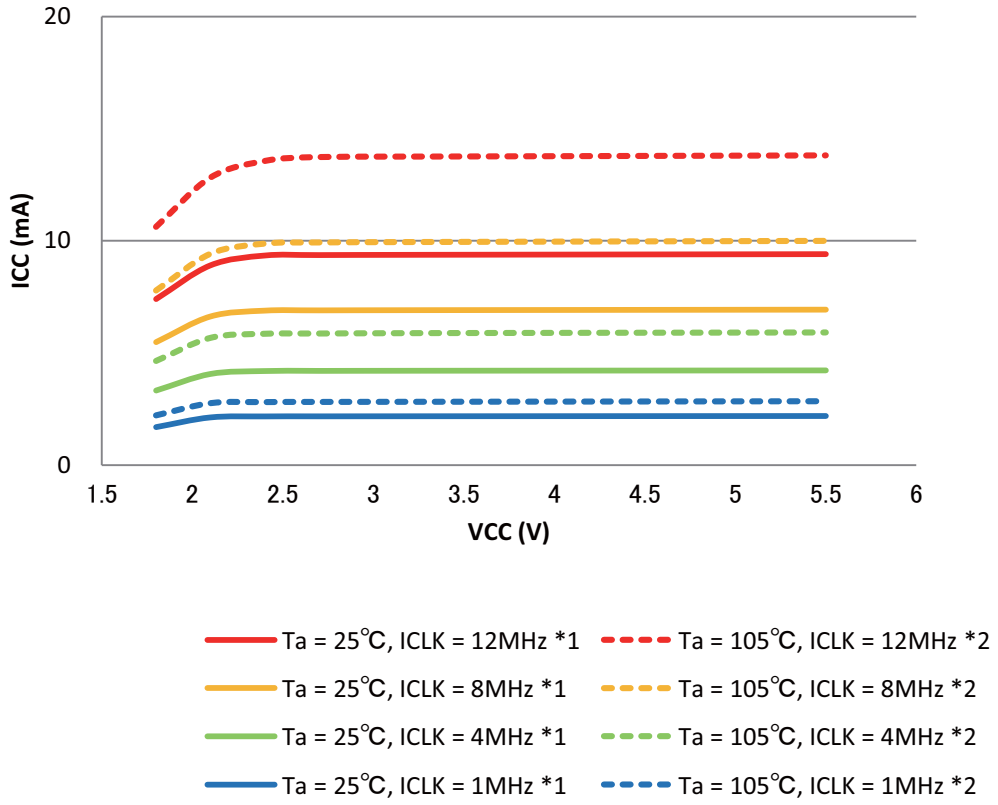
Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

2.2.9 Operating and Standby Current

Table 2.11 Operating and standby current (1) (1/2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 48 MHz	I_{CC}	11.8	-	mA	*7
				ICLK = 32 MHz		8.6	-		
				ICLK = 16 MHz		5.1	-		
				ICLK = 8 MHz		3.4	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 48 MHz		18.6	-		
				ICLK = 32 MHz		12.7	-		
				ICLK = 16 MHz		7.2	-		
				ICLK = 8 MHz		4.5	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 48 MHz		30.1	-		*9
				ICLK = 32 MHz		23.2	-		*8
				ICLK = 16 MHz		12.6	-		
				ICLK = 8 MHz		7.3	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 48 MHz		-	75.0		*9
		Sleep mode	All peripheral clock disabled*5	ICLK = 48 MHz		6.4	-		*7
				ICLK = 32 MHz		4.7	-		
				ICLK = 16 MHz		3.2	-		
				ICLK = 8 MHz		2.4	-		
			All peripheral clock enabled*5	ICLK = 48 MHz		24.7	-		*9
				ICLK = 32 MHz		19.2	-		*8
				ICLK = 16 MHz		10.7	-		
				ICLK = 8 MHz		6.4	-		
		Increase during BGO operation*6				2.5	-		-
	Middle-speed mode*2	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 12 MHz	I_{CC}	3.6	-	mA	*7
				ICLK = 8 MHz		3.0	-		
				ICLK = 1 MHz		1.4	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		5.2	-		
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.6	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 12 MHz		9.4	-		*8
				ICLK = 8 MHz		6.9	-		
				ICLK = 1 MHz		2.2	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 12 MHz		-	30.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 12 MHz		2.2	-		*7
				ICLK = 8 MHz		2.0	-		
				ICLK = 1 MHz		1.3	-		
			All peripheral clock enabled*5	ICLK = 12 MHz		7.9	-		*8
				ICLK = 8 MHz		5.9	-		
				ICLK = 1 MHz		1.3	-		
		Increase during BGO operation*6				2.5	-		-



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.18 Voltage dependency in middle-speed mode (reference data)

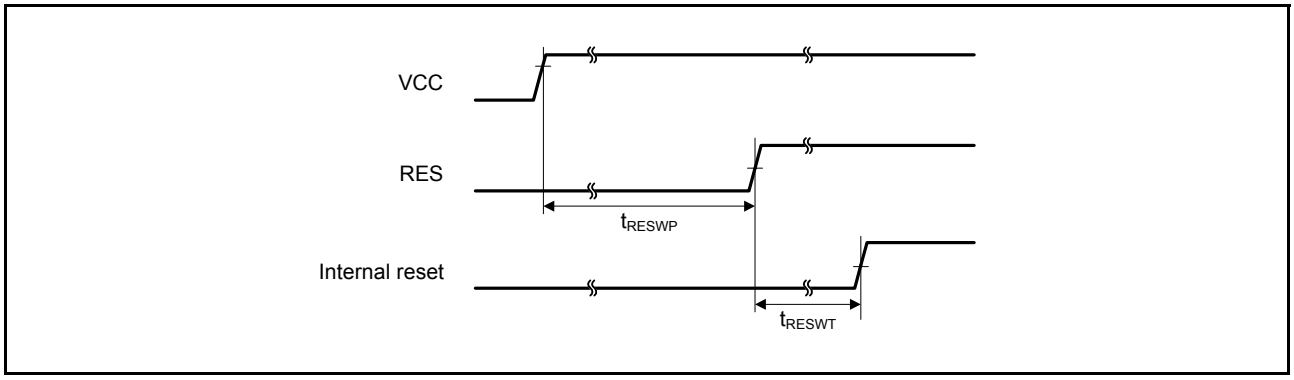


Figure 2.32 Reset input timing at power-on

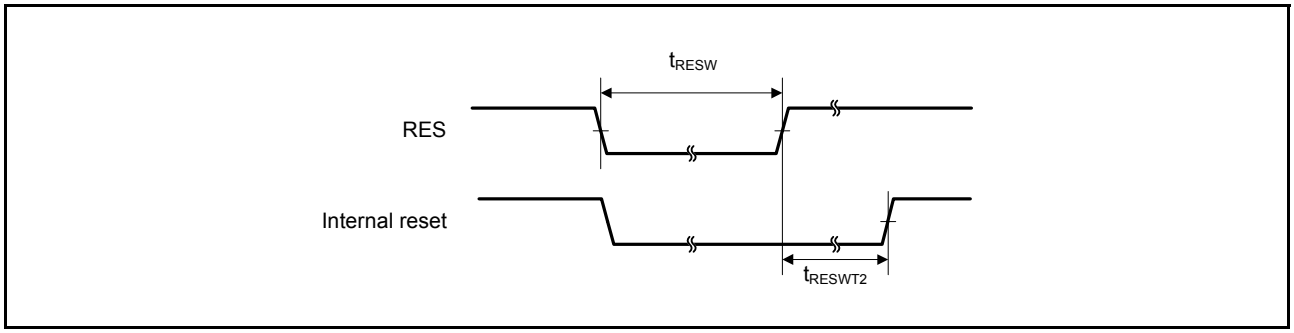


Figure 2.33 Reset input timing (1)

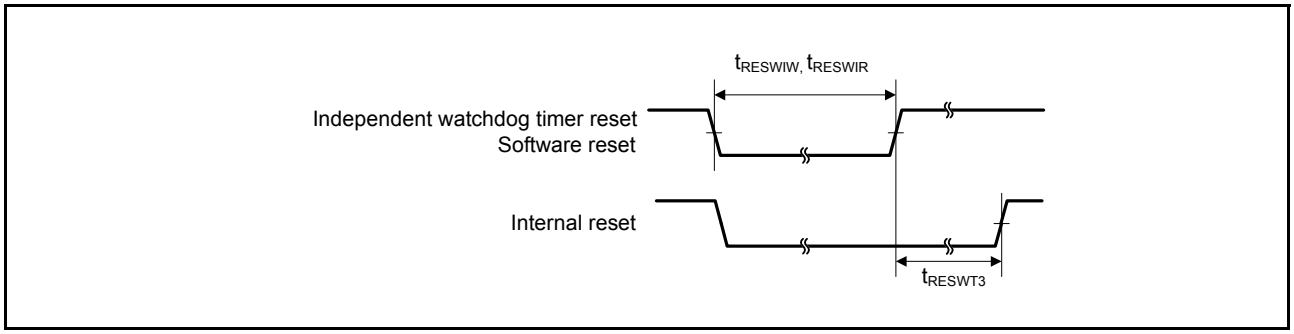


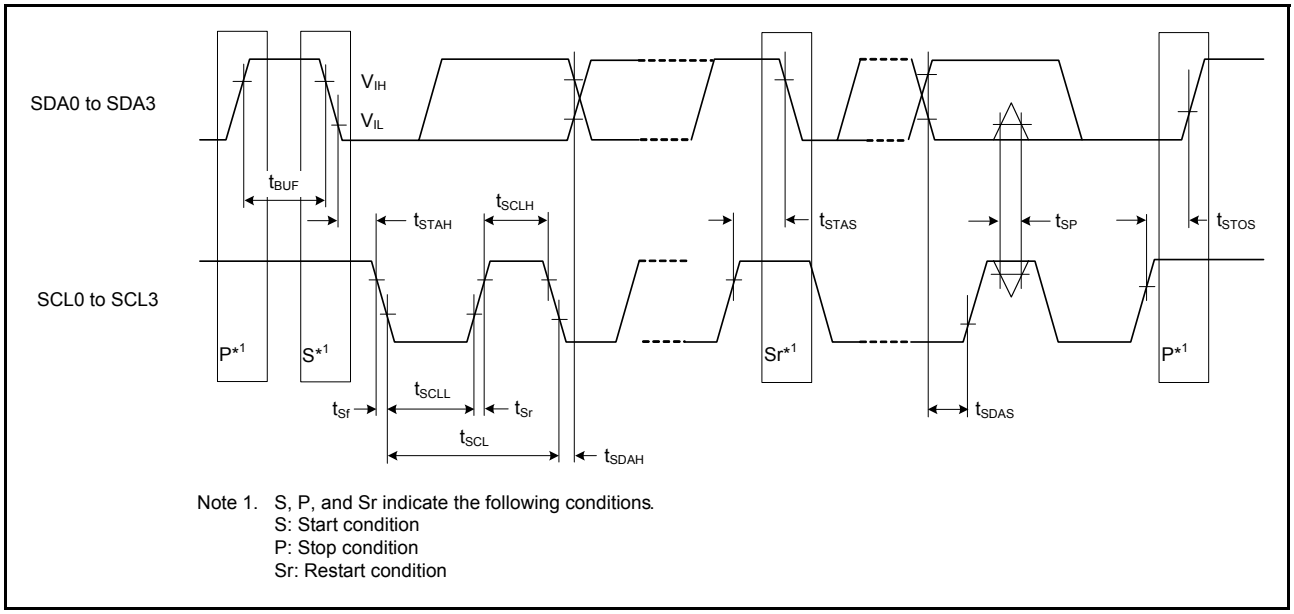
Figure 2.34 Reset input timing (2)

2.3.12 IIC Timing

Table 2.42 IIC timing
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Item		Symbol	Min*1, *2	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.66
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.66
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.66 I²C bus interface input/output timing

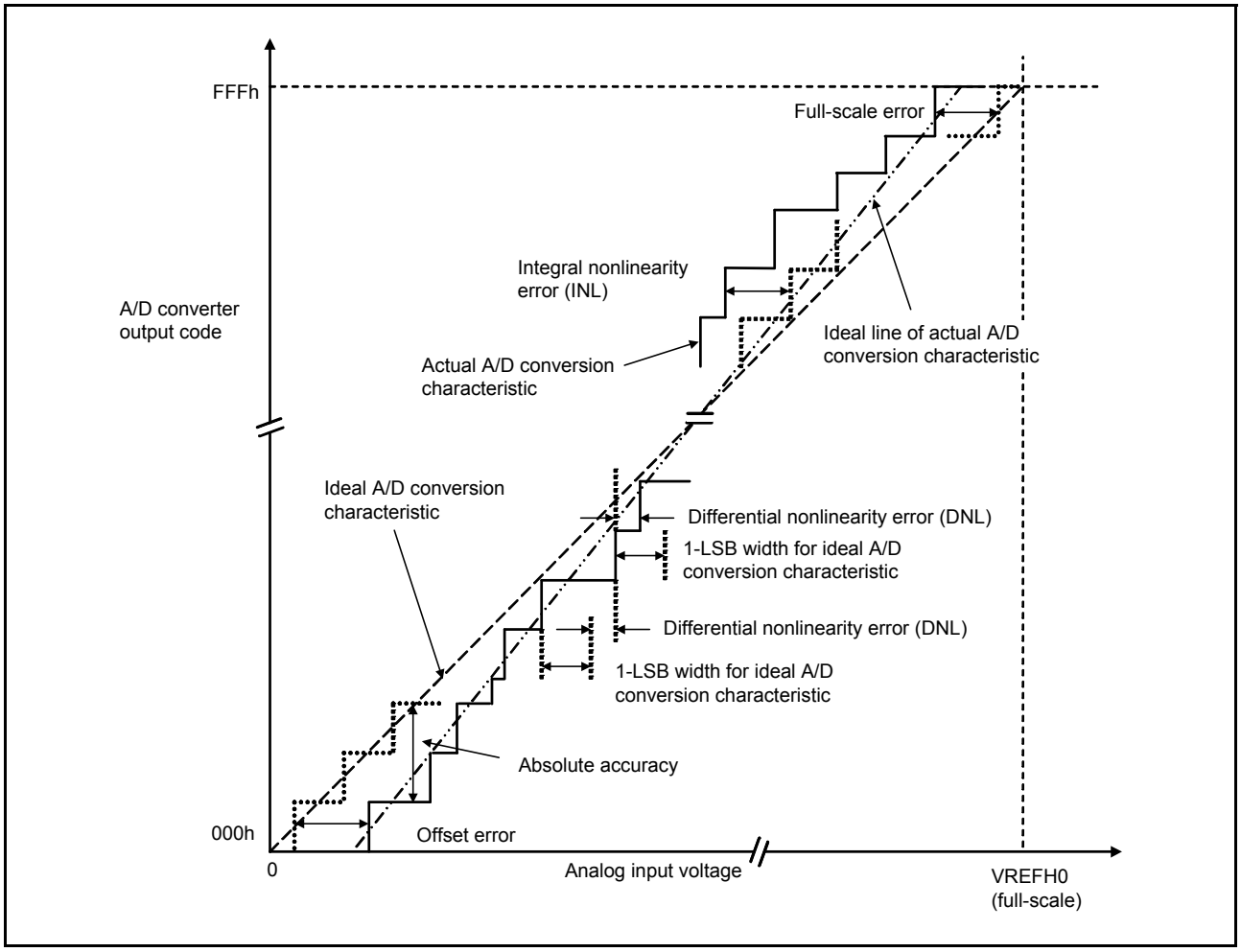


Figure 2.77 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.7 TSN Characteristics

Table 2.60 TSN characteristics
Conditions: VCC = AVCC0 = 2.0 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
	-	-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	–3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	-	-	5	µs	-
Sampling time	-	5	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.61 Oscillation stop detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.79

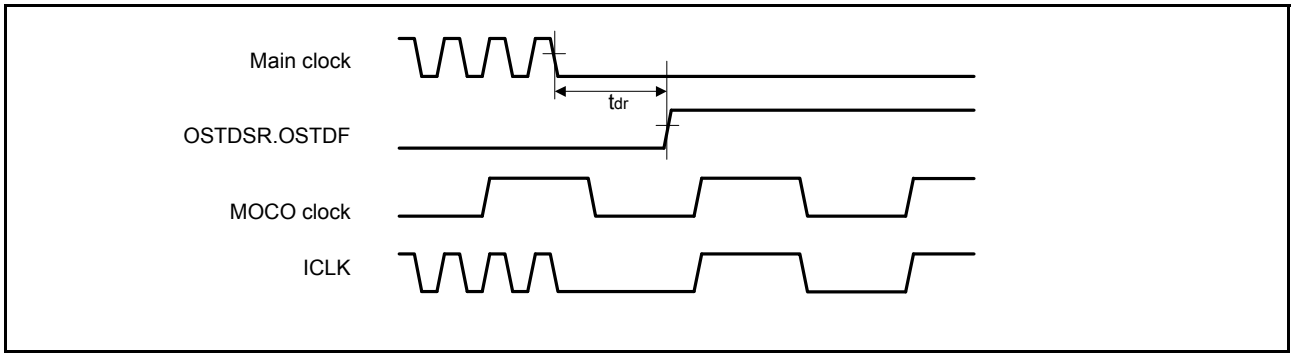
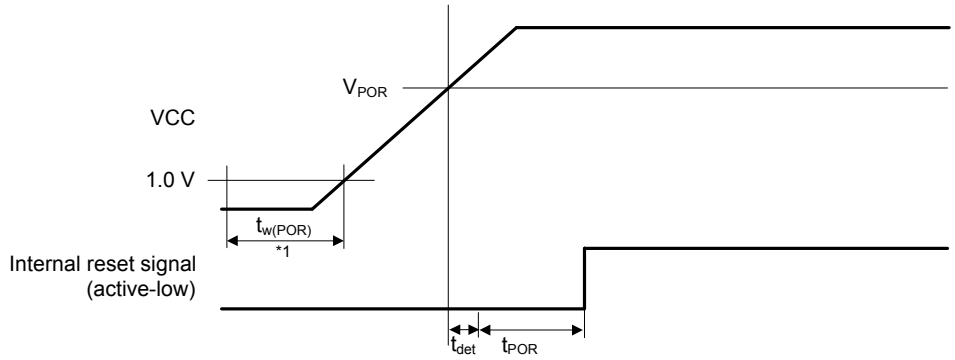


Figure 2.79 Oscillation stop detection timing



Note: $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(por)}$ for 1.0 ms or more.

Figure 2.81 Power-on reset timing

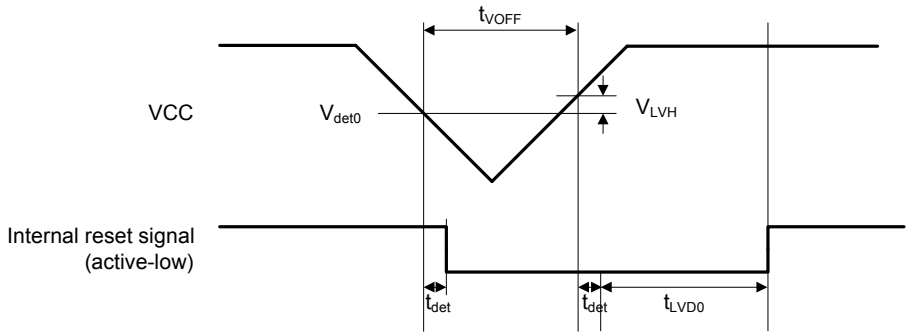


Figure 2.82 Voltage detection circuit timing (V_{det0})

2.12 Segment LCD Controller/Driver Characteristics

2.12.1 Resistance Division Method

[Static Display Mode]

Table 2.66 Resistance division method LCD characteristics (1)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 2.67 Resistance division method LCD characteristics (2)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 2.68 Resistance division method LCD characteristics (3)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

2.12.2 Internal Voltage Boosting Method

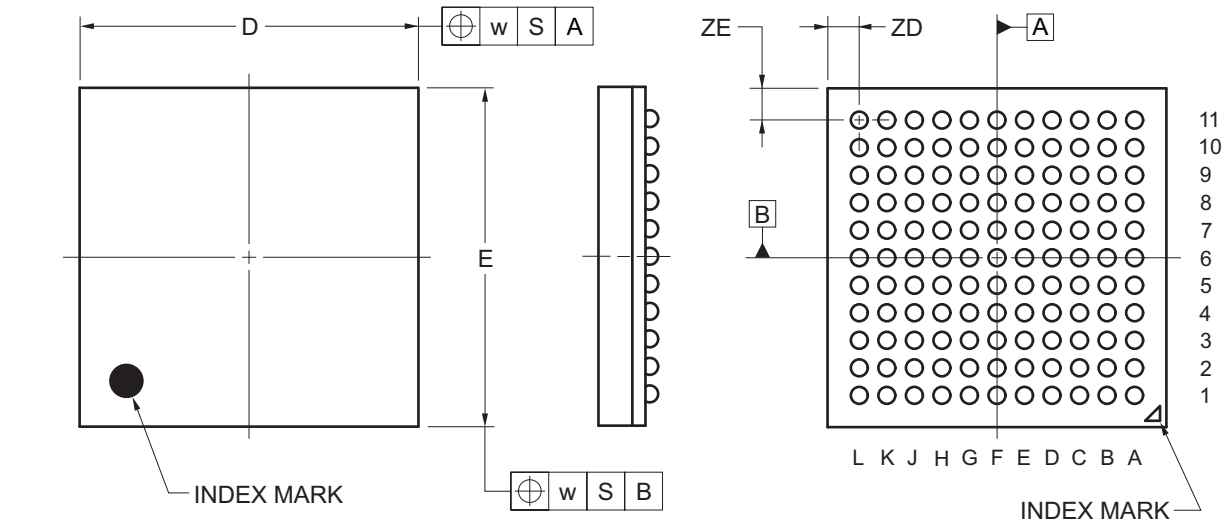
[1/3 Bias Method]

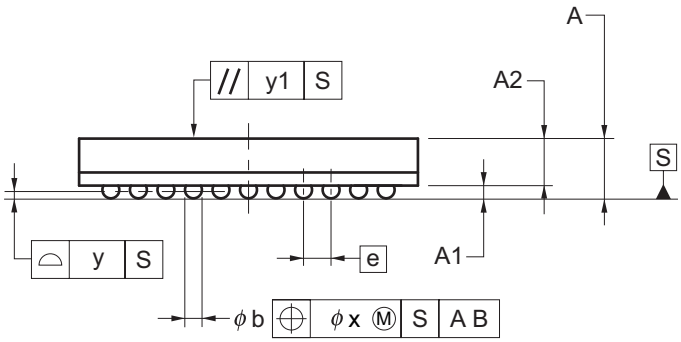
Table 2.69 Internal voltage boosting method LCD characteristics
Conditions: VCC = AVCC0 = 1.8 V to 5.5 V

Item	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
			VLCD = 0Dh	1.35	1.45	1.53	V	-
			VLCD = 0Eh	1.40	1.50	1.58	V	-
			VLCD = 0Fh	1.45	1.55	1.63	V	-
			VLCD = 10h	1.50	1.60	1.68	V	-
			VLCD = 11h	1.55	1.65	1.73	V	-
			VLCD = 12h	1.60	1.70	1.78	V	-
			VLCD = 13h	1.65	1.75	1.83	V	-
Doubler output voltage	V_{L2}	C1 to C4*1 = 0.47 µF		$2 \times V_{L1}$ - 0.1	$2 \times V_{L1}$	$2 \times V_{L1}$	V	-
Tripler output voltage	V_{L4}	C1 to C4*1 = 0.47 µF		$3 \times V_{L1}$ - 0.15	$3 \times V_{L1}$	$3 \times V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.88
LCD output voltage variation range*3	t_{VLWT}	C1 to C4*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
-	PLBG0121JA-A	P121F1-65-CAH	-





(UNIT: mm)

ITEM	DIMENSIONS
D	8.00±0.10
E	8.00±0.10
w	0.20
A	1.21±0.10
A1	0.30±0.05
A2	0.91
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.75
ZE	0.75

Figure 1.3 BGA 121-pin