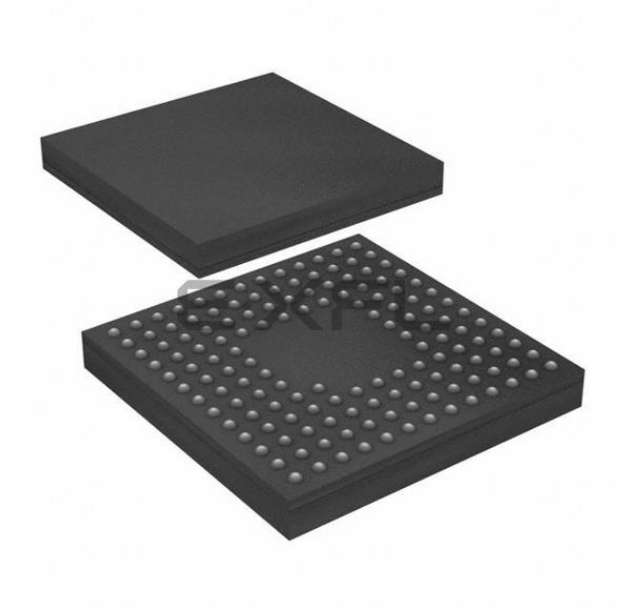
Renesas Electronics America Inc - R7FS3A77C2A01CLK#AC1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	124
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 28x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c2a01clk-ac1

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1, SSLA2, SSLA3, SSLB1, SSLB2, SSLB3	Output	Output pin for slave selection.
QSPI	QSPCLK	Output	QSPI clock output pin.
	QSSL	Output	QSPI slave output pin.
	QIO0	I/O	Master transmit data/data 0.
	QIO1	I/O	Master input data/data 1.
	QIO2, QIO3	I/O	Data 2, Data 3.
CAN	CRX0	Input	Receive data.
	CTX0	Output	Transmit data.
USBFS	VSS_USB	Input	Ground pins.
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator.
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	External overcurrent detection signals should be connected to these pins. VBUS comparator signals should be connected to these pins when the OTG power supply chip is connected.
	USB_ID	Input	MicroAB connector ID input signal should be connected to this pin during operation in OTG mode.
SDHI	SD0CLK	Output	SD clock output pin.
	SD0CMD	I/O	SD command output, response input signal pin.
	SD0DAT0 to SD0DAT7	I/O	SD data bus pins.
	SD0WP	Input	SD write-protect signal.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the analog. Connect this pin to VCC.
	AVSS0	Input	Analog ground pin. Connect this pin to VSS.
	VREFH0	Input	Analog reference voltage supply pin for the A/D converter. Connect this pin to VCC when not using the A/D converter.
	VREFL0	Input	Analog reference ground pin for the A/D converter. Connect this pin to VSS when not using the A/D converter.
	VREFH	Input	Analog reference voltage supply pin for D/A converter.
	VREFL	Input	Analog reference ground pin for D/A converter.
ADC14	AN000 to AN027	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active LOW.
DAC12	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
Comparator output	VCOUT	Output	Comparator output pin.
ACMPHS	IVREF0 to IVREF5	Input	Reference voltage input pin.
	IVCMP0 to IVCMP5	Input	Analog voltage input pin.
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pin.
	CMPIN0, CMPIN1	Input	Analog voltage input pins.

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	A	B	C	D	E	F	G	H	J	K	L	
11	P407	P408	P411	P414	P212/ EXTAL	P215/ XCIN	VCL	P406	P403	P401	P400	11
10	USB_DM	USB_DP	P410	P415	P213/ XTAL	P214/ XCOUT	VBATT	P405	P402	P511	P512	10
9	VCC_ USB	VSS_ USB	P409	P412	P708	VCC	VSS	P404	P002	P001	P000	9
8	P205	VCC_ USB_ LDO	P206	P204	P413	P710	P702	P006	P004	P003	P005	8
7	P203	P202	P313	P314	P315	P709	P701	P007	AVSS0	P011/ VREFL0	P010/ VREFH0	7
6	VSS	VCC	RES	P201/MD	P200	NC	P700	P008	AVCC0	P013/ VREFL	P012/ VREFH	6
5	P308	P309	P307	P302	P304	P612	P601	P506	P505	P015	P014	5
4	P305	P306	P808	P114	P611	P603	P600	P504	P503	VSS	VCC	4
3	P809	P303	P110/TDI	P111	P609	P604	P106	P104	P502	P500	P501	3
2	P301	P108/ TMS/ SWDIO	P113	P608	P613	P605	P602	P105	P102	P801	P800	2
1	P300/ TCK/ SWCLK	P109/ TDO/ SWO	P112	P115	P610	VCC	VSS	P107	P103	P101	P100	1
	A	B	C	D	E	F	G	H	J	K	L	

Figure 1.5 Pin assignment for BGA 121-pin (Upper perspective view)

Pin number										Timers				Communication interfaces						Analogs			HMI		
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64	Power, System, Clock, Debug, CAC, VBATT	I/O ports	External bus	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSI	SDHI	ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	SLCDC	CTSU	Interrupt
D11	32	C11	21	D8	12	12		P411		AGTOA1	GTOVUP_B	GTIOC9A_A			TXD0_B/MOSI0_B/SDA0_B/CTS3_RTS3_A/SS3_A		MOSIA_B		SD0DAT0					TS07	IRQ4
C12	33	C10	22	E6	13	13		P410		AGTOB1	GTOVLO_B	GTIOC9B_A			RXD0_B/MISO0_B/SCL0_B/SCK3_A		MISOA_B		SD0DAT1					TS06	IRQ5
B13	34	C9	23	B10	14	14		P409			GTOWUP_B			USB_EXICEN_A	TXD3_A/MOSI3_A/SDA3_A									TS05	IRQ6
D10	35	B11	24	D7	15	15		P408			GTOWLO_B			USB_ID_A	RXD3_A/MISO3_A/SCL3_A									TS04	IRQ7
A13	36	A11	25	A10	16	16		P407					RTCOUT	USB_VBUS	CTS4_RTS4_A/SS4_A	SDA0_B	SSLB3_A			ADTRG0_B				TS03	
B11	37	B9	26	B8	17	17	VSS_USB																		
A12	38	A10	27	A9	18	18								USB_DM											
B12	39	B10	28	B9	19	19								USB_DP											
A11	40	A9	29	A8	20	20	VCC_USB																		
C11	41	B8	30	C8	21	21	VCC_USB_LDO																		
B10	42	C8	31	C7	22	22		P206	WAIT		GTIU_A			USB_VBUSEN_A	RXD4_A/MISO4_A/SCL4_A	SDA1_A	SSLB1_A	SSIDATA1_A	SD0DAT2					TS01	IRQ0
A10	43	A8	32	A7	23	23	CLKOUT_A	P205	A16	AGTO1	GTIV_A	GTIOC4A_B		USB_OVRCURA	TXD4_A/MOSI4_A/SDA4_A/CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A	SSIWS1_A	SD0DAT3					TSCAP_A	IRQ1
C10	44	D8	33	B7	24	24	CACREF_A	P204		AGTIO1_A	GTIW_A	GTIOC4B_B		USB_OVRCURB	SCK4_A/SCK9_A	SCL0_B	RSPCKB_A	SSISCK1_A	SD0DAT4				SEG23	TS00	
A9	45	A7	34	D6				P203				GTIOC5A_A		CTX0_A	CTS2_RTS2_A/SS2_A/TXD9_A/MOSI9_A/SDA9_A		MOSIB_A		SD0DAT5				SEG22	TSCAP_B	IRQ2
C9	46	B7	35	C6				P202	WR1/BC1			GTIOC5B_A		CRX0_A	SCK2_A/RXD9_A/MISO9_A/SCL9_A		MISOB_A		SD0DAT6				SEG21		IRQ3
B9	47	C7						P313											SD0DAT7				SEG20		
D9	48	D7						P314															SEG4		
D8	49	E7						P315															SEG5		
A8	50							P900															SEG6		
B8	51							P901															SEG7		
B7	52							P902															SEG8		
A7	53	A6	36	A6			VSS																		
A6	54	B6	37	B6			VCC																		
C7	55	C6	38	D5	25	25	RES																		
B6	56	D6	39	B5	26	26	MD	P201																	
C8	57	E6	40	A5	27	27		P200																	NMI
C6	58							P312	CS3														SEG9		

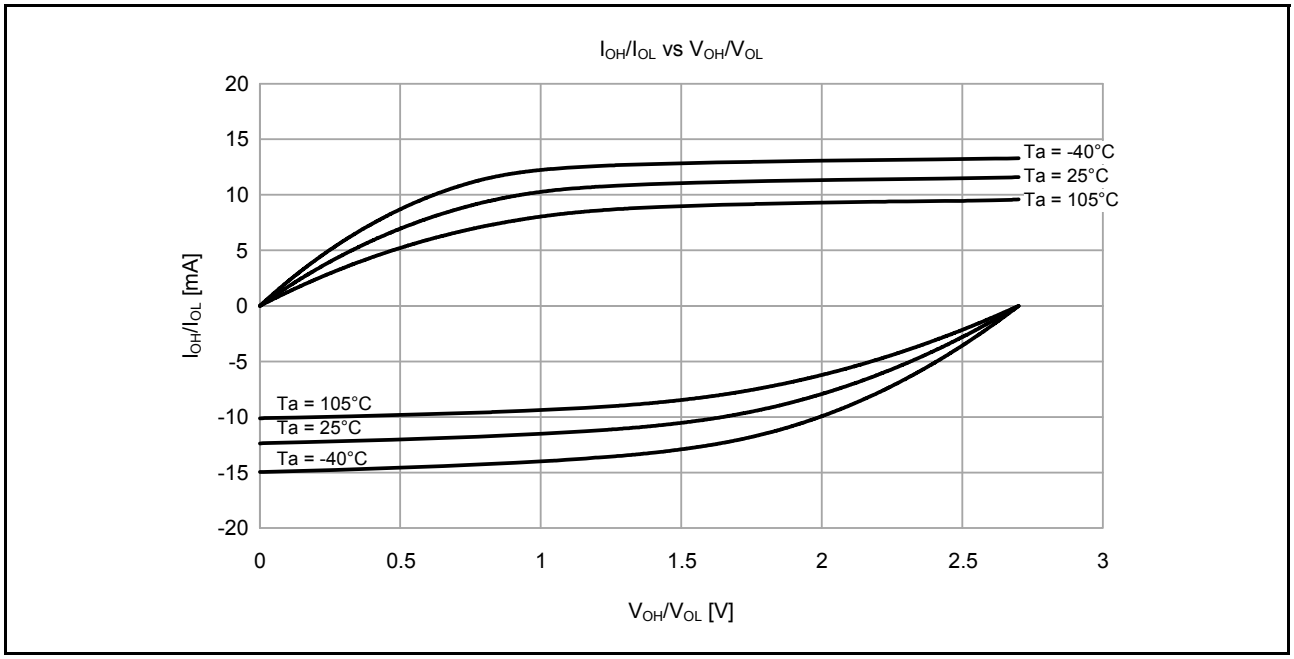


Figure 2.4 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Low drive output is Selected (Reference Data)**

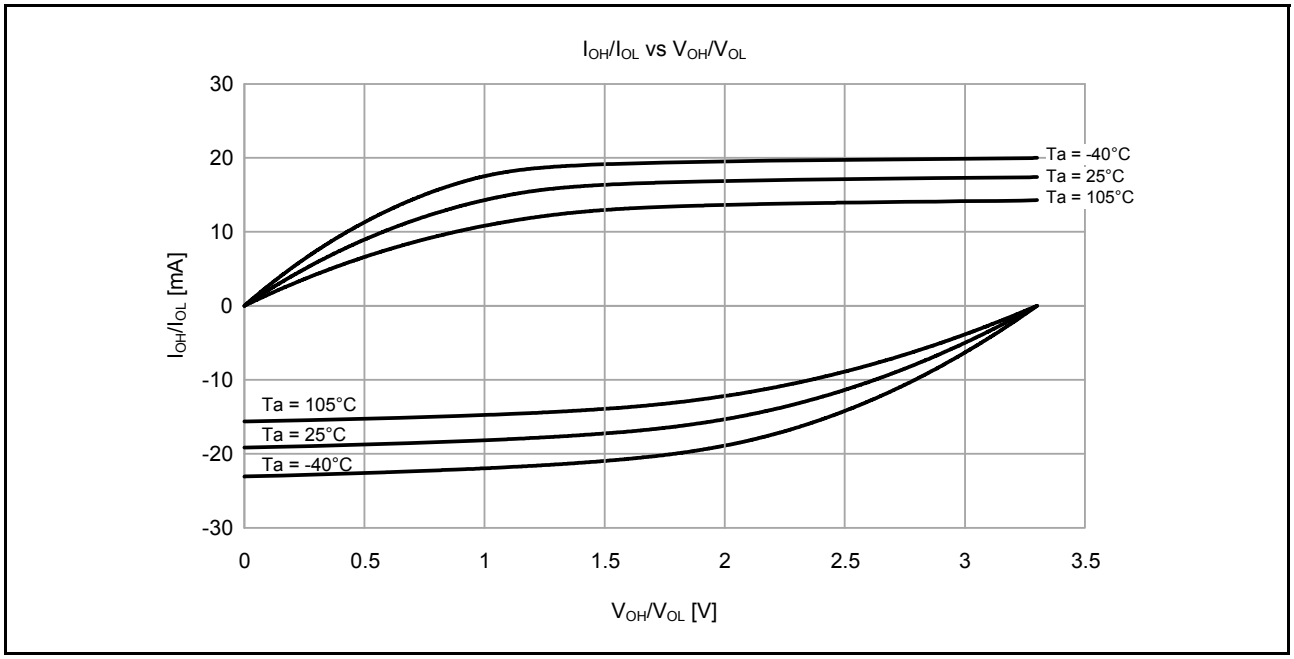


Figure 2.5 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Low drive output is Selected (Reference Data)**

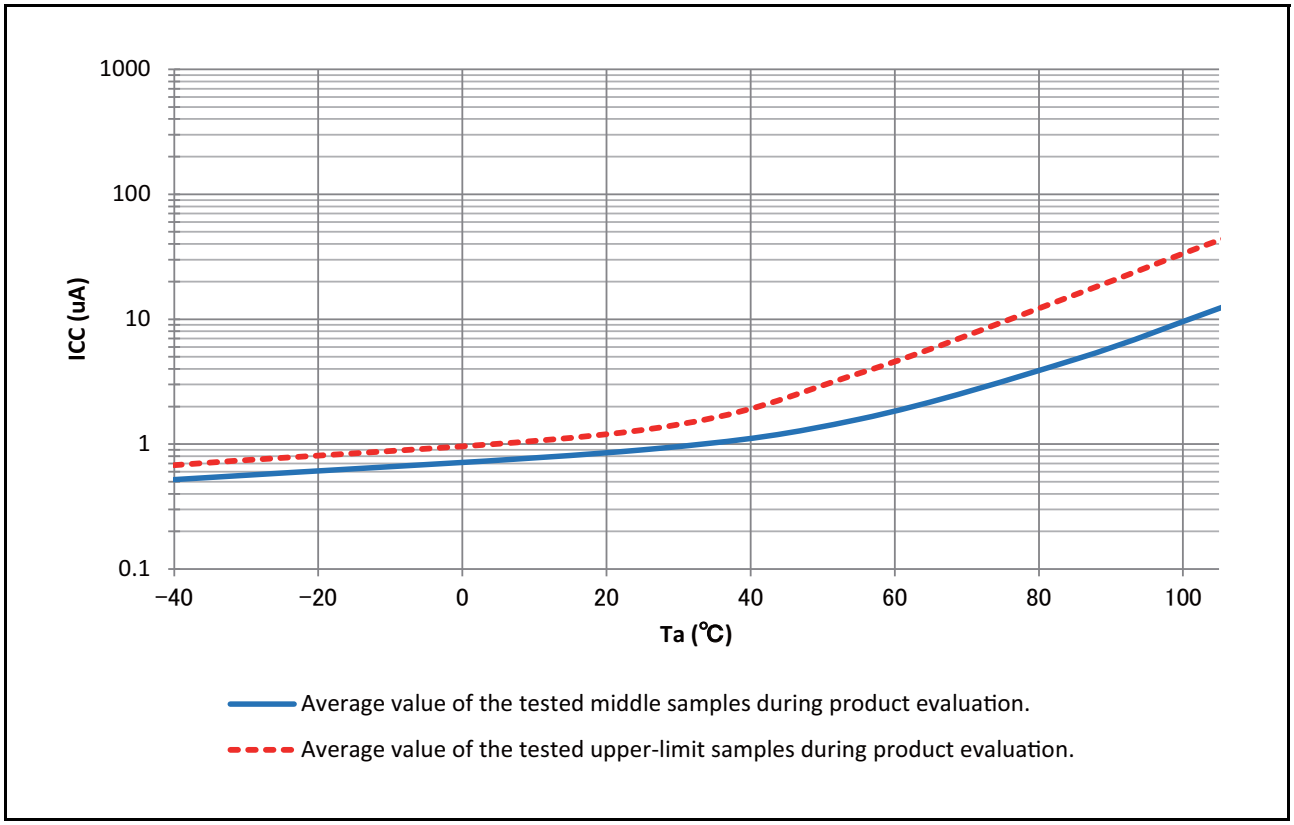


Figure 2.22 Temperature dependency in Software Standby mode 48-KB SRAM on (reference data)

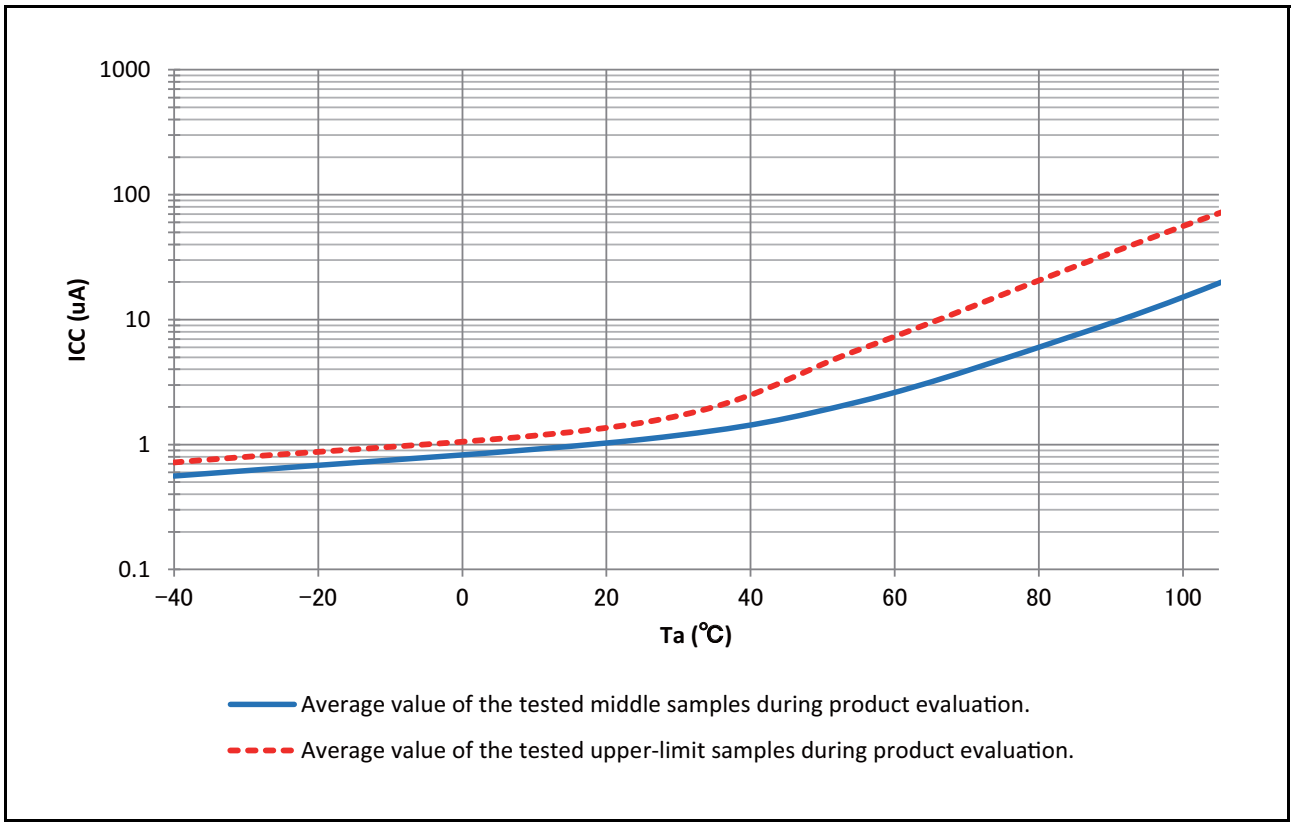


Figure 2.23 Temperature dependency in Software Standby mode all SRAM on (reference data)

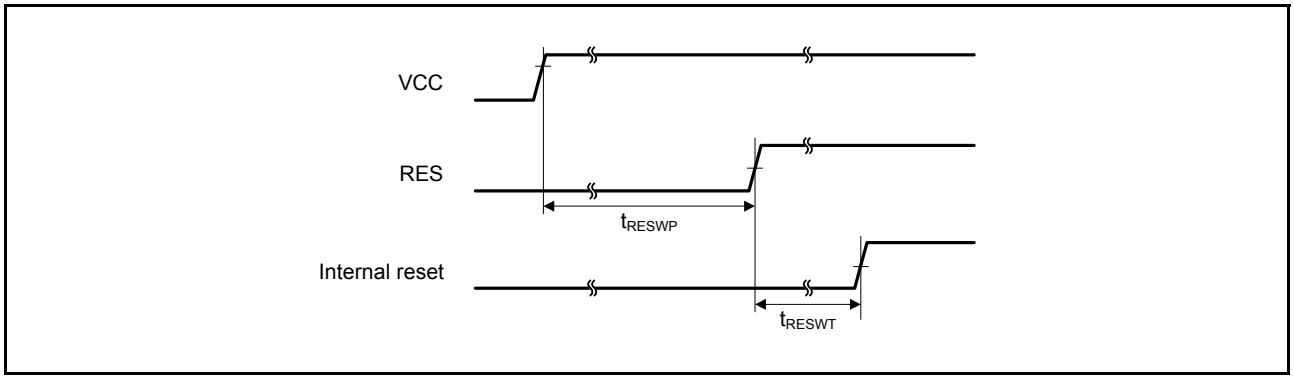


Figure 2.32 Reset input timing at power-on

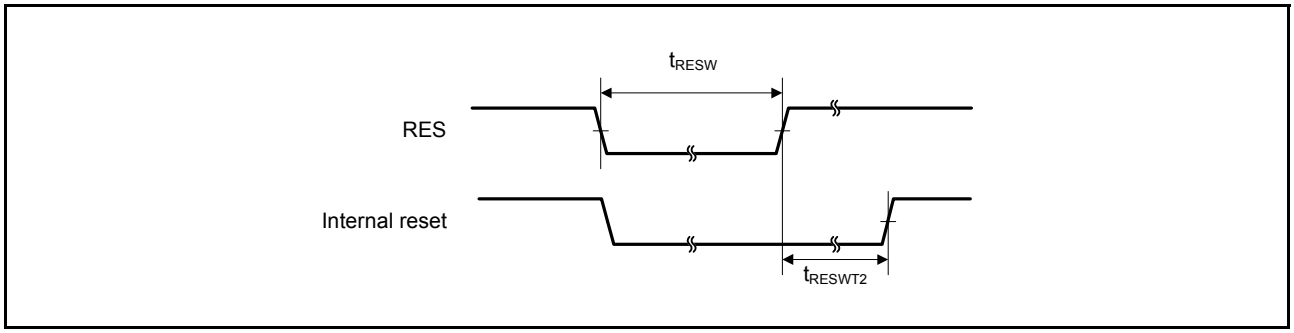


Figure 2.33 Reset input timing (1)

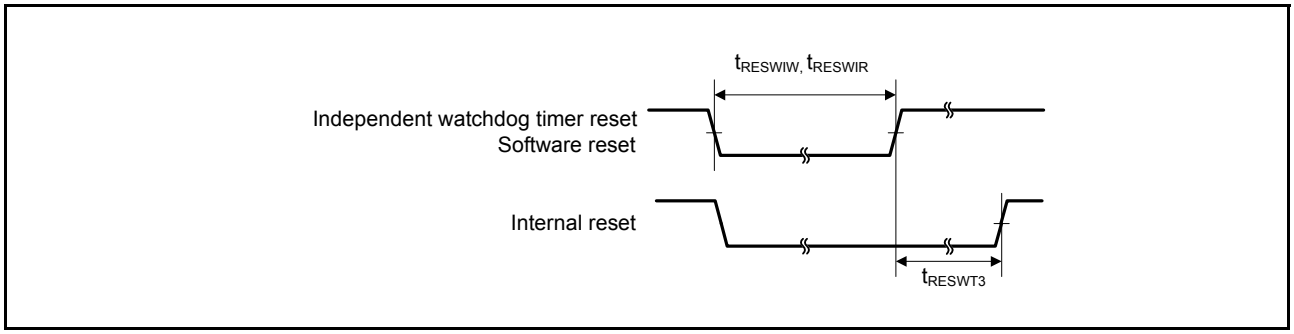


Figure 2.34 Reset input timing (2)

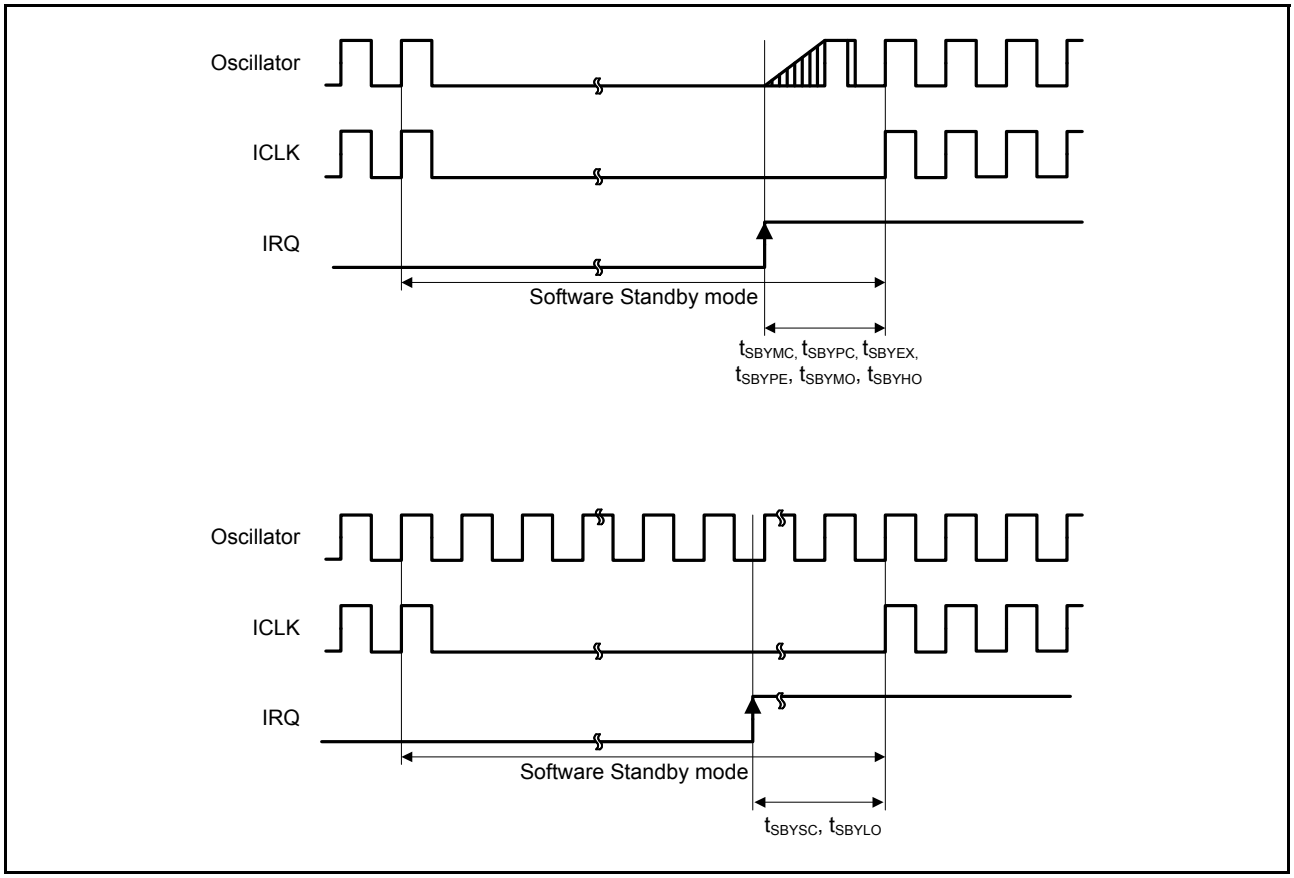


Figure 2.35 Software Standby mode cancellation timing

Table 2.29 Timing of recovery from low power modes (6)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	µs	-
	Middle-speed mode System clock source is MOCO (8 MHz)	t_{SNZ}	-	1.3	3.6	µs	
	Low-speed mode System clock source is MOCO (1 MHz)	t_{SNZ}	-	10	13	µs	
	Low-voltage mode System clock source is HOCO (4 MHz)	t_{SNZ}	-	87	110	µs	

2.3.5 NMI and IRQ Noise Filter

Table 2.30 NMI and IRQ noise filter

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 15).

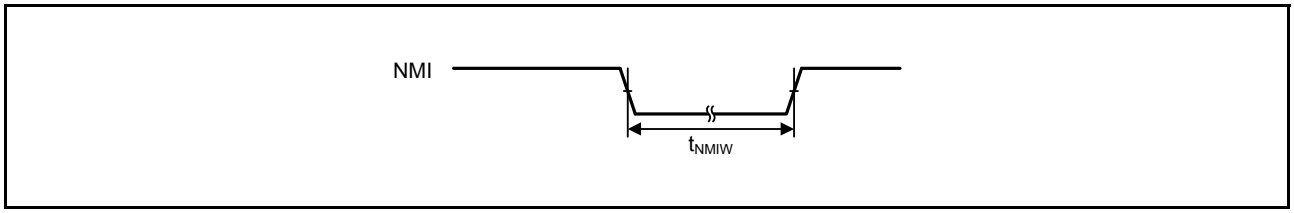


Figure 2.36 NMI interrupt input timing

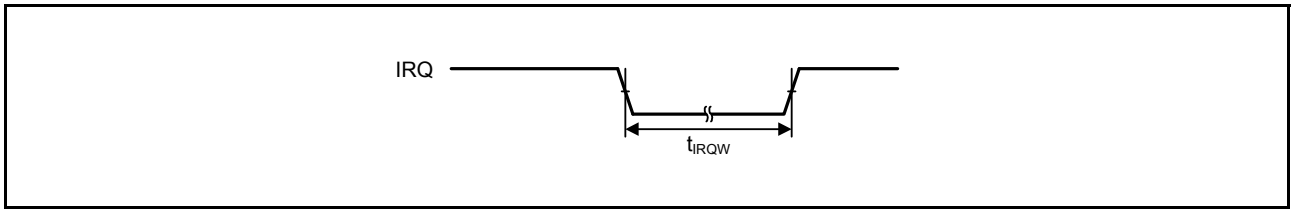


Figure 2.37 IRQ interrupt input timing

Table 2.33 Bus timing (3)

Conditions: EBCLK pin ≤ 4 MHz (package with 145 to 100 pins) (BCLK: up to 4 MHz)
VCC = AVCC0 = 1.8 to 2.4 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
WAIT setup time	t_{WTS}	70	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.34 Bus timing (4)

Conditions: EBCLK pin ≤ 2 MHz (package with 145 to 100 pins) (BCLK: up to 2 MHz)
VCC = AVCC0 = 1.6 to 1.8 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	120	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	120	ns	
CS delay	t_{CSD}	-	120	ns	
RD delay	t_{RSD}	-	120	ns	
Read data setup time	t_{RDS}	90	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	120	ns	
Write data delay	t_{WDD}	-	120	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	90	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

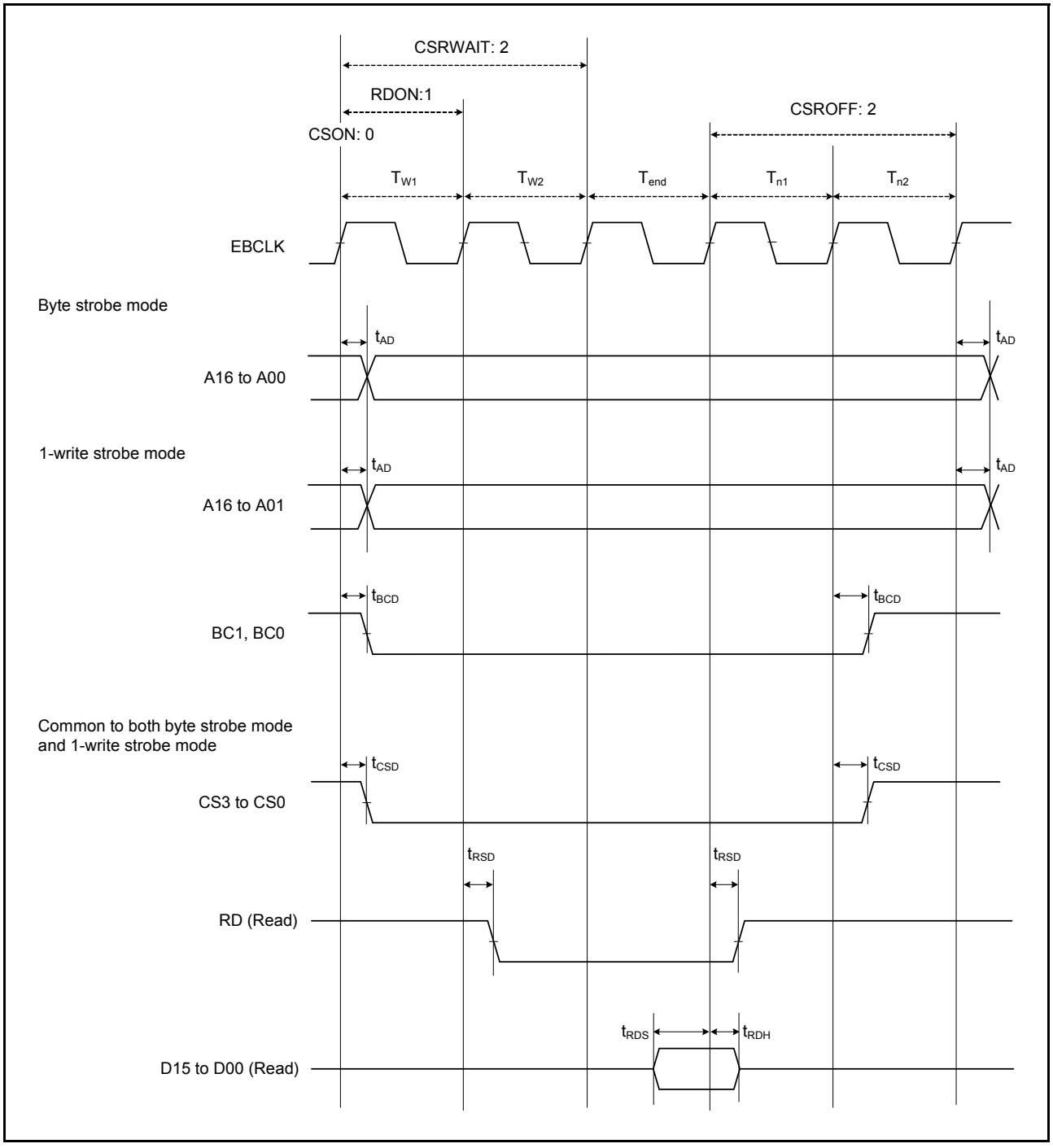


Figure 2.38 External bus timing/normal read cycle (bus clock synchronized)

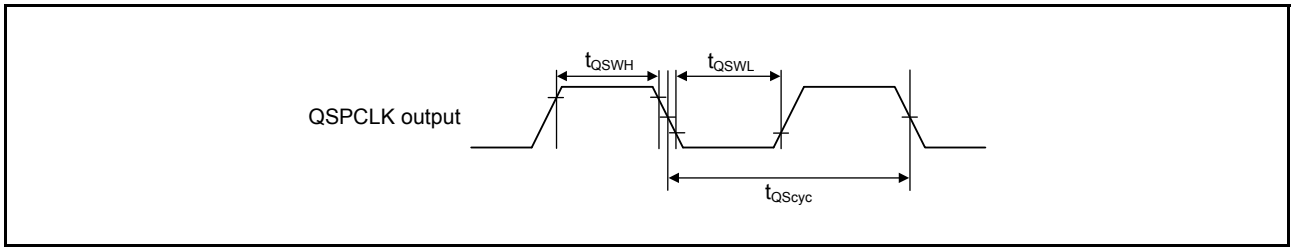


Figure 2.64 QSPI clock timing

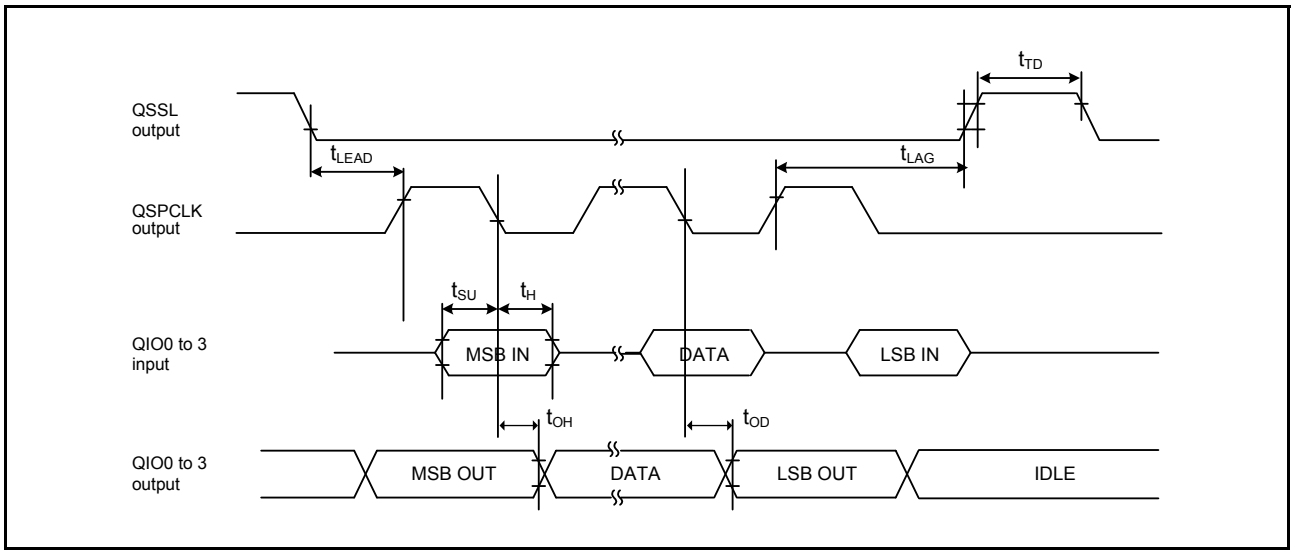


Figure 2.65 Transfer/receive timing

2.3.13 SSI Timing

Table 2.43 SSI timing
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item			Symbol	Min	Max	Unit	Test conditions
SSI	AUDIO_CLK input frequency	2.7 V or above	t_{AUDIO}	-	25	MHz	-
		1.6 V or above		-	4		
	Output clock period		t_O	250	-	ns	Figure 2.67
	Input clock period		t_I	250	-	ns	
	Clock high pulse width	1.8 V or above	t_{HC}	100	-	ns	
		1.6 V or above		200	-		
	Clock low pulse width	1.8 V or above	t_{LC}	100	-	ns	
		1.6 V or above		200	-		
	Clock rise time		t_{RC}	-	25	ns	
	Data delay	2.7 V or above	t_{DTR}	-	65	ns	Figure 2.68, Figure 2.69
		1.8 V or above		-	105		
		1.6 V or above		-	140		
	Set-up time	2.7 V or above	t_{SR}	65	-	ns	
		1.8 V or above		90	-		
		1.6 V or above		140	-		
	Hold time		t_{HTR}	40	-	ns	
	SSIDATA output delay from WS change time	1.8 V or above	T_{DTRW}	-	105	ns	Figure 2.70
		1.6 V or above		-	140		

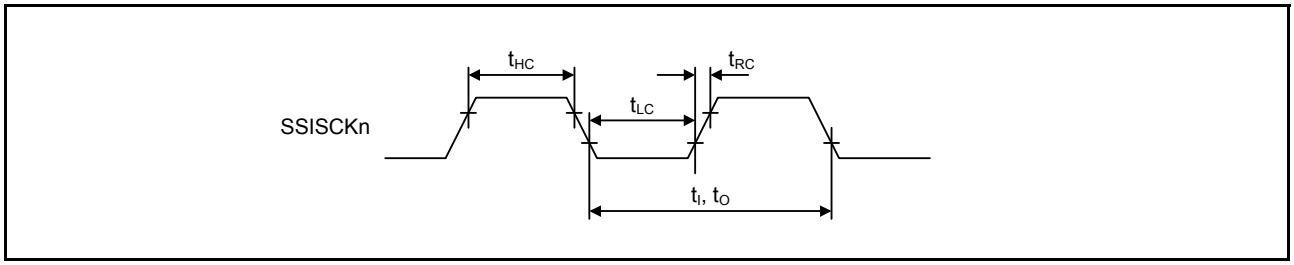


Figure 2.67 SSI clock input/output timing

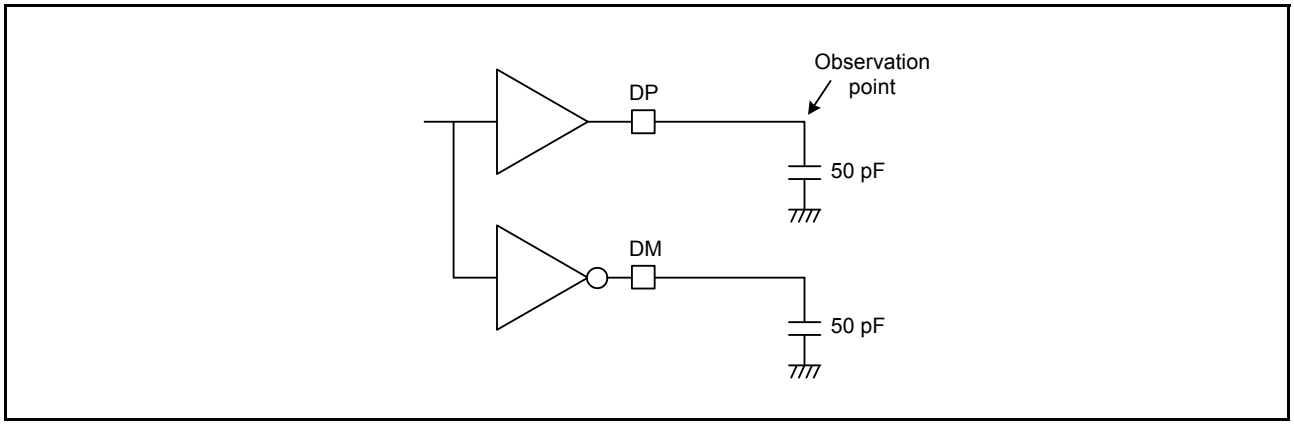


Figure 2.74 Test circuit for Full-Speed (FS) connection

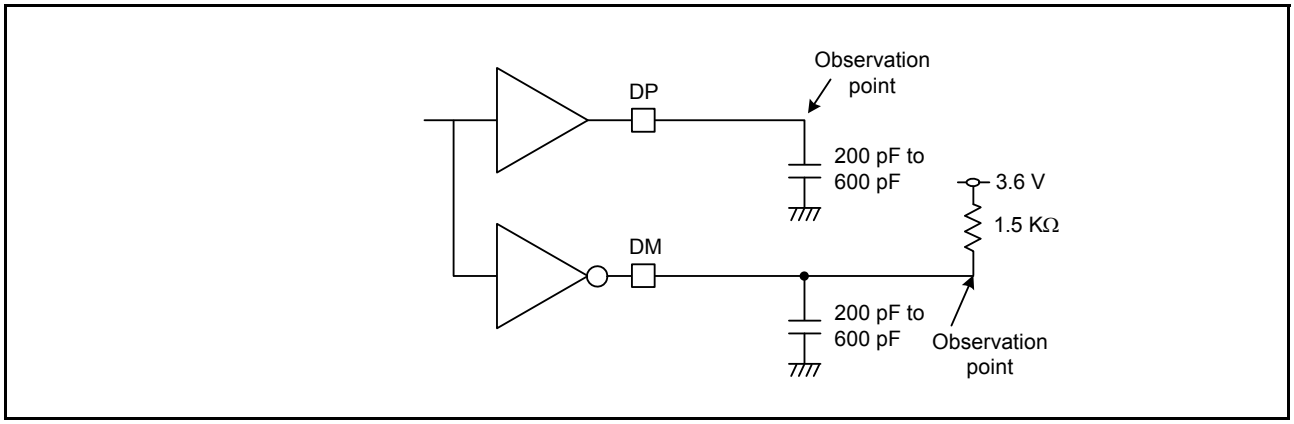


Figure 2.75 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.47 USB regulator

Item		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

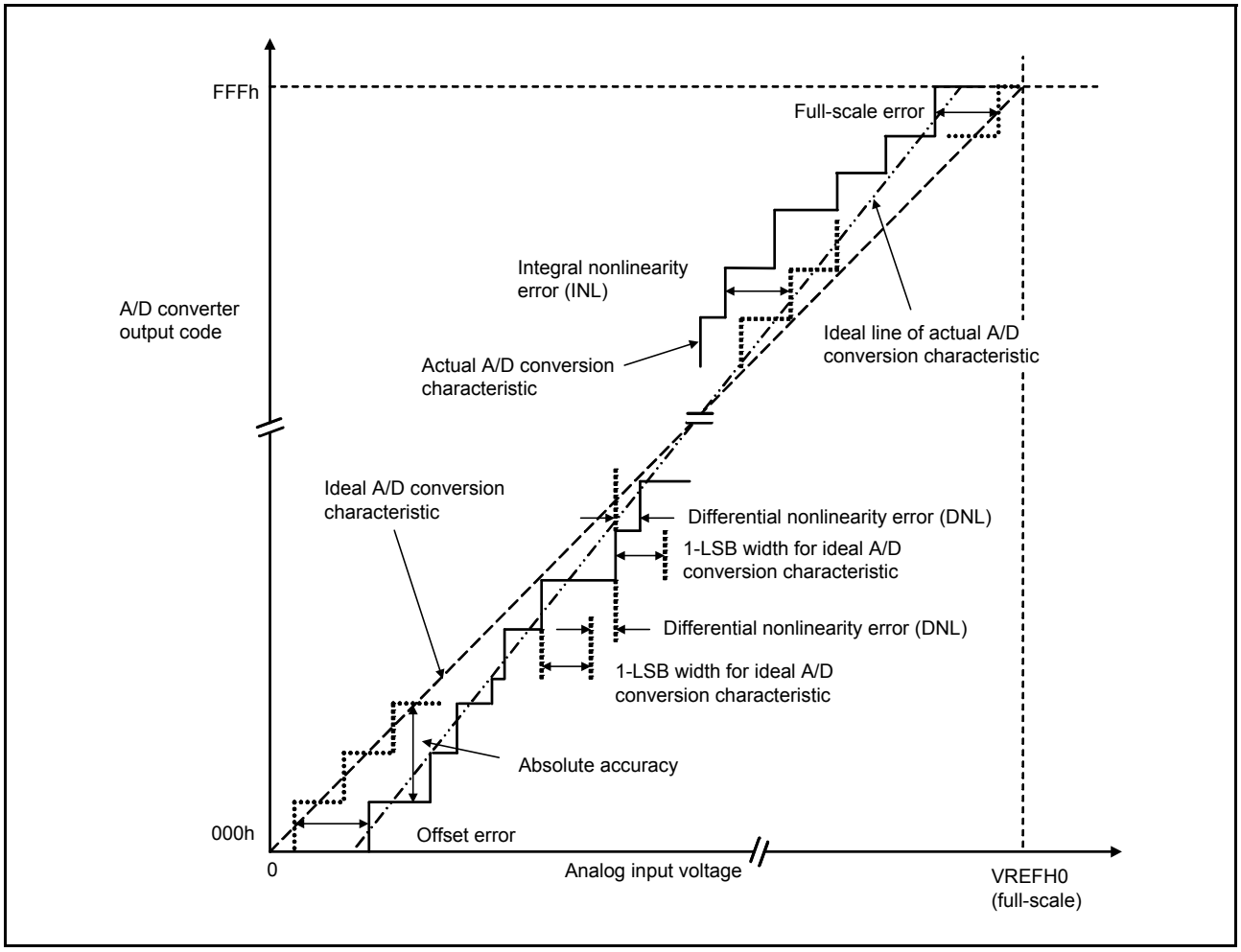


Figure 2.77 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.7 TSN Characteristics

Table 2.60 TSN characteristics
Conditions: VCC = AVCC0 = 2.0 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
	-	-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	–3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	-	-	5	µs	-
Sampling time	-	5	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.61 Oscillation stop detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.79

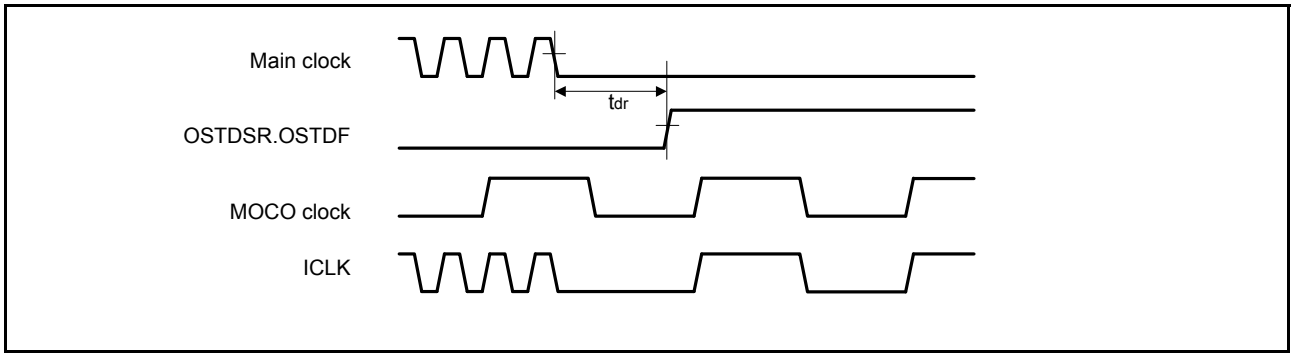


Figure 2.79 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.62 Power-on reset circuit and voltage detection circuit characteristics (1)
Conditions: VCC = AVCC0 = VCC_USB

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.80, Figure 2.81
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.82 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.83 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.84 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit (LVD2), it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol Vdet0_# denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.63 Power-on reset circuit and voltage detection circuit characteristics (2)
Conditions: VCC = AVCC0 = VCC_USB

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after voltage monitoring 0,1,2 reset cancellation	LVD0:enable*1	$t_{LVD0,1,2}$	-	0.6	-	µs	-
	LVD0:disable*2	$t_{LVD1,2}$	-	0.2	-	µs	-
Response delay*3		t_{det}	-	-	350	µs	Figure 2.80, Figure 2.81
Minimum VCC down time		t_{VOFF}	450	-	-	µs	Figure 2.80, VCC = 1.0 V or above
Power-on reset enable time		$t_{W (POR)}$	1	-	-	ms	Figure 2.81, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$T_{d (E-A)}$	-	-	300	µs	Figure 2.83, Figure 2.84
Hysteresis width (POR)		V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD1 and LVD2)		V_{LVH}	-	70	-	mV	V_{det1_0} to V_{det1_4} selected.
			-	60	-		V_{det1_5} to V_{det1_9} selected.
			-	50	-		V_{det1_A} or V_{det1_B} selected.
			-	40	-		V_{det1_C} or V_{det1_D} selected.
			-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, Vdet0, Vdet1, and Vdet2 for the POR/LVD.

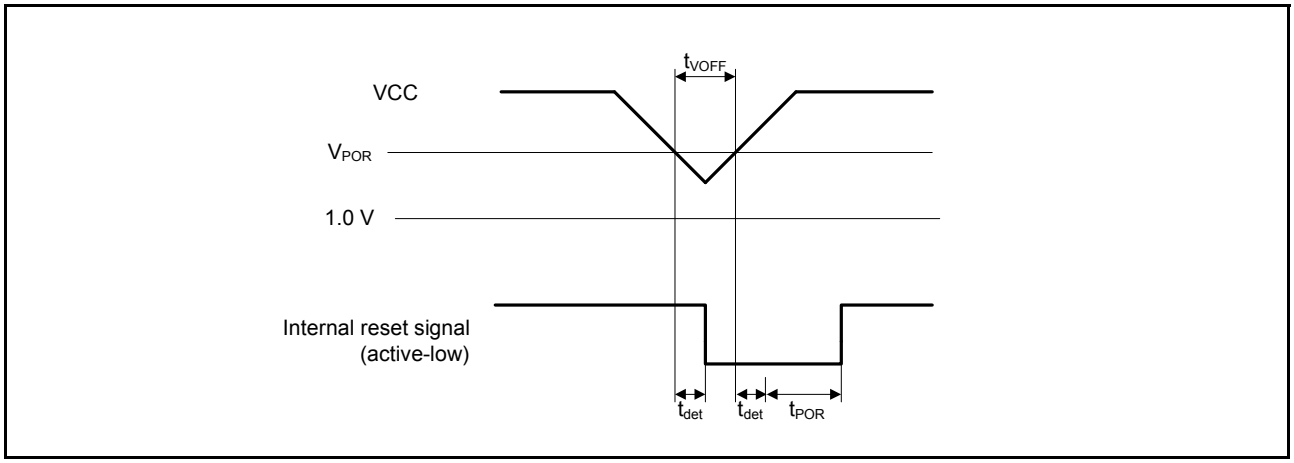


Figure 2.80 Voltage detection reset timing

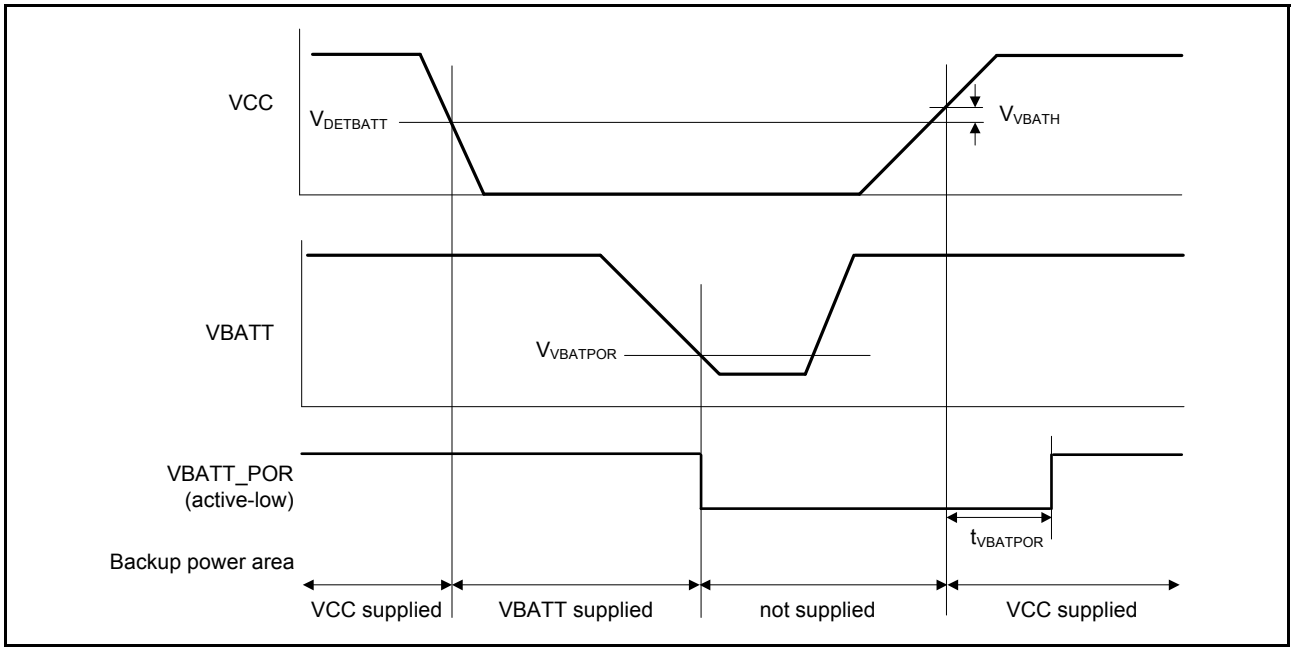


Figure 2.86 VBATT_POR Reset Timing

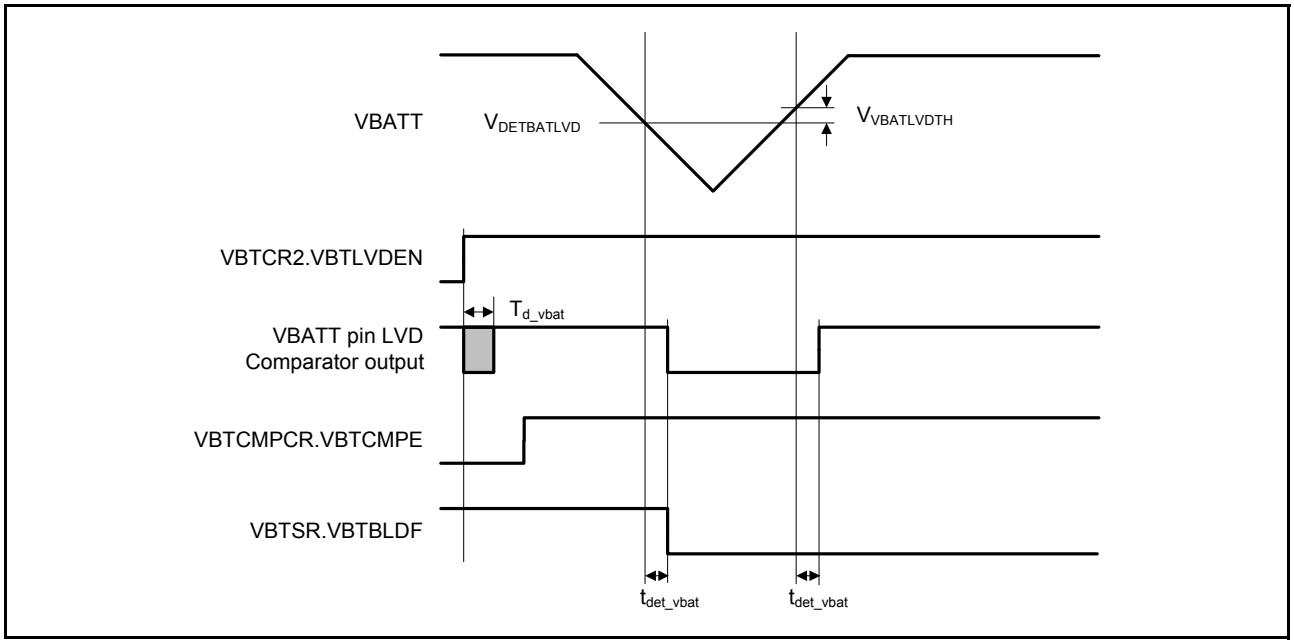


Figure 2.87 VBATT pin Voltage Detection Circuit Timing

2.11 CTSU Characteristics

Table 2.65 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

Table 2.80 Data flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = –40 to +85°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	94.7	886	-	87.0	837	µs
Erasure time	1-KB	t_{DE1K}	-	9.59	299	-	7.82	266	ms
Blank check time	1-byte	t_{DBC1}	-	-	56.2	-	-	50.9	µs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.21	ms
Suspended time during erasing		t_{DSED}	-	-	23.0	-	-	21.0	µs
Data flash STOP recovery time		t_{DSTOP}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.
Note 2. The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 3. The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

2.16 Boundary Scan

Table 2.81 Boundary scan
Conditions: VCC = AVCC = 2.4 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.89
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.90
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	70	ns	
Boundary Scan circuit start up time*1	t_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.91

Note 1. Boundary scan does not function until Power-On-Reset becomes negative.

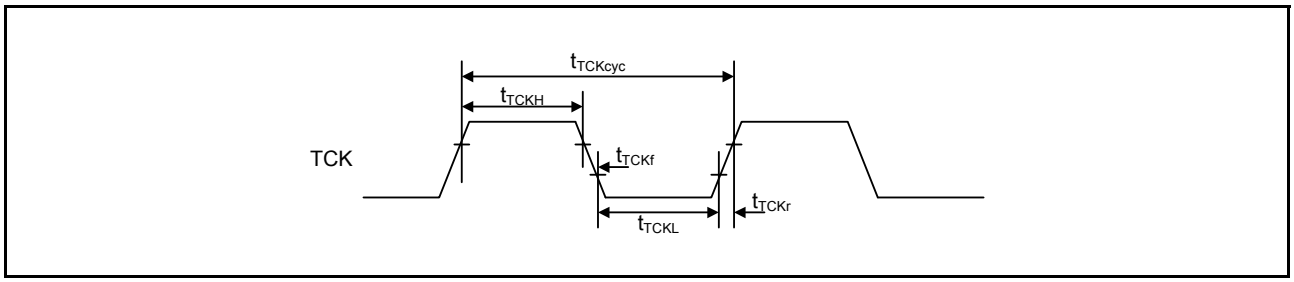
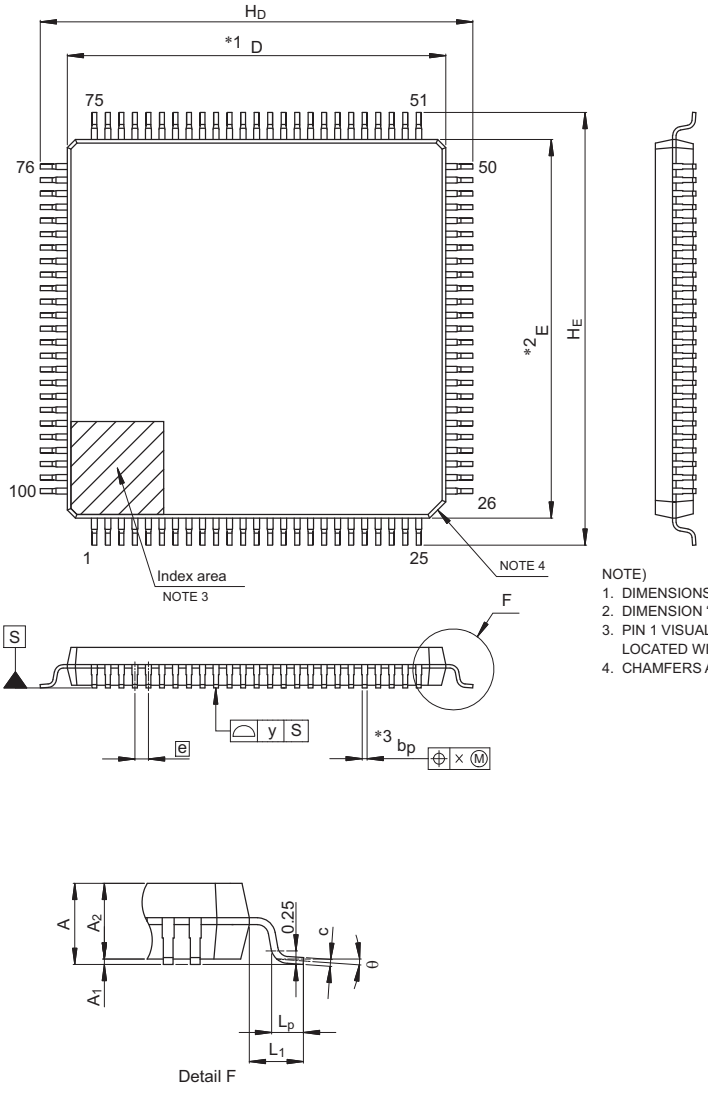


Figure 2.89 Boundary scan TCK timing

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 LQFP 100-pin