Renesas Electronics America Inc - R7FS3A77C3A01CFB#AA1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	124
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 28x14b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c3a01cfb-aa1

Table 1.3 System (2/2)

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset this MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 26, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The independent watchdog timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset this MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning this MCU to a known state as a fail safe mechanism when the system runs out of control. The watchdog timer can be triggered automatically on reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 27, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Interrupt control

Feature	Functional description
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.

Table 1.5 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.6 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	This MCU incorporates a Data Transfer Controller (DTC) that performs data transfers when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	This MCU incorporates an 4-channel DMA Controller (DMAC) module that can transfer data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.7 External bus interface

Feature	Functional description
External bus	• CS area: Connected to the external devices (external memory interface) • QSPI area: Connected to the QSPI (external device interface)

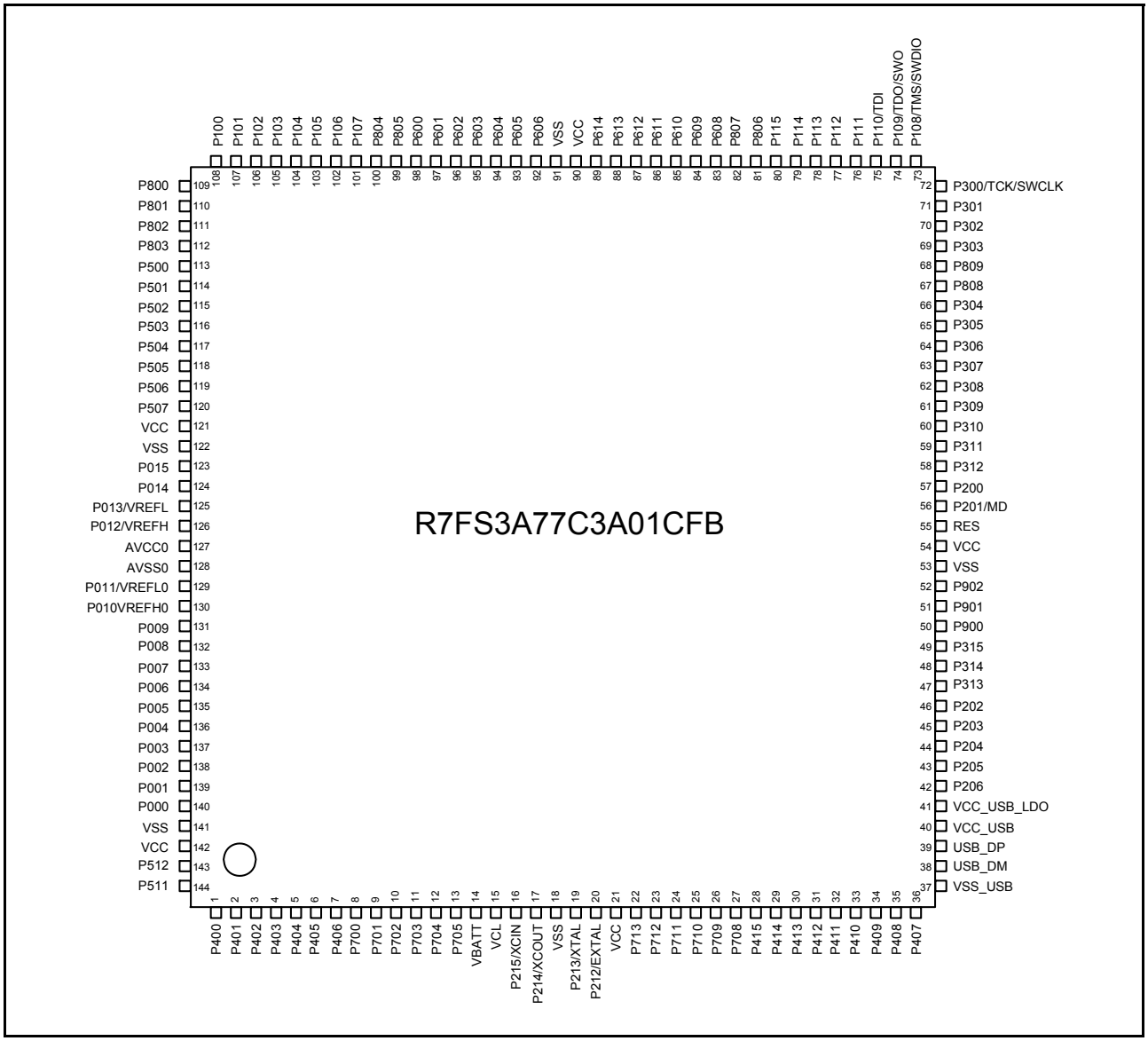


Figure 1.4 Pin assignment for LQFP 144-pin (Top view)

R7FS3A77C2A01CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	P215/ XCIN	VCL	P403	P400	P000	10
9	USB_DM	USB_DP	P413	VSS	P213/ XTAL	P214/ XCOUT	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	VCC_US B_LDO	P411	P415	P708	P404	P003	P004	P002	8
7	P205	P204	P206	P408	P414	P406	P006	P007	P008	P005	7
6	VSS	VCC	P202	P203	P410	P402	P505	AVSS0	P011/ VREFL0	P010/ VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	P013/ VREFL	P012/ VREFH	5
4	P305	P304	P808	P306	P115	P601	P503	P100	P015	P014	4
3	P809	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	P603	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO/ SWO	P112	P608	VCC	VSS	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.7 Pin assignment for LGA 100-pin (Upper perspective view)

Table 2.5 I/O V_{IH}, V_{IL} (2)

Conditions: VCC = 1.6 to 2.7 V, AVCC0 = 1.6 to 2.7 V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	VCC + 0.3	V	-
		V_{IL}	–0.3	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	–0.3	-	VCC × 0.2		
	P000 to P015	V_{IH}	AVCC0 × 0.8	-	AVCC + 0.3		
		V_{IL}	–0.3	-	AVCC0 × 0.2		
	EXTAL D0 to D15 Input ports pins except for P000 to P015	V_{IH}	VCC × 0.8	-	VCC + 0.3		
		V_{IL}	–0.3	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	–0.3	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.01	-	-		

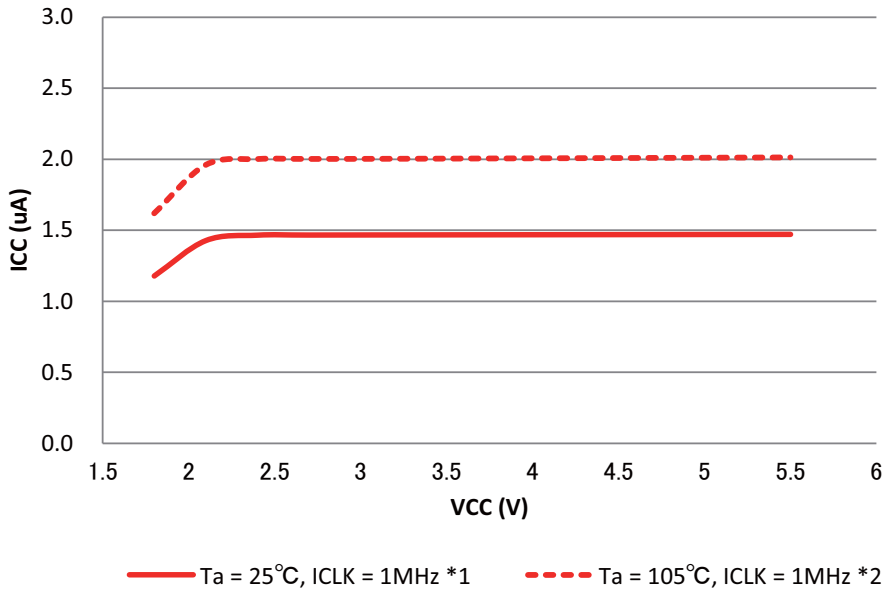
Note 1. P205, P206, P400 to P404, P407, P511, P512 (total 10 pins)

Table 2.11 Operating and standby current (1) (2/2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

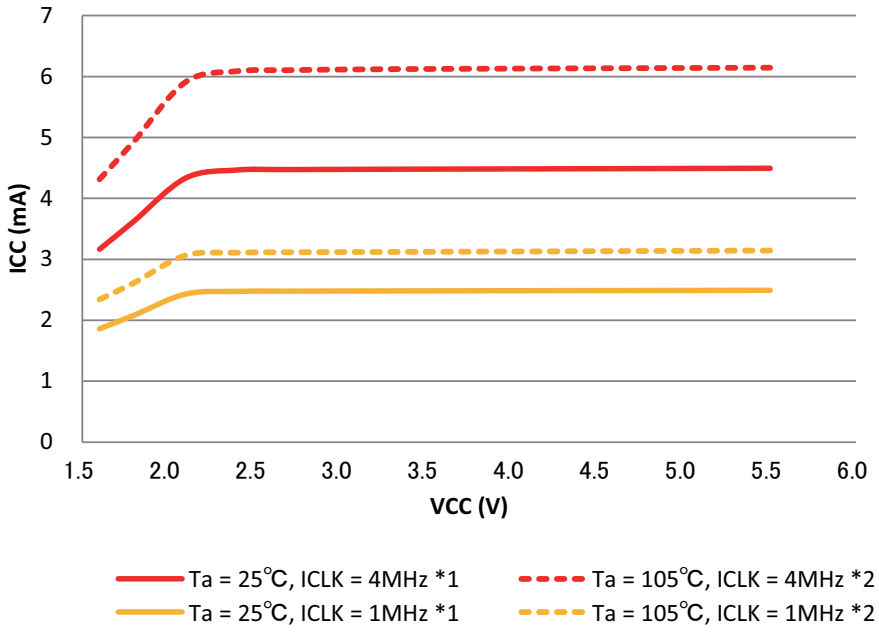
Item					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.7	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 1 MHz		1.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	3.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.4	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		1.3	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 4 MHz	I_{CC}	2.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		3.0	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		4.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	11.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		2.0	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		4.0	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	13.5	-	µA	*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		25.0	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	214.1		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		9.5	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		21.0	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 7. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.
Note 8. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK, BCLK, and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.



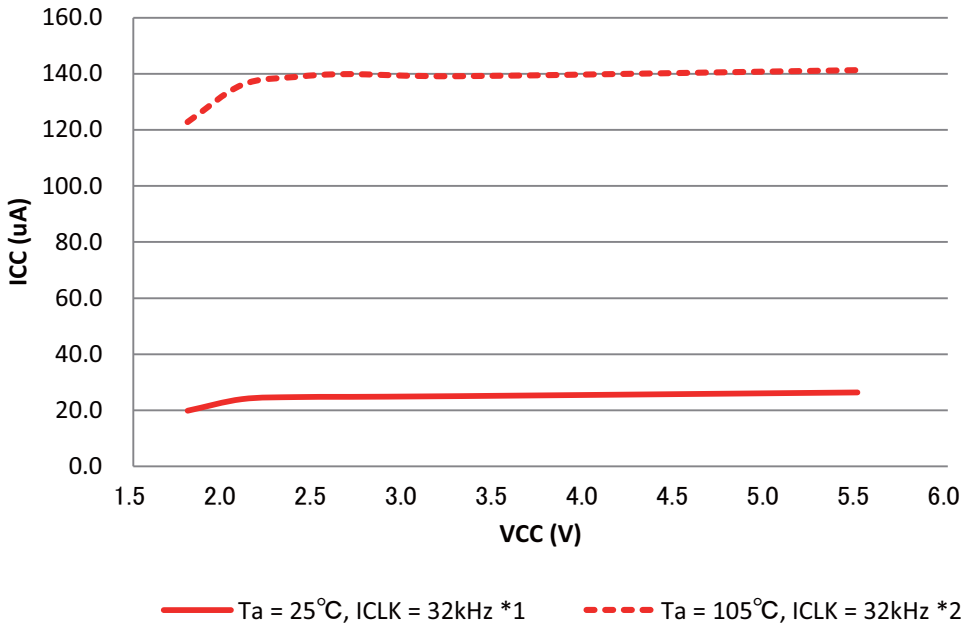
Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.19 Voltage dependency in low-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.20 Voltage dependency in low-voltage mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.21 Voltage dependency in Subosc-speed mode (reference data)

Table 2.12 Operating and standby current (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item			Symbol	Typ*4	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.9	6.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
		T_a = 55°C		1.6	12.2		
		T_a = 85°C		4.8	27.1		
		T_a = 105°C		12.2	66.7		
		T_a = 25°C		1.1	7.5		PSMCR.PSMC[1:0] = 00b (All SRAM on)
		T_a = 55°C		2.2	17.0		
		T_a = 85°C		7.5	43.3		
		T_a = 105°C		19.6	105.9		
	Increment for RTC operation with low-speed on-chip oscillator*3			0.5	-		-
	Increment for RTC operation with sub-clock oscillator*3			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.6	-		SOMCR.SODRV[1:0] are 00b (Normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.
Note 4. VCC = 3.3 V.

Table 2.18 Operation frequency value in middle-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	EBCLK pin output	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	8	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

Table 2.19 Operation frequency value in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK)*1, *3	1.8 to 5.5 V		0.032768	-	1	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	1	
	External bus clock (BCLK)*3	1.8 to 5.5 V		-	-	1	
	EBCLK pin output	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.

Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.

Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

2.3.2 Clock Timing

Table 2.22 Clock timing (1/2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	VCC = 2.7 V or above	t_{Bcyc}	83.3	-	-	ns	Figure 2.26
	VCC = 1.8 V or above		125	-	-		
	VCC = 1.6 V or above		500	-	-		
EBCLK pin output high pulse width	VCC = 2.7 V or above	t_{CH}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output low pulse width	VCC = 2.7 V or above	t_{CL}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EBCLK pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 2.27
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	µs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	µs	Figure 2.28
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	µs	-

Table 2.22 Clock timing (2/2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillation frequency		f_{HOCO24}	23.64	24	24.36	MHz	Ta = –40 to –20°C 1.8 ≤ VCC ≤ 5.5
			22.68	24	25.32		Ta = –40 to 85°C 1.6 ≤ VCC < 1.8
			23.76	24	24.24		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO32}	31.52	32	32.48		Ta = –40 to -20°C 1.8 ≤ VCC ≤ 5.5
			30.24	32	33.76		Ta = –40 to 85°C 1.6 ≤ VCC < 1.8
			31.68	32	32.32		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO48}*4	47.28	48	48.72		Ta = –40 to –20°C 1.8 ≤ VCC ≤ 5.5
			47.52	48	48.48		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			47.04	48	48.96		Ta = –40 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO64}*5	63.04	64	64.96		Ta = –40 to –20°C 2.4 ≤ VCC ≤ 5.5
			63.36	64	64.64		Ta = –20 to 85°C 2.4 ≤ VCC ≤ 5.5
			62.72	64	65.28		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*6, *7	Except Low-Voltage mode	t_{HOCO24} t_{HOCO32}	-	-	37.1	µs	Figure 2.29
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-Voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
PLL input frequency*2		f_{PLLIN}	4	-	12.5	MHz	-
PLL circuit oscillation frequency*2		f_{PLL}	24	-	64	MHz	-
PLL clock oscillation stabilization time*8		t_{PLL}	-	-	55.5	µs	Figure 2.30
PLL free-running oscillation frequency		f_{PLLFR}	-	8	-	MHz	-
Sub-clock oscillator oscillation frequency		f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization time*3		t_{SUBOSC}	-	0.5	-	s	Figure 2.31

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. The VCC range that the PLL can be used is 2.4 to 5.5 V.
Note 3. After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator manufacturer's recommended value has elapsed.
Note 4. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.
Note 5. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.
Note 6. This is a characteristic when HOCOCR.HCSTP bit is set to 0 (oscillation) in MOCO stop state.
When HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 7. Whether stabilization time has elapsed can be confirmed by OSCSF.HOCOSF.
Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in MOCO stop state.
When PLLCR.PLLSTP bit is set to 0 (operation) during MOCO oscillation, this specification is shortened by 1 µs.

2.3.6 Bus Timing

Table 2.31 Bus timing (1)
Conditions: EBCLK pin ≤ 12 MHz (package with 145 to 100 pins) (BCLK: up to 24 MHz)
VCC = AVCC0 = 2.7 to 5.5 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	37	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	37	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.32 Bus timing (2)
Conditions: EBCLK pin ≤ 8 MHz (package with 145 to 100 pins) (BCLK: up to 8 MHz)
VCC = AVCC0 = 2.4 to 2.7 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	45	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	45	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.33 Bus timing (3)
Conditions: EBCLK pin ≤ 4 MHz (package with 145 to 100 pins) (BCLK: up to 4 MHz)
VCC = AVCC0 = 1.8 to 2.4 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	90	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	90	ns	
CS delay	t_{CSD}	-	90	ns	
RD delay	t_{RSD}	-	90	ns	
Read data setup time	t_{RDS}	70	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	90	ns	
Write data delay	t_{WDD}	-	90	ns	
Write data hold time	t_{WDH}	0	-	ns	

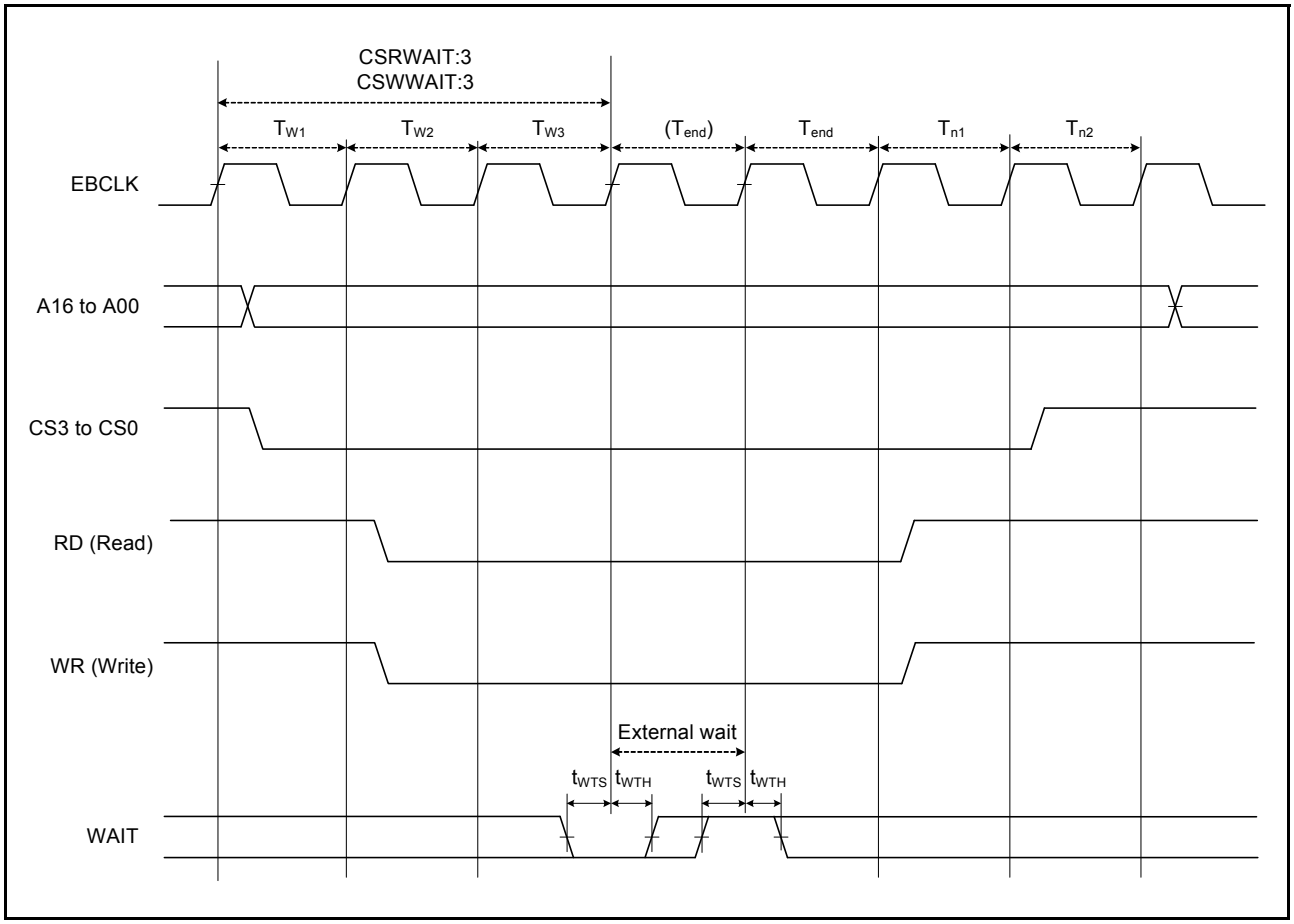


Figure 2.42 External bus timing/external wait control

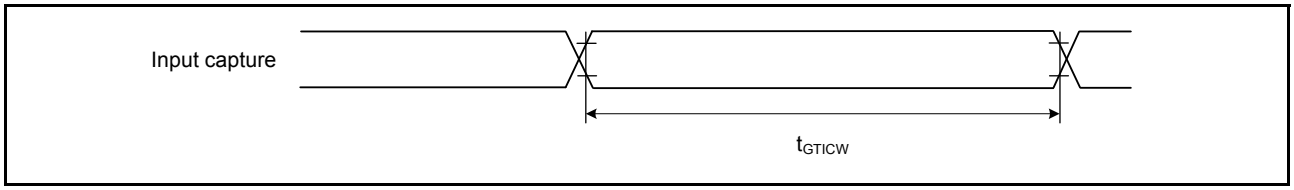


Figure 2.45 GPT input capture timing

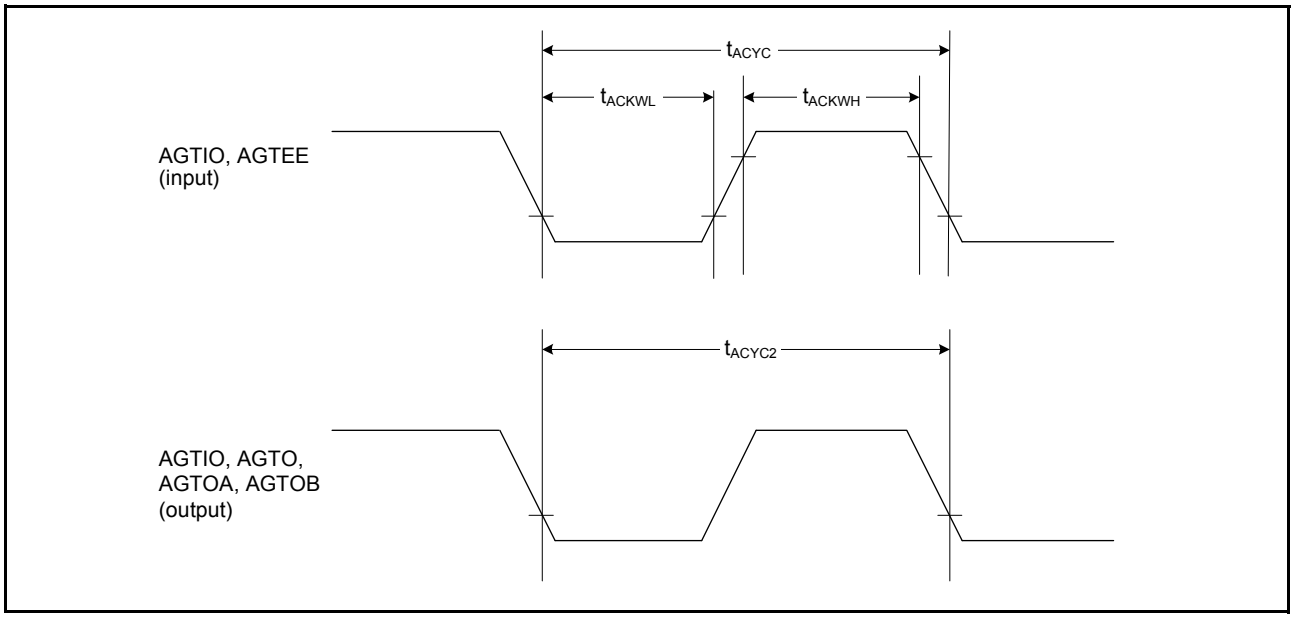


Figure 2.46 AGT I/O timing

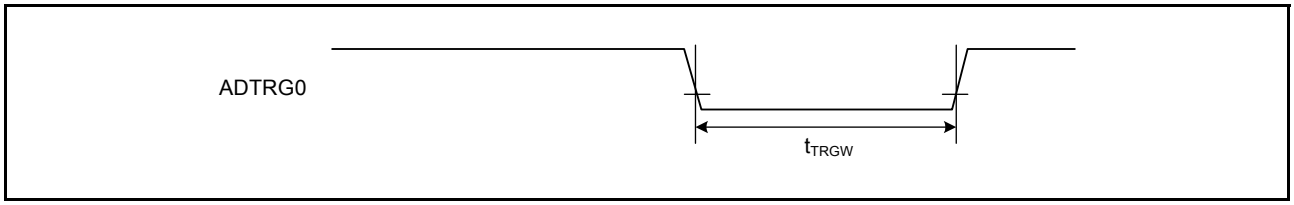


Figure 2.47 ADC14 trigger input timing

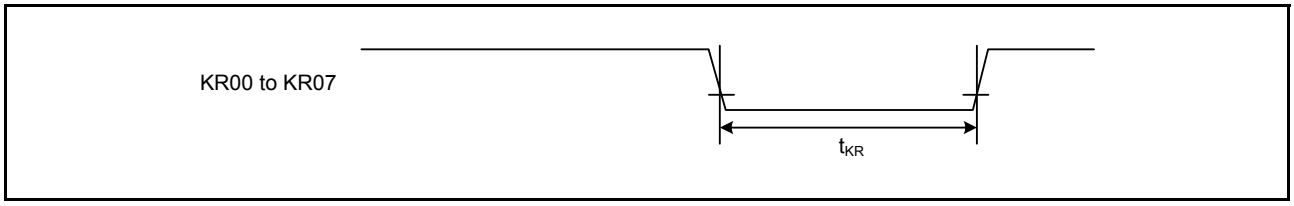
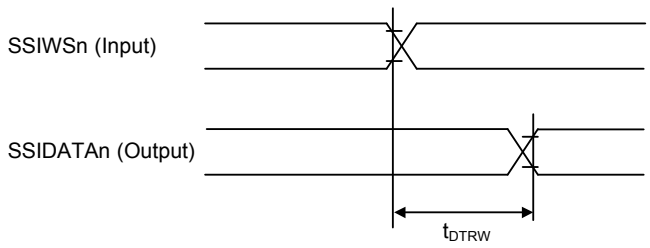


Figure 2.48 Key interrupt input timing

2.3.8 CAC Timing

Table 2.36 CAC timing

Item			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > t_{cac}$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	



MSB bit output delay from SSIWSn change time for Slave transmitter when DEL = 1, SDTA = 0 or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0]

Figure 2.70 SSI data output delay from SSIWSn change time

2.3.14 SD/MMC Host Interface Timing

Table 2.44 SD/MMC host interface signal timing

Conditions: VCC = AVCC0 = 2.7 to 5.5 V
Middle drive output is selected in the Drive Capavility Control in PmnPFS register

Item	Symbol	Min	Max	Unit	Test conditions
SDCLK clock cycle	t_{SDCYC}	62.5	-	ns	Figure 2.71
SDCLK clock high-level pulse width	t_{SDWH}	18.25	-	ns	
SDCLK clock low-level pulse width	t_{SDWL}	18.25	-	ns	
SDCLK clock rising time	t_{SDLH}	-	10	ns	
SDCLK clock falling time	t_{SDHL}	-	10	ns	
SDCMD/SDDAT output data delay	t_{SDODLY}	–18.25	18.25	ns	
SDCMD/SDDAT input data setup	t_{SDIS}	9.25	-	ns	
SDCMD/SDDAT input data hold	t_{SDIH}	23.25	-	ns	

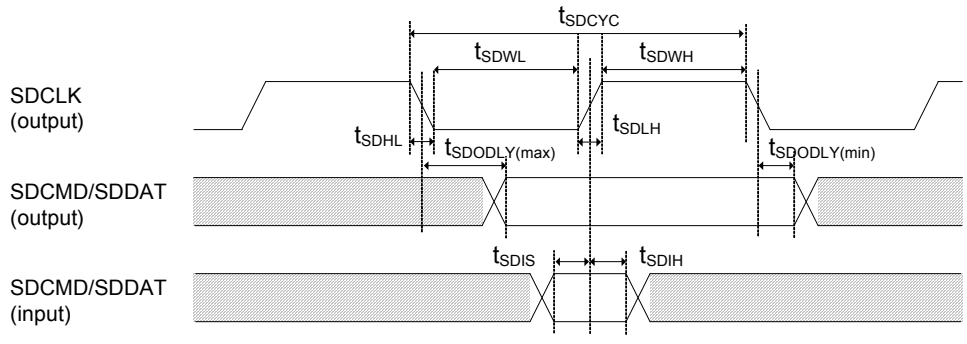


Figure 2.71 SD/MMC host interface signal timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.46 USB characteristics
Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 5.5 V

Item			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP - USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL}= 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 2.73, Figure 2.74, Figure 2.75
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D + sink current		I_{DP_SINK}	25	175	µA	-
	D – sink current		I_{DM_SINK}	25	175	µA	-
	DCD source current		I_{DP_SRC}	7	13	µA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D + source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D – source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

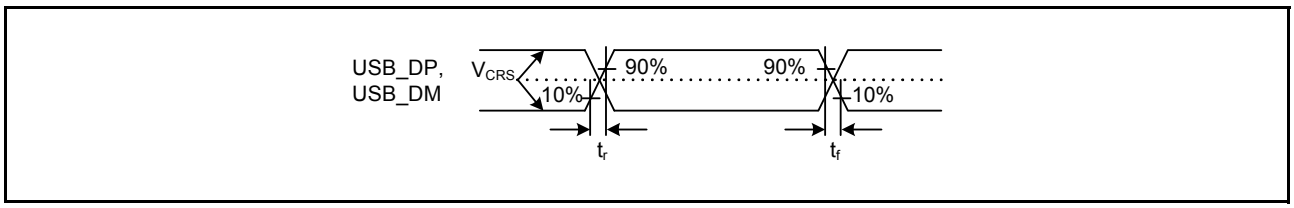


Figure 2.73 USB_DP and USB_DM output timing

2.5 ADC14 Characteristics

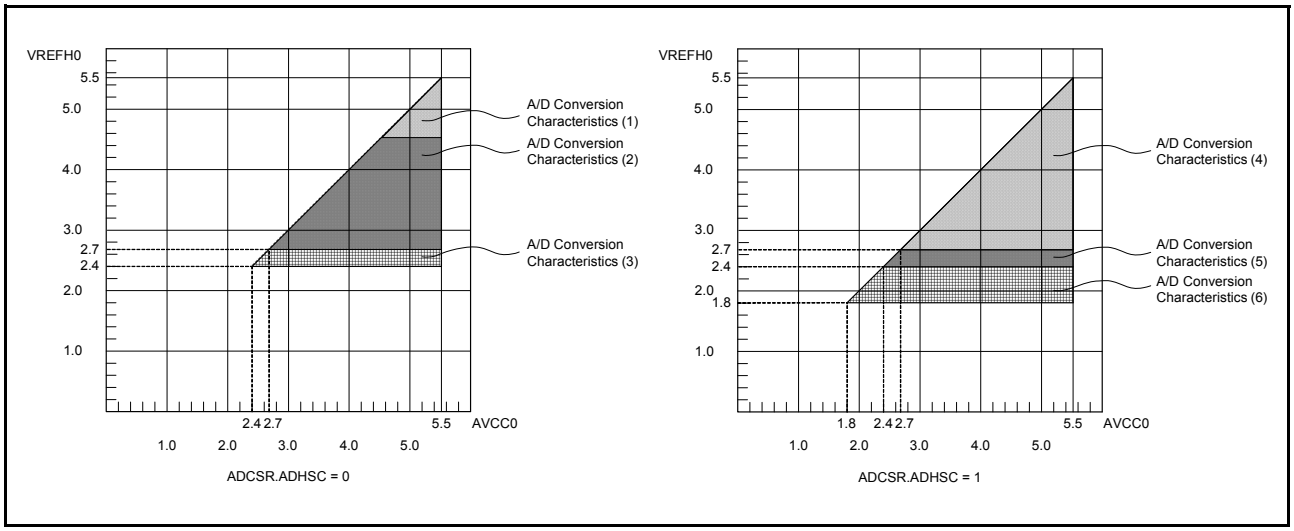


Figure 2.76 AVCC0 to VREFH0 voltage range

Table 2.48 A/D conversion characteristics (1) in high-speed mode (1/2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	64	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

2.9 POR and LVD Characteristics

Table 2.62 Power-on reset circuit and voltage detection circuit characteristics (1)
Conditions: VCC = AVCC0 = VCC_USB

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.80, Figure 2.81
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.82 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.83 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.84 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit (LVD2), it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol Vdet0_# denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

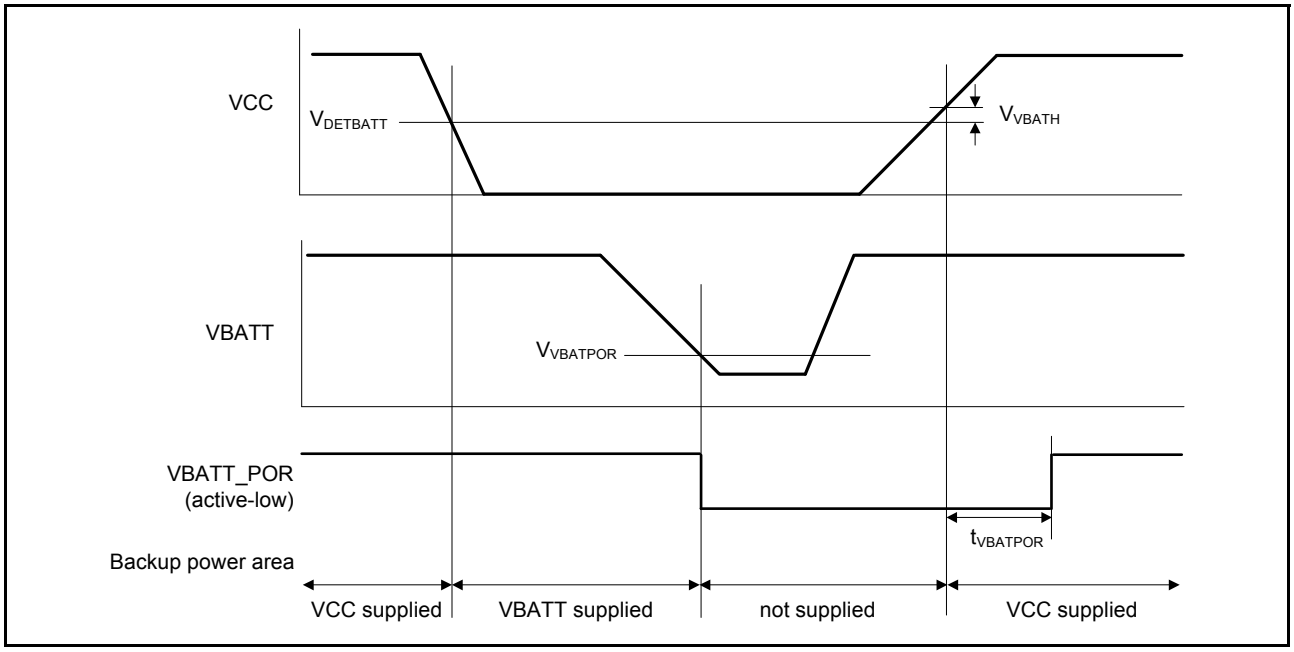


Figure 2.86 VBATT_POR Reset Timing

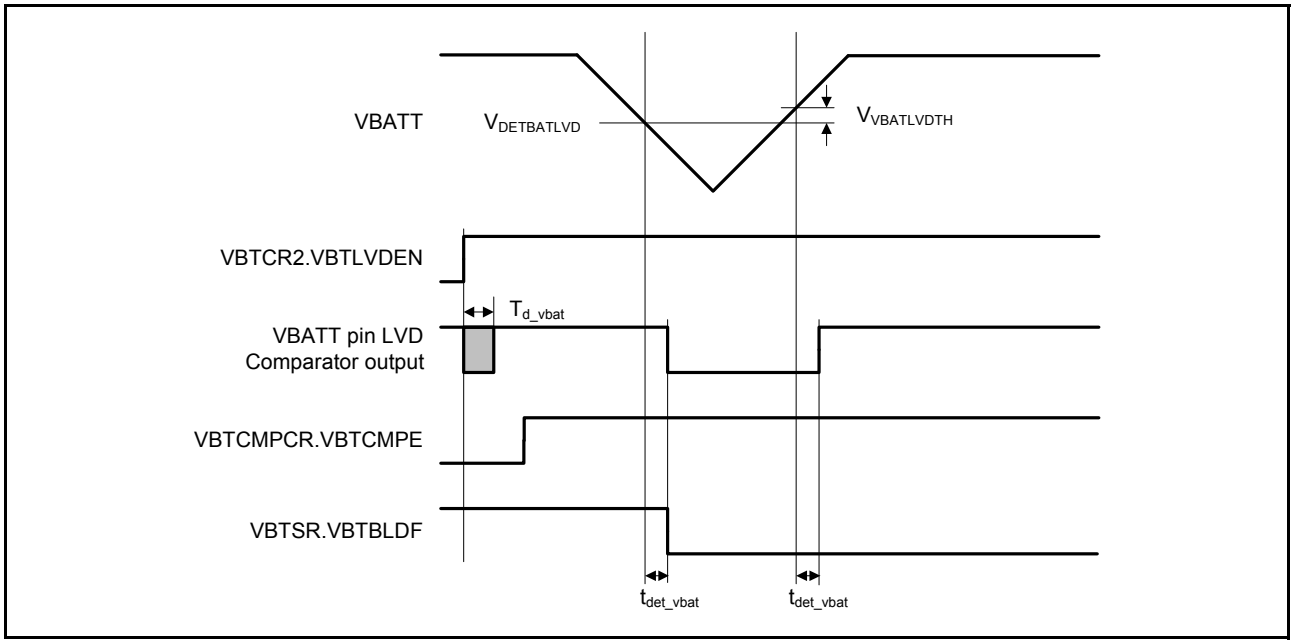


Figure 2.87 VBATT pin Voltage Detection Circuit Timing

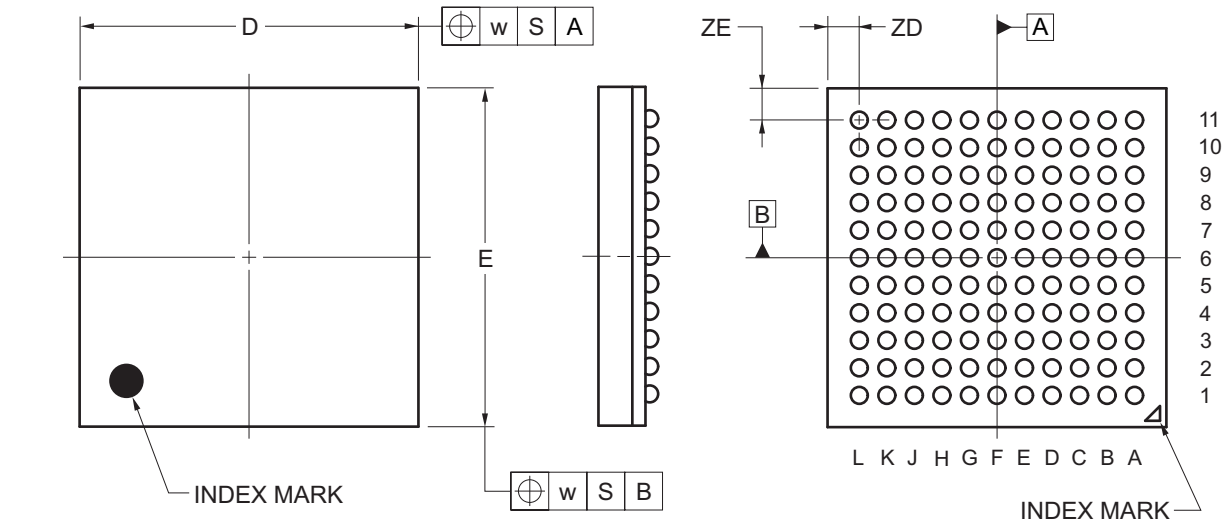
2.11 CTSU Characteristics

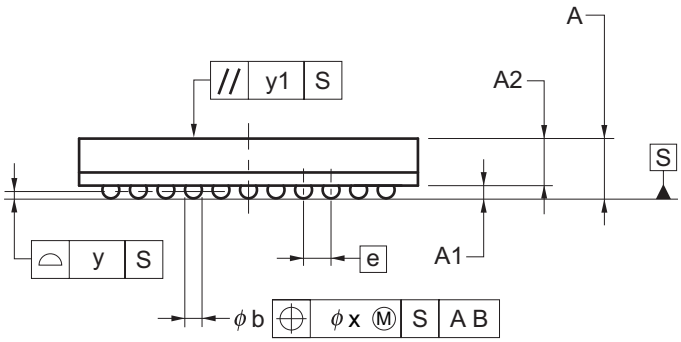
Table 2.65 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
-	PLBG0121JA-A	P121F1-65-CAH	-





(UNIT: mm)

ITEM	DIMENSIONS
D	8.00±0.10
E	8.00±0.10
w	0.20
A	1.21±0.10
A1	0.30±0.05
A2	0.91
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.75
ZE	0.75

Figure 1.3 BGA 121-pin

Revision History	S3A7 Datasheet

Rev.	Date	Chapter	Summary
0.80	Oct. 12, 2015	—	First Edition issued
0.85	Dec. 15, 2015	—	Second Edition issued
1.00	Feb. 23, 2016	section 1, Overview	Updated channel number of CTSU in Table 1.14, Function comparison
			Updated pin name of CTSU in section 1.5, Pin Functions
			Updated pin name of CTSU in section 1.7, Pin Lists
		section 2, Electrical Characteristics	Added section 2.17, Joint European Test Action Group (JTAG) and section 2.17.1, Serial Wire Debug (SWD) in section 2, Electrical Characteristics
			Updated input voltage in Table 2.1, Absolute maximum ratings
			Added section 2.2.5, I/O Pin Output Characteristics of Low Drive Capacity
			Updated Table 2.6, I/O I_{OH}, I_{OL} in section 2.2.3, I/O I_{OH}, I_{OL} to change from normal drive to low drive
			Changed Note 6 to Note 5. in Table 2.11, Operating and standby current (1)
			Updated the conditions in Table 2.13, Operating and standby current (3)
			Updated Note 2. in Table 2.17, Operation frequency value in high-speed operating mode
			Updated Note 2. in Table 2.18, Operation frequency value in middle-speed mode
			Removed the 2nd note from Table 2.19, Operation frequency value in low-speed mode
			Updated Note 2. in Table 2.20, Operation frequency value in low-voltage mode
			Updated Table 2.22, Clock timing
			Updated the condition of the I/O Ports in Table 2.35, I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing
			Removed the 2nd note from Table 2.37, SCI timing (1)
			Updated the conditions in Table 2.38, SCI timing (2)
			Updated Figure 2.59, SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)
			Added the conditions in Table 2.42, IIC timing
			Updated Figure 2.68, SSI data transmit/receive timing (SSICR.SCKP = 0)
			Updated the Quantization error in the following tables: · Table 2.48, A/D conversion characteristics (1) in high-speed mode · Table 2.49, A/D conversion characteristics (2) in high-speed mode · Table 2.50, A/D conversion characteristics (3) in high-speed mode · Table 2.51, A/D conversion characteristics (4) in low power mode · Table 2.52, A/D conversion characteristics (5) in low power mode
			Updated Table 2.55, 14-Bit A/D converter channel classification
			Updated Table 2.64, Battery Backup Function Characteristics
			Deleted VLCD = 0Dh to 13h in Table 2.70, Internal voltage boosting method LCD characteristics
			Updated the response time in Table 2.72, ACMPHS characteristics
			Added the temperature in Table 2.77, Code flash characteristics (3)
			Added the temperature in Table 2.80, Data flash characteristics (3)
		All	Deleted # from pin names