Renesas Electronics America Inc - R7FS3A77C3A01CFM#AA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, MMC/SD, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c3a01cfm-aa1

1. Overview

The S3A7 MCU comprises multiple series of software- and pin-compatible ARM-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

This MCU provides an optimal combination of low-power, high-performance ARM® Cortex®-M4 core running up to 48 MHz with the following features:

- Up to 1-MB code flash memory
- 192-KB SRAM
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit ADC
- 12-bit DAC
- Security features.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 48 MHz • ARM Cortex-M4: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single Precision Floating Point Unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 1 MB code flash memory. See section 48, Flash Memory in User's Manual.
Data flash memory	16 KB data flash memory. See section 48, Flash Memory in User's Manual.
Option-Setting Memory	The Option-Setting Memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the desired application image load address in code flash memory to the application image link address in the unused memory 23-bit space (memory mirror space addresses). The user application code is developed and linked to run from this MMF destination address. The user application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	This MCU has an on-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). There is an area in SRAM0 that provides error correction capability using ECC. See section 47, SRAM in User's Manual.

Table 1.3 System (1/2)

Feature	Functional description
Operating mode	Two operating modes: - Single-chip mode - SCI/USB boot mode. See section 3, Operating Modes in User's Manual.
Reset	This MCU has 14 types of resets: • RES pin reset • Power-on reset • VBATT selected voltage power on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clock	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) is used to check the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Low Power Mode	This MCU has several functions for reducing power consumption, such as setting clock dividers, controlling EBCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Mode in User's Manual.
Battery Backup Function	This MCU has a battery backup function that can be partly powered by a battery. The battery powered area includes RTC/AGT/SOSC/LOCO/Wakeup Control/Backup Memory/VBATT_R Low Voltage Detection/Switch between VCC/VBATT. During normal operation, the battery powered area is powered by the main power supply which is the VCC pin. When a VCC voltage drop is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 12, Battery Backup Function in User's Manual.
Register Write Protection	The Register Write Protection function protects important registers from being overwritten due to software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	This MCU incorporates two memory protection units and provide a CPU stack pointer monitor function. See section 16, Memory Protection Unit (MPU) in User's Manual.

Table 1.9 Communication interfaces (2/2)

Feature	Functional description
Controller Area Network (CAN) Module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 32, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed Module (USBFS)	This MCU incorporates a USB 2.0 Full-Speed module (USBFS). The USBFS is a USB controller that is equipped to operate as a host controller or function controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. PIPE1 to PIPE9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. This MCU supports revision 1.2 of the battery charging specification. Because this MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply 3.3 V. See section 28, USB 2.0 Full-Speed Module (USBFS) in User's Manual.
SD/MMC Host Interface (SDHI)	The Secure Digital Host Interface (SDHI) and MultiMediaCard (MMC) interface provide the functionality needed to connect a variety of external memory cards with this MCU. The SDHI supports both 1-bit and 4-bit buses for connecting different memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports for high-speed SDR transfer modes. See section 37, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.10 Analog (1/2)

Feature	Functional description
14-bit A/D Converter (ADC14)	This MCU incorporates up to one unit of a 14-bit successive approximation A/D converter. Up to 28 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 39, 14-Bit A/D Converter (ADC14) in User's Manual.
12-bit D/A Converter (DAC12)	This MCU includes a 12-bit D/A converter with an output amplifier. See section 40, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature Sensor (TSN)	The on-chip temperature sensor can be used to determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC for conversion and can be further used by the end application. See section 41, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	Analog comparators can be used to compare a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the comparator from internal sources such as D/A converter output and internal reference voltage, and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 43, High-Speed Analog Comparator (ACMPHS) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	Analog comparators can be used to compare a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin or from the internal reference voltage (Vref) generated internally in this MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 44, Low-Power Analog Comparator (ACMPLP) in User's Manual.

1.2 Block Diagram

Figure 1.1 shows the block diagram of this MCU superset. Individual devices within the group may have a subset of the features.

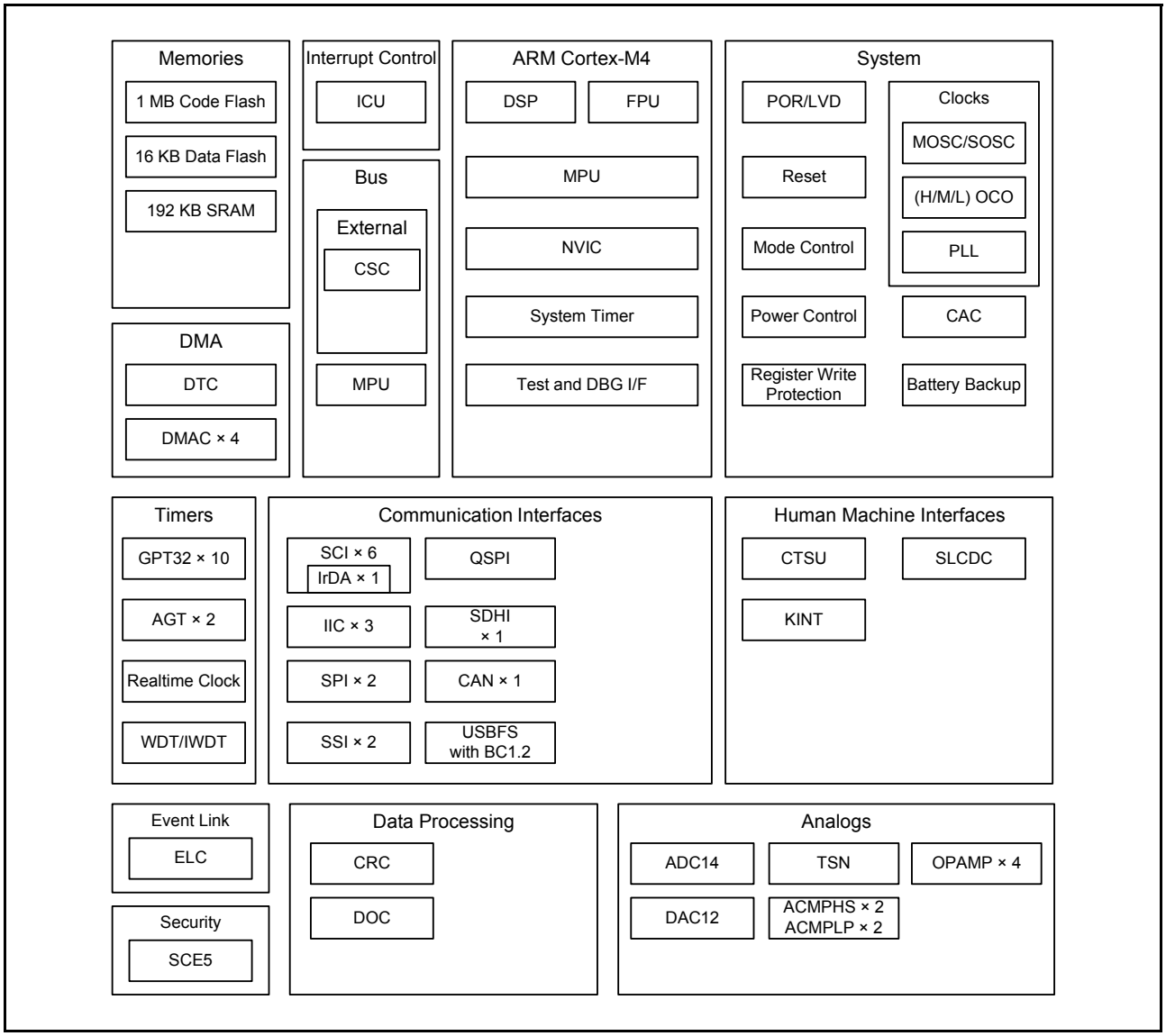

Figure 1.1 Block diagram

R7FS3A77C2A01CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	P215/ XCIN	VCL	P403	P400	P000	10
9	USB_DM	USB_DP	P413	VSS	P213/ XTAL	P214/ XCOUT	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	VCC_US B_LDO	P411	P415	P708	P404	P003	P004	P002	8
7	P205	P204	P206	P408	P414	P406	P006	P007	P008	P005	7
6	VSS	VCC	P202	P203	P410	P402	P505	AVSS0	P011/ VREFL0	P010/ VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	P013/ VREFL	P012/ VREFH	5
4	P305	P304	P808	P306	P115	P601	P503	P100	P015	P014	4
3	P809	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	P603	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO/ SWO	P112	P608	VCC	VSS	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.7 Pin assignment for LGA 100-pin (Upper perspective view)

Pin number							Power, System, Clock, Debug, CAC, VBATT	I/O ports	External bus	Timers				Communication interfaces						Analogs			HMI		
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64				AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSI	SDHI	ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	SLCDC	CTSU	Interrupt
M10	138	J9	98	K8	62	62		P002												AN002	AMP0O	IVREF2/ IVCMP2			IRQ8
N10	139	K9	99	K9	63	63		P001												AN001	AMP0-	IVREF1/ IVCMP1		TS22	IRQ7
L10	140	L9	100	K10	64	64		P000												AN000	AMP0+	IVREF0/ IVCMP0		TS21	IRQ6
N11	141						VSS																		
N12	142						VCC																		
M11	143	L10						P512				GTIOC0A_B			TXD4_B/ MOSI4_B/ SDA4_B	SCL2									IRQ14
M12	144	K10						P511				GTIOC0B_B			RXD4_B/ MISO4_B/ SCL4_B	SDA2									IRQ15
E5		F6					NC																		

Note: Several pin names have the added suffix of _A, _B, and _C. The suffix can be ignored when assigning functionality.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC Characteristics
Conditions: Products with operating temperature (T_a) –40 to +105°C

Item	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)
Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 2.7 to 5.5 V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	IIC*1 (except for SMBus)	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	–0.3	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	VCC + 0.3		
		V_{IL}	–0.3	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	VCC + 0.3		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	VCC + 0.3		VCC = 2.7 to 3.6 V
		V_{IL}	–0.3	-	0.8		-
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	–0.3	-	VCC × 0.2		
	P000 to P015	V_{IH}	AVCC0 × 0.8	-	AVCC + 0.3		
		V_{IL}	–0.3	-	AVCC0 × 0.2		
	EXTAL D00 to D15 Input ports pins except for P000 to P015	V_{IH}	VCC × 0.8	-	VCC + 0.3		
		V_{IL}	–0.3	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	–0.3	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.05	-	-		

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A, SCL2, SDA2, SDA0_B (total 7 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B, SCL2, SDA2 (total 10 pins).
Note 3. P205, P206, P400 to P404, P407, P511, P512 (total 10pins).

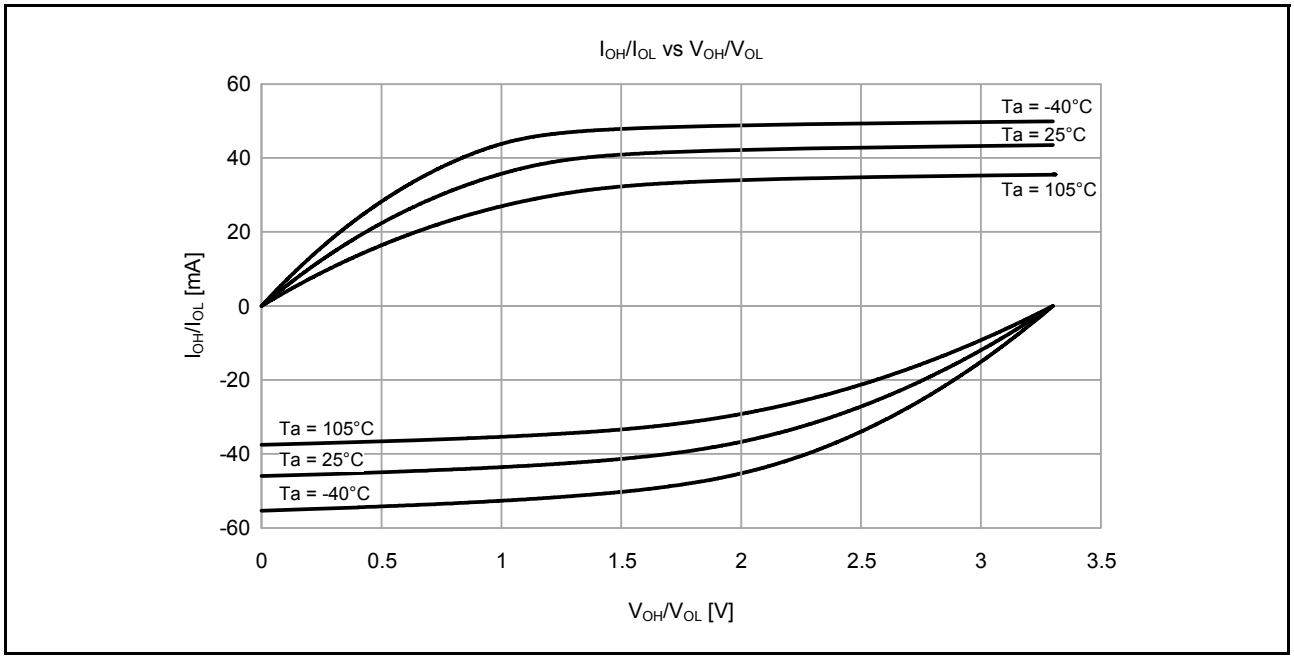

Figure 2.10 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Middle drive output is Selected (Reference Data)**

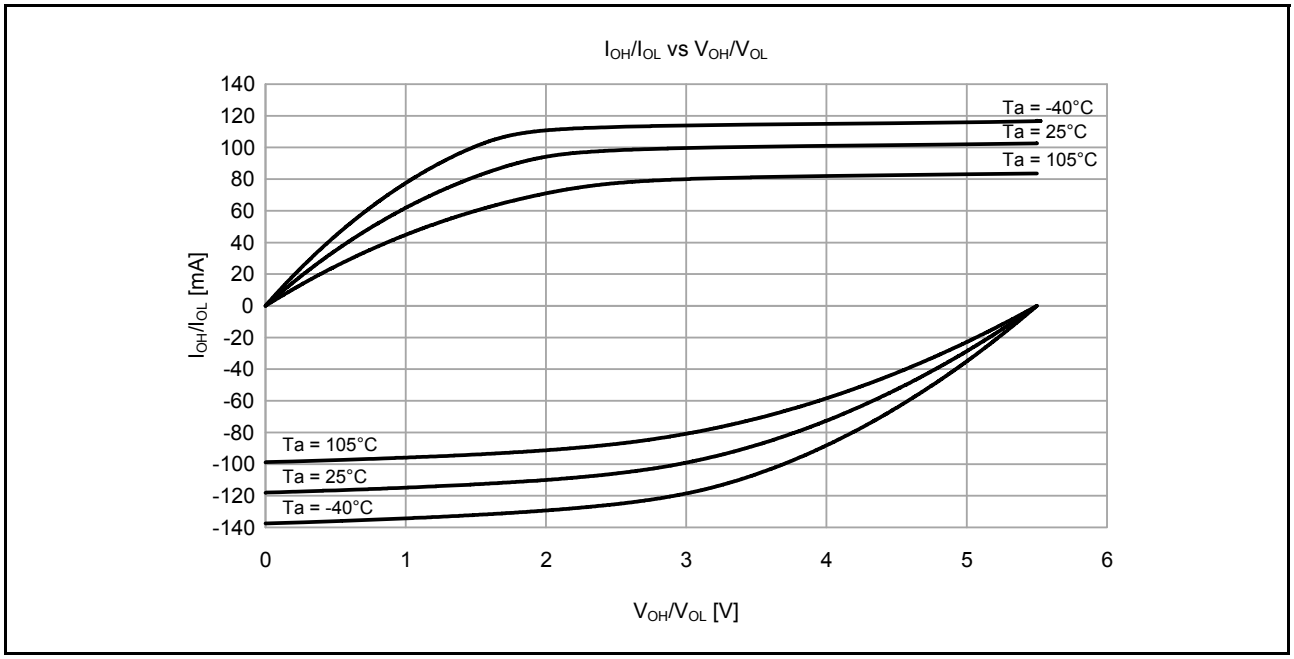

Figure 2.11 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When Middle drive output is Selected (Reference Data)**

2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

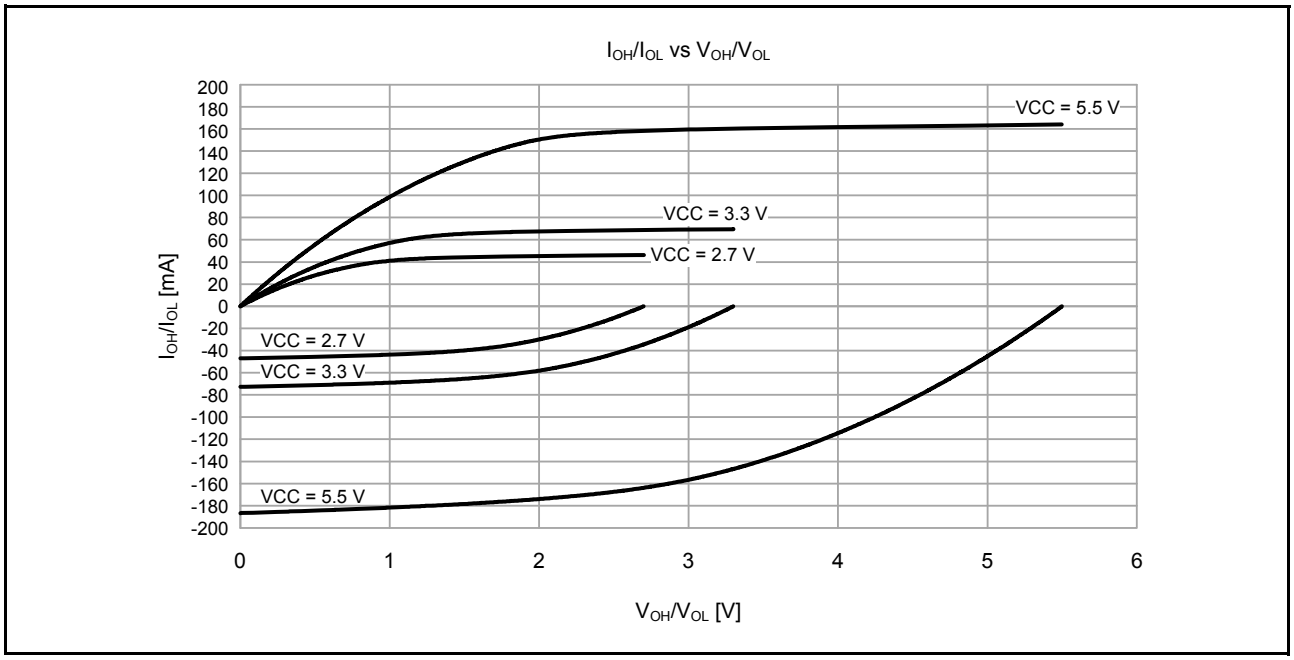

Figure 2.12 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at Ta = 25°C When Middle drive output is Selected (Reference Data)**

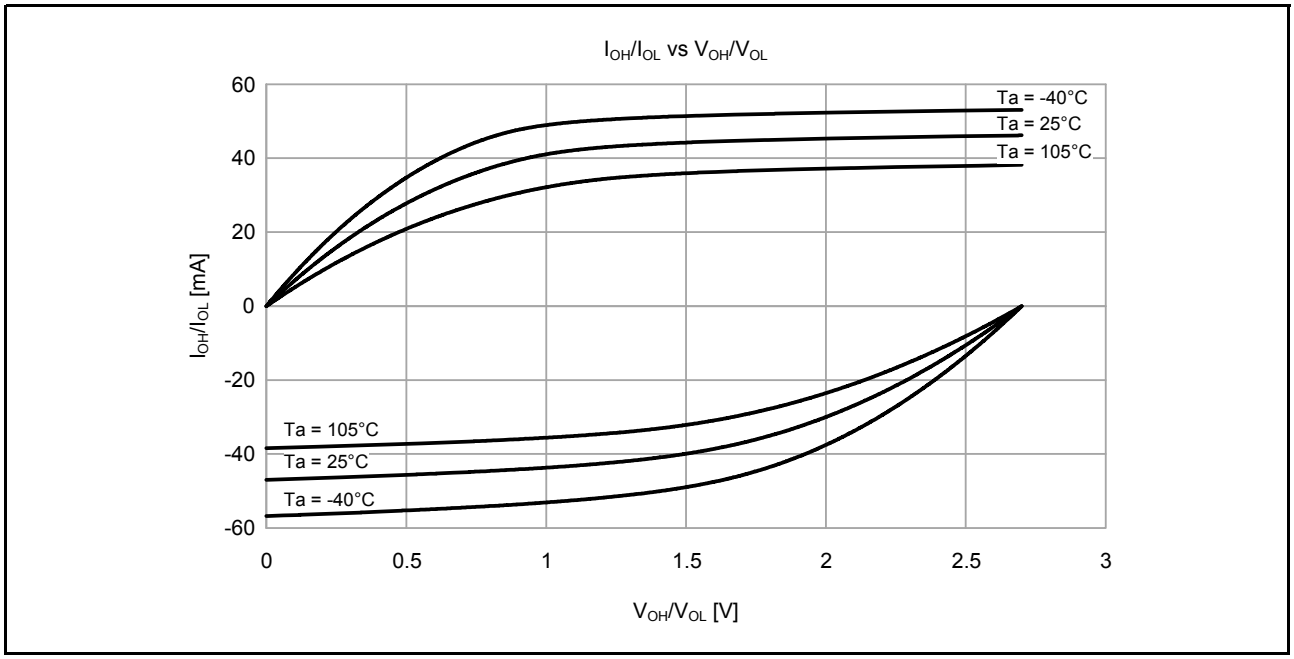

Figure 2.13 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Low drive output is Selected (Reference Data)**

Table 2.11 Operating and standby current (1) (2/2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.7	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 1 MHz		1.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	3.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.4	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		1.3	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 4 MHz	I_{CC}	2.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		3.0	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		4.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	11.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		2.0	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		4.0	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	13.5	-	µA	*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		25.0	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	214.1		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		9.5	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		21.0	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 7. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.
Note 8. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK, BCLK, and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.

2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.15 Rise and fall gradient characteristics
Conditions: VCC = AVCC0 = 0 to 5.5 V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1, *2		0.02	-	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn the power supply voltage on according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 2.16 Rising and falling gradient and ripple frequency characteristics
Conditions: VCC = AVCC0 = VCC_USB = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 2.25 $V_{r\ (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.25 $V_{r\ (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.25 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

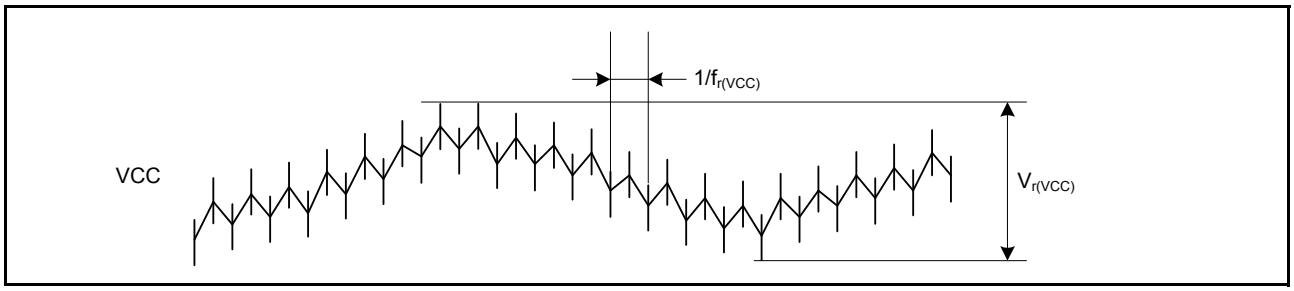

Figure 2.25 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.17 Operation frequency value in high-speed operating mode

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	48	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	24	
		2.4 to 2.7 V		-	-	16	
	EBCLK pin output	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

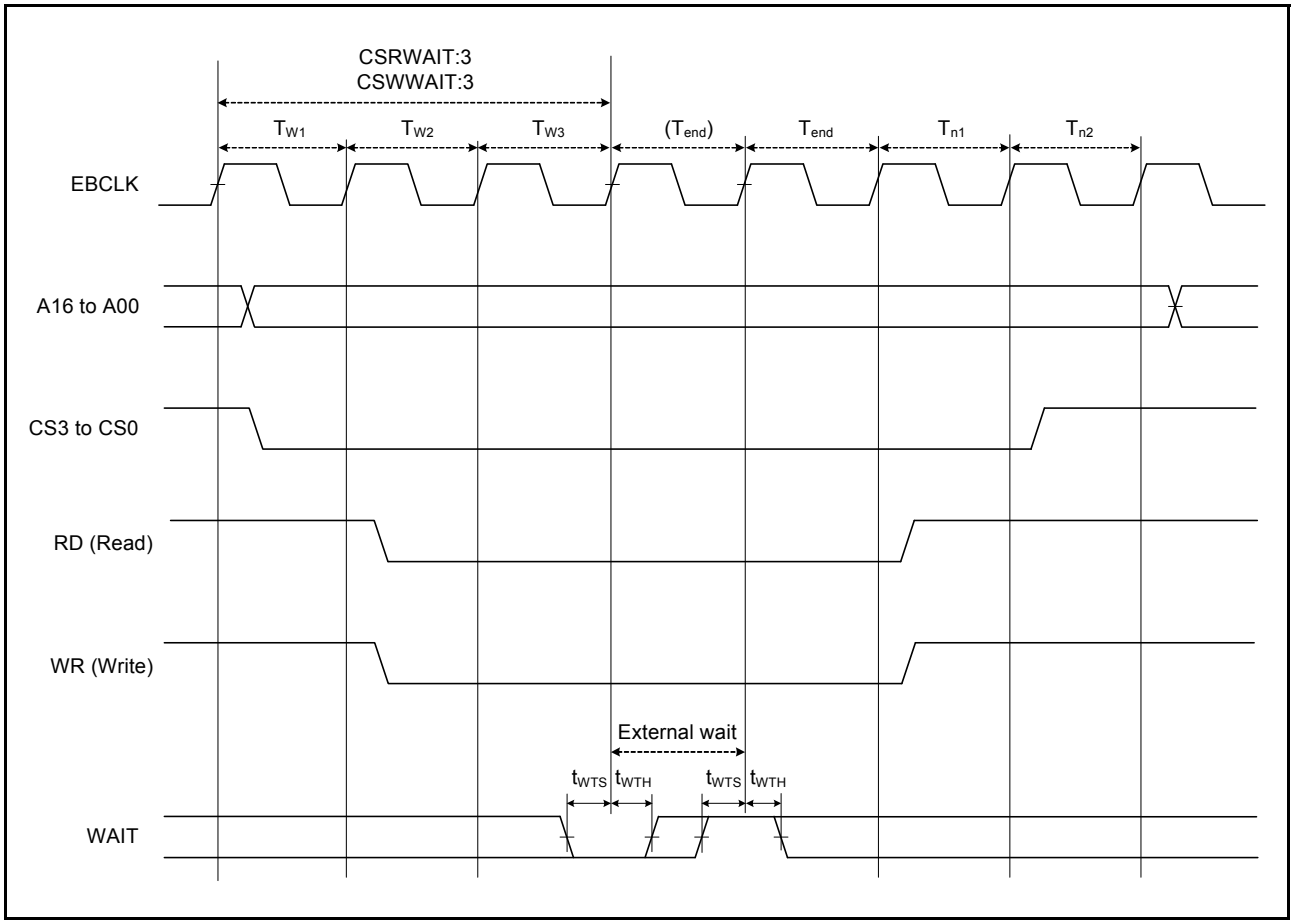

Figure 2.42 External bus timing/external wait control

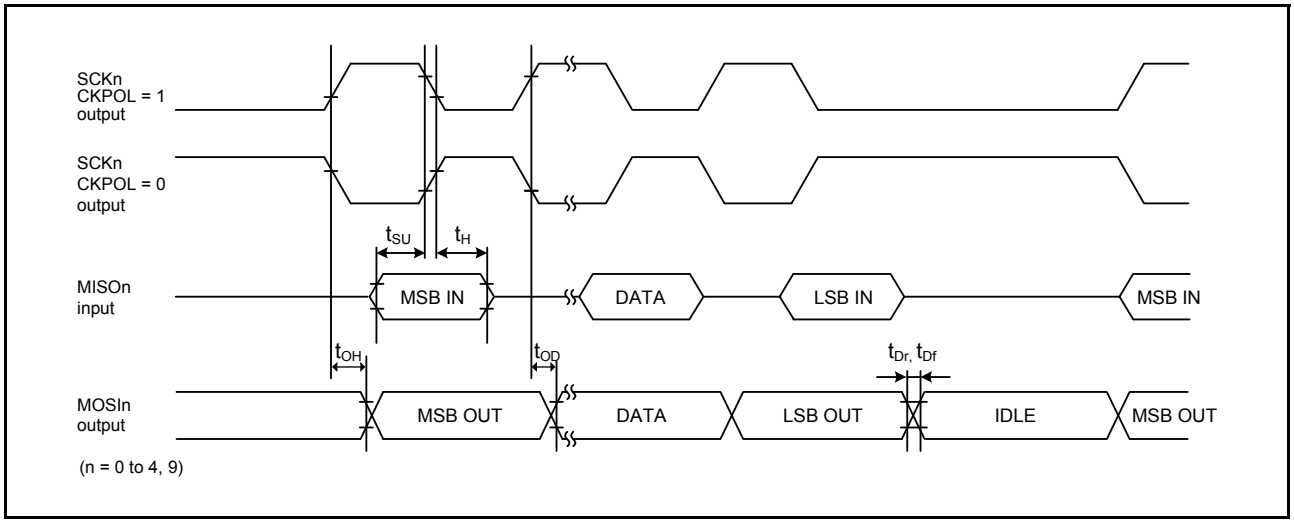

Figure 2.53 SCI simple SPI mode timing (master, CKPH = 0)

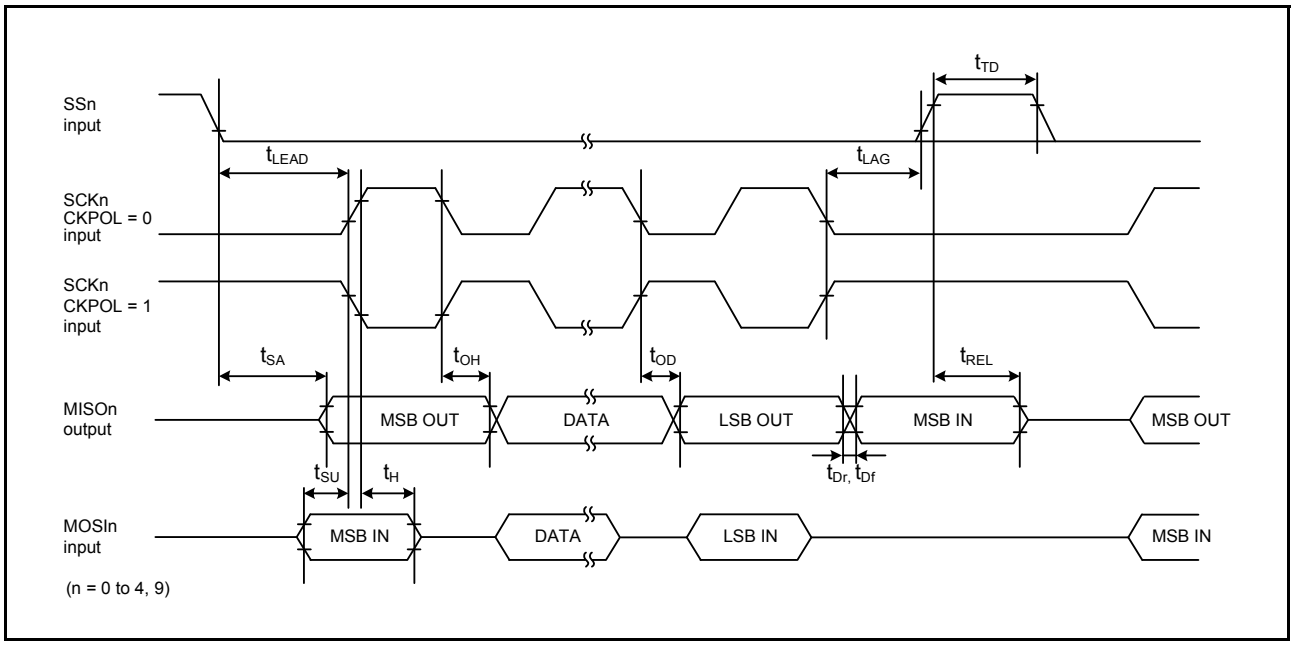

Figure 2.54 SCI simple SPI mode timing (slave, CKPH = 1)

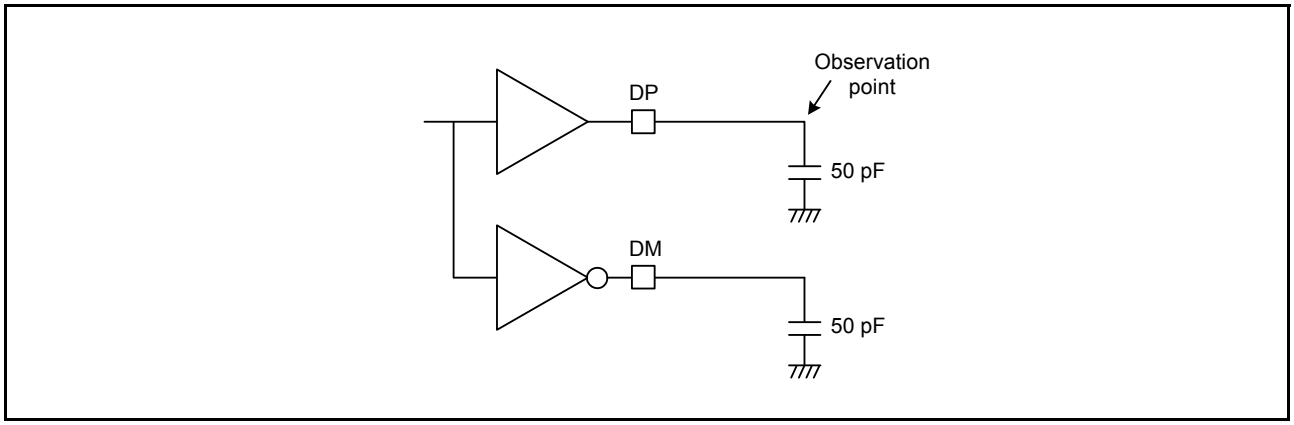

Figure 2.74 Test circuit for Full-Speed (FS) connection

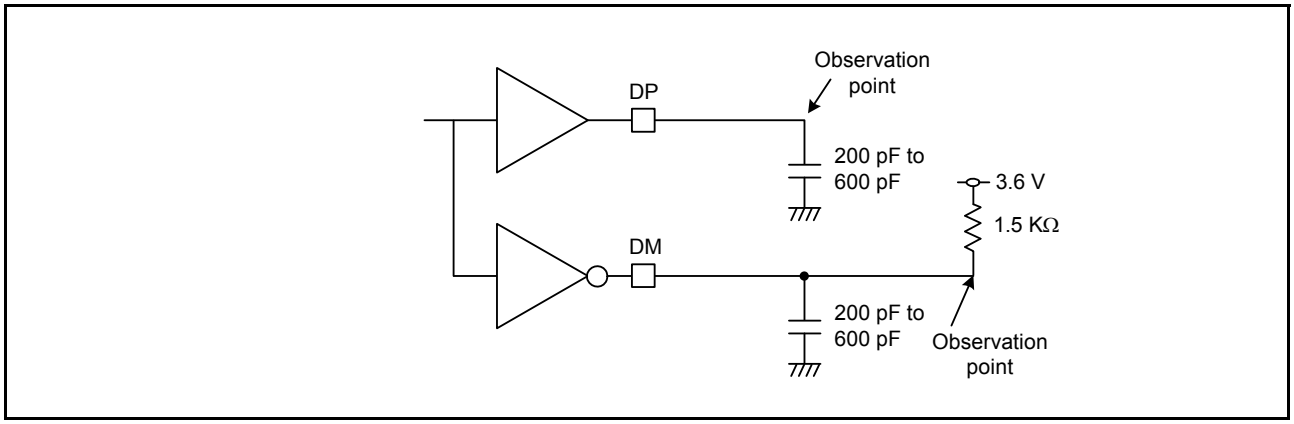

Figure 2.75 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.47 USB regulator

Item		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

2.5 ADC14 Characteristics

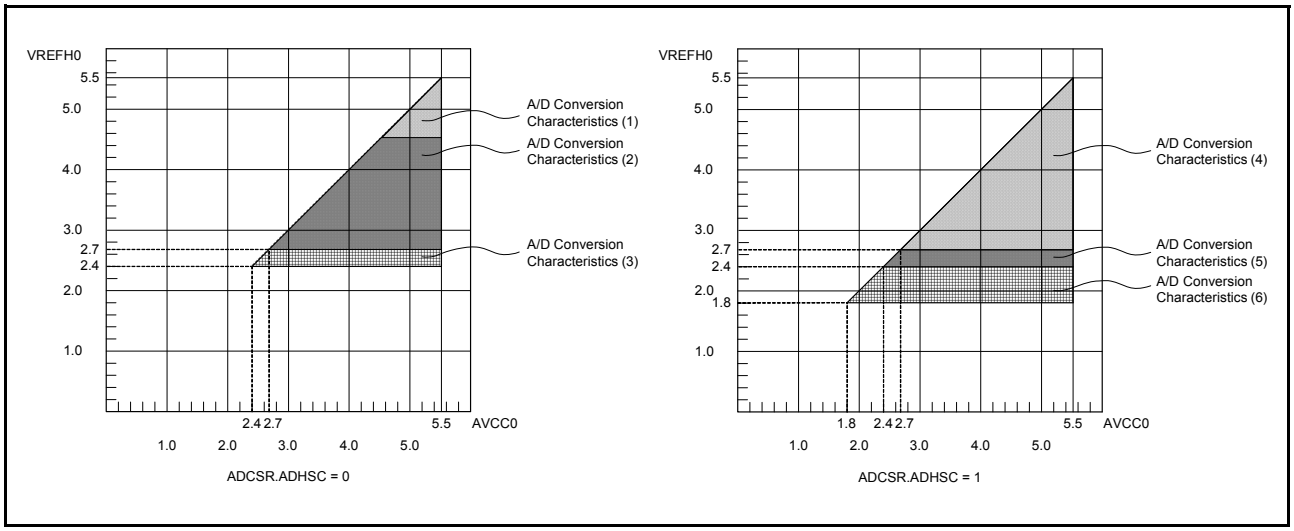

Figure 2.76 AVCC0 to VREFH0 voltage range

Table 2.48 A/D conversion characteristics (1) in high-speed mode (1/2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	64	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

2.12 Segment LCD Controller/Driver Characteristics

2.12.1 Resistance Division Method

[Static Display Mode]

Table 2.66 Resistance division method LCD characteristics (1)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 2.67 Resistance division method LCD characteristics (2)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 2.68 Resistance division method LCD characteristics (3)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

2.12.2 Internal Voltage Boosting Method

[1/3 Bias Method]

Table 2.69 Internal voltage boosting method LCD characteristics
Conditions: VCC = AVCC0 = 1.8 V to 5.5 V

Item	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
			VLCD = 0Dh	1.35	1.45	1.53	V	-
			VLCD = 0Eh	1.40	1.50	1.58	V	-
			VLCD = 0Fh	1.45	1.55	1.63	V	-
			VLCD = 10h	1.50	1.60	1.68	V	-
			VLCD = 11h	1.55	1.65	1.73	V	-
			VLCD = 12h	1.60	1.70	1.78	V	-
			VLCD = 13h	1.65	1.75	1.83	V	-
Doubler output voltage	V_{L2}	C1 to C4*1 = 0.47 µF		$2 \times V_{L1}$ - 0.1	$2 \times V_{L1}$	$2 \times V_{L1}$	V	-
Tripler output voltage	V_{L4}	C1 to C4*1 = 0.47 µF		$3 \times V_{L1}$ - 0.15	$3 \times V_{L1}$	$3 \times V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.88
LCD output voltage variation range*3	t_{VLWT}	C1 to C4*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between VL1 and GND
C3: A capacitor connected between VL2 and GND
C4: A capacitor connected between VL4 and GND
C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 2. This is the time required to wait from when the reference voltage is specified using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

[1/4 Bias Method]

Table 2.70 Internal voltage boosting method LCD characteristics

Conditions: VCC = AVCC0 = 1.8 V to 5.5 V

Item	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
Doubler output voltage	V_{L2}	C1 to C5*1 = 0.47 µF		$2V_{L1}$ - 0.08	$2V_{L1}$	$2V_{L1}$	V	-
Tripler output voltage	V_{L3}	C1 to C5*1 = 0.47 µF		$3V_{L1}$ - 0.12	$3V_{L1}$	$3V_{L1}$	V	-
Quadruply output voltage	V_{L4}*4	C1 to C5*1 = 0.47 µF		$4V_{L1}$ - 0.16	$4V_{L1}$	$4V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.88
LCD output voltage variation range*3	t_{VLWT}	C1 to C5*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between VL1 and GND
C3: A capacitor connected between VL2 and GND
C4: A capacitor connected between VL3 and GND
C5: A capacitor connected between VL4 and GND
C1 = C2 = C3 = C4 = C5 = 0.47 µF ± 30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. V_{L4} must be 5.5 V or lower.

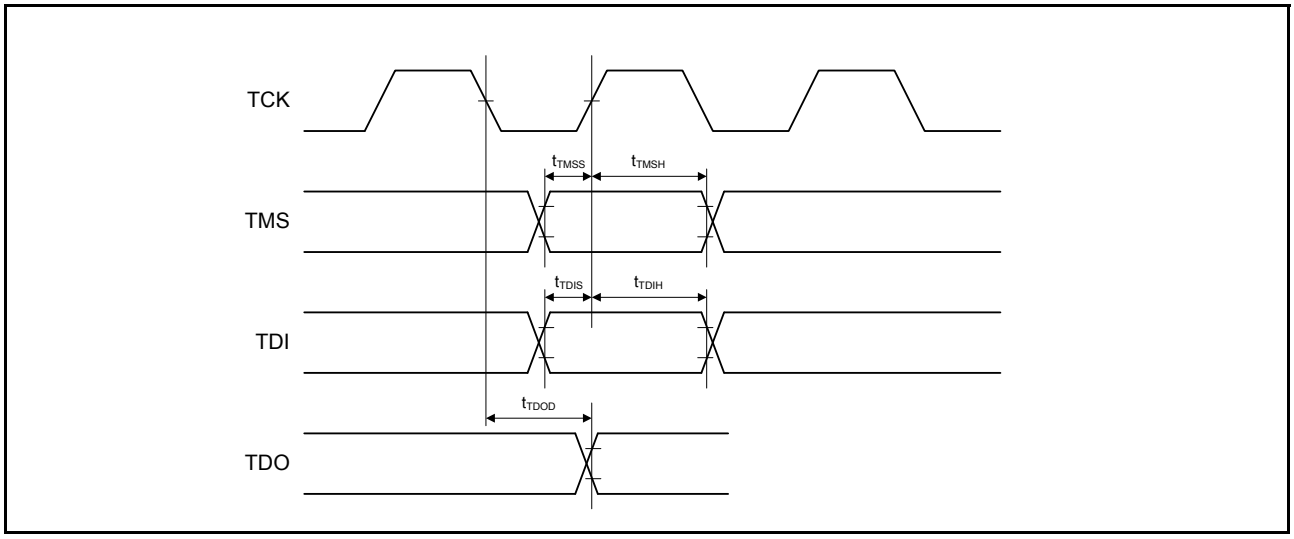

Figure 2.90 Boundary scan input/output timing

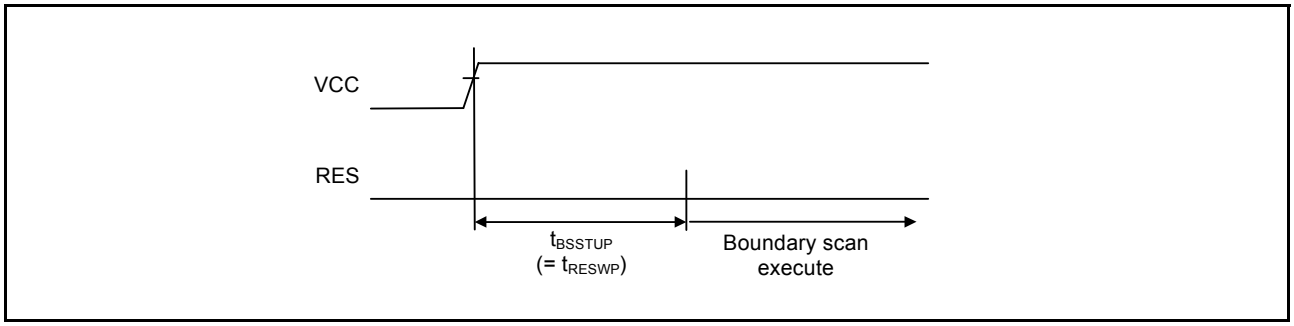

Figure 2.91 Boundary scan circuit start up timing

2.17 Joint European Test Action Group (JTAG)

Table 2.82 JTAG (Debug) characteristics (1)
Conditions: VCC = AVCC = 2.4 to 5.5 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	80	-	-	ns	Figure 2.92
TCK clock high pulse width	t_{TCKH}	35	-	-	ns	
TCK clock low pulse width	t_{TCKL}	35	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	16	-	-	ns	Figure 2.93
TMS hold time	t_{TMSH}	16	-	-	ns	
TDI setup time	t_{TDIS}	16	-	-	ns	
TDI hold time	t_{TDIH}	16	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	70	ns	

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