Renesas Electronics America Inc - R7FS3A77C3A01CFP#AA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 25x14b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c3a01cfp-aa1

Table 1.10 Analog (2/2)

Feature	Functional description
Operational Amplifier (OPAMP)	Operational amplifiers can be used to amplify small analog input voltages and output the amplified voltages. This MCU has a total of four differential operational amplifier units with two input pins and one output pin. See section 42, Operational Amplifier (OPAMP) in User's Manual.

Table 1.11 Human machine interfaces

Feature	Functional description
Segment LCD Controller (SLCDC)	The SLCDC provides the following functions: • Waveform A or B selectable • The LCD driver voltage generator can switch between internal voltage boosting method, capacitor split method, and external resistance division method • Automatic output of segment and common signals based on automatic display data register read • The reference voltage generated when operating the voltage boost circuit can be selected in 16 steps (contrast adjustment) • The LCD can be made to blink. See section 49, Segment LCD Controller/Driver (SLCDC) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising/falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode. See section 45, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) Calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB first or MSB first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 35, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) is used to compare, add, and subtract 16-bit data. See section 46, Data Operation Circuit (DOC) in User's Manual.

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 5 (SCE5)	• Security algorithm: - Symmetric algorithm: AES • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: GHASH

1.2 Block Diagram

Figure 1.1 shows the block diagram of this MCU superset. Individual devices within the group may have a subset of the features.

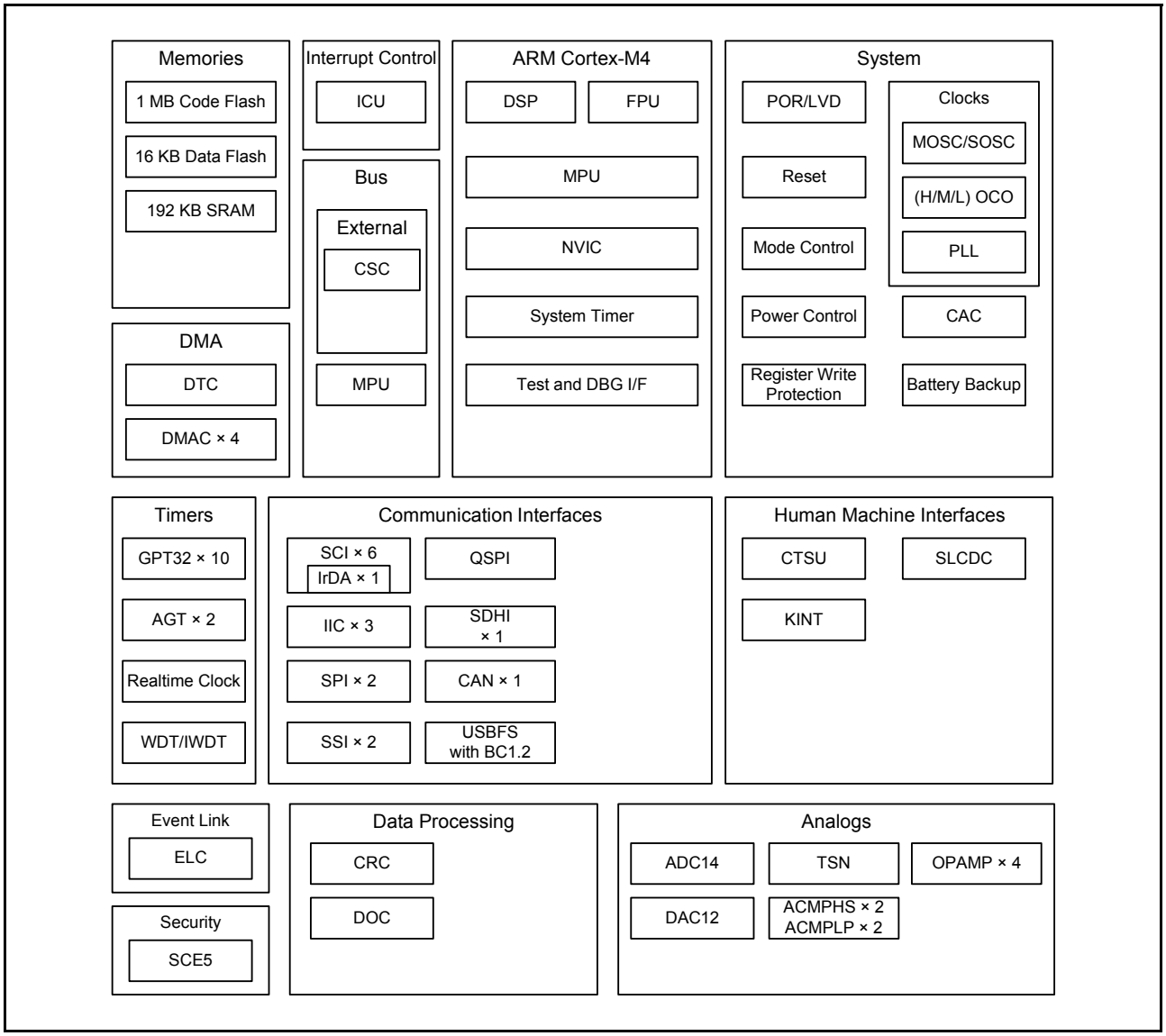

Figure 1.1 Block diagram

Function	Signal	I/O	Description
OPAMP	AMP0+ to AMP3+	Input	Analog voltage input pins.
	AMP0- to AMP3-	Input	Analog voltage input pins.
	AMP0O to AMP3O	Output	Analog voltage output pins.
CTSU	TS00, TS01, TS03 to TS22, TS26 to TS27, TS29 to TS35	Input	Capacitive touch detection pins (touch pins).
	TSCAP	-	Secondary power supply pin for the touch driver.
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
I/O ports	P000 to P015	I/O	General-purpose input/output pins.
	P100 to P115	I/O	General-purpose input/output pins.
	P200	Input	General-purpose input pin.
	P201 to P206, P212, P213	I/O	General-purpose input/output pins.
	P214, P215	Input	General-purpose input pins.
	P300 to P315	I/O	General-purpose input/output pins.
	P400 to P415	I/O	General-purpose input/output pins.
	P500 to P507, P511, P512	I/O	General-purpose input/output pins.
	P600 to P606, P608 to P614	I/O	General-purpose input/output pins.
	P700 to P705, P708 to P713	I/O	General-purpose input/output pins.
	P800 to P809	I/O	General-purpose input/output pins.
	P900 to P902	I/O	General-purpose input/output pins.
SLCDC	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD.
	CAPH, CAPL	I/O	Capacitor connection pin for the LCD controller/driver.
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver.
	SEG00 to SEG51	Output	Segment signal output pins for the LCD controller/driver.

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	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	P215/ XCIN	VCL	P403	P400	P000	10
9	USB_DM	USB_DP	P413	VSS	P213/ XTAL	P214/ XCOUT	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	VCC_US B_LDO	P411	P415	P708	P404	P003	P004	P002	8
7	P205	P204	P206	P408	P414	P406	P006	P007	P008	P005	7
6	VSS	VCC	P202	P203	P410	P402	P505	AVSS0	P011/ VREFL0	P010/ VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	P013/ VREFL	P012/ VREFH	5
4	P305	P304	P808	P306	P115	P601	P503	P100	P015	P014	4
3	P809	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	P603	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO/ SWO	P112	P608	VCC	VSS	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.7 Pin assignment for LGA 100-pin (Upper perspective view)

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VRERH = VREFH0 = 1.6 to AVCC0, VBATT = 1.6 to 3.6V, VSS = AVSS0 = VREFL = VREFL0 = VSS_USB = 0V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

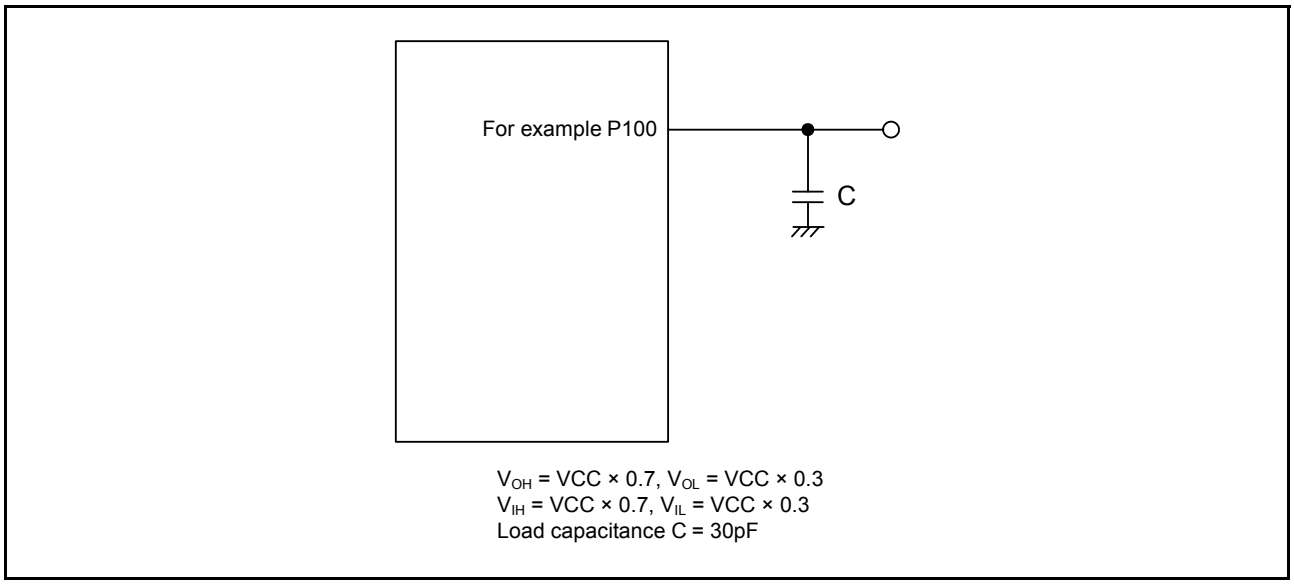


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pins to meet your conditions.

Table 2.5 I/O V_{IH}, V_{IL} (2)

Conditions: VCC = 1.6 to 2.7 V, AVCC0 = 1.6 to 2.7 V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	VCC + 0.3	V	-
		V_{IL}	–0.3	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	–0.3	-	VCC × 0.2		
	P000 to P015	V_{IH}	AVCC0 × 0.8	-	AVCC + 0.3		
		V_{IL}	–0.3	-	AVCC0 × 0.2		
	EXTAL D0 to D15 Input ports pins except for P000 to P015	V_{IH}	VCC × 0.8	-	VCC + 0.3		
		V_{IL}	–0.3	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	–0.3	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.01	-	-		

Note 1. P205, P206, P400 to P404, P407, P511, P512 (total 10 pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.6 I/O I_{OH}, I_{OL}
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P015, Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P115, P201 to P204, P300 to P315, P500 to P503, P600 to P606, P608 to P614, P800 to P809, P900 to P902 (total 67 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Other output pin*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (Max value per pin)	Ports P000 to P015, Ports P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P115, P201 to P204, P300 to P315, P500 to P503, P600 to P606, P608 to P614, P800 to P809, P900 to P902 (total 67 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	8.0	mA
	Other output pin*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P000 to P015		$\Sigma I_{OH\ (max)}$	-	-	–30	mA
			$\Sigma I_{OL\ (max)}$	-	-	30	mA
	Total of all output pin		$\Sigma I_{OH\ (max)}$	-	-	–60	mA
			$\Sigma I_{OL\ (max)}$	-	-	60	mA

Caution: To protect the reliability of this MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected with the port drive capability bit in PmnPFS register.
Note 2. This is the value when middle driving ability is selected with the port drive capability bit in PmnPFS register.
Note 3. Except for ports P200, P214, P215, which are input ports.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.7 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA
			V_{OL}	-	-	1.0		I_{OL} = 20 mA
	Ports P000 to P004, P010 to P015	Low drive	V_{OH}	AVCC0 – 0.8	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.8	-	-		I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.8	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	VCC – 0.8	-	-		I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B, SCL2, SDA2 (total 10 pins).
Note 2. This is the value when middle driving ability is selected with the port drive capability bit in PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for ports P200, P214, P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (2)
Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P000 to P004, P010 to P015	Low drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	VCC – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B, SCL2, SDA2 (total 10 pins).
Note 2. This is the value when middle driving ability is selected with the port drive capability bit in PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for ports P200, P214, P215, which are input ports.

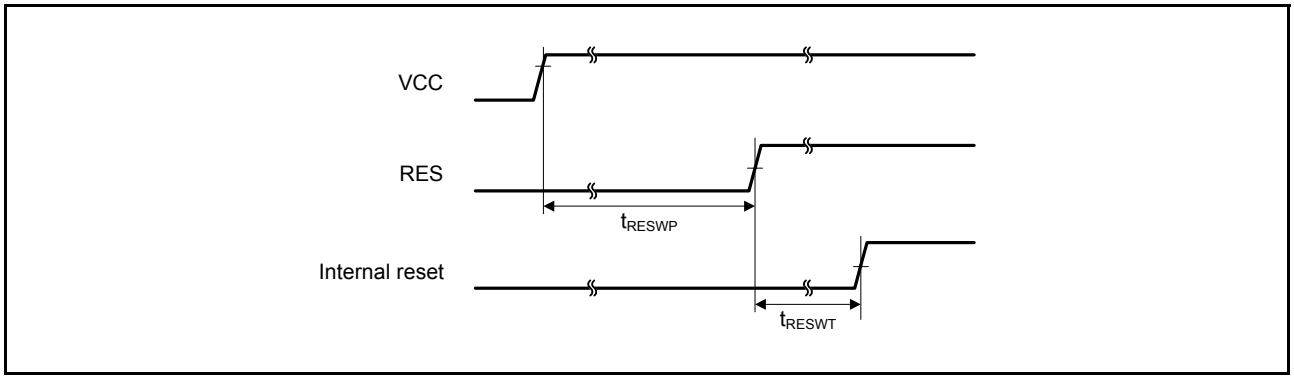


Figure 2.32 Reset input timing at power-on

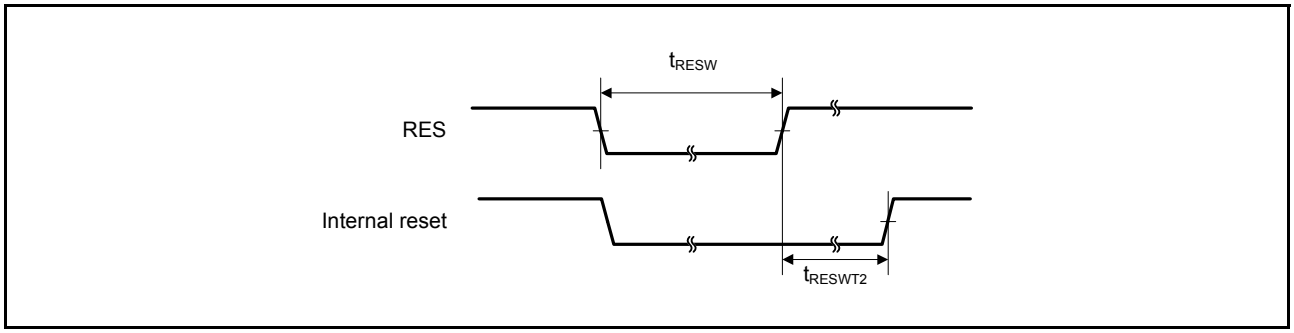


Figure 2.33 Reset input timing (1)

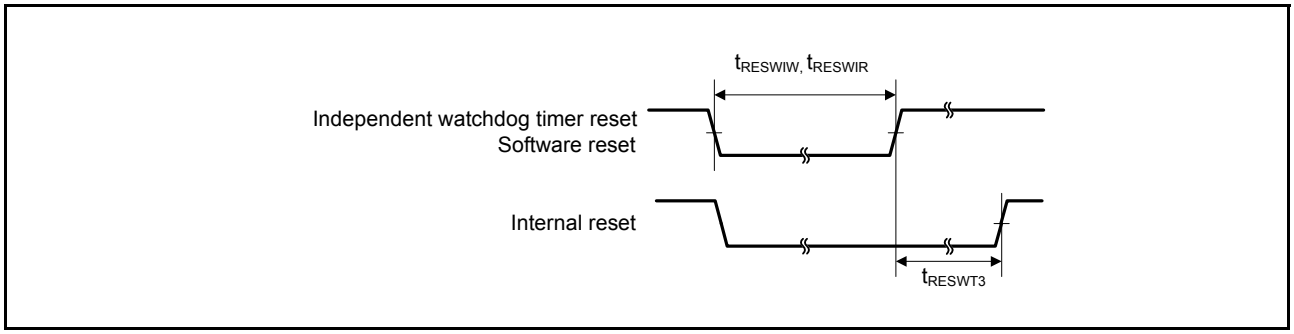
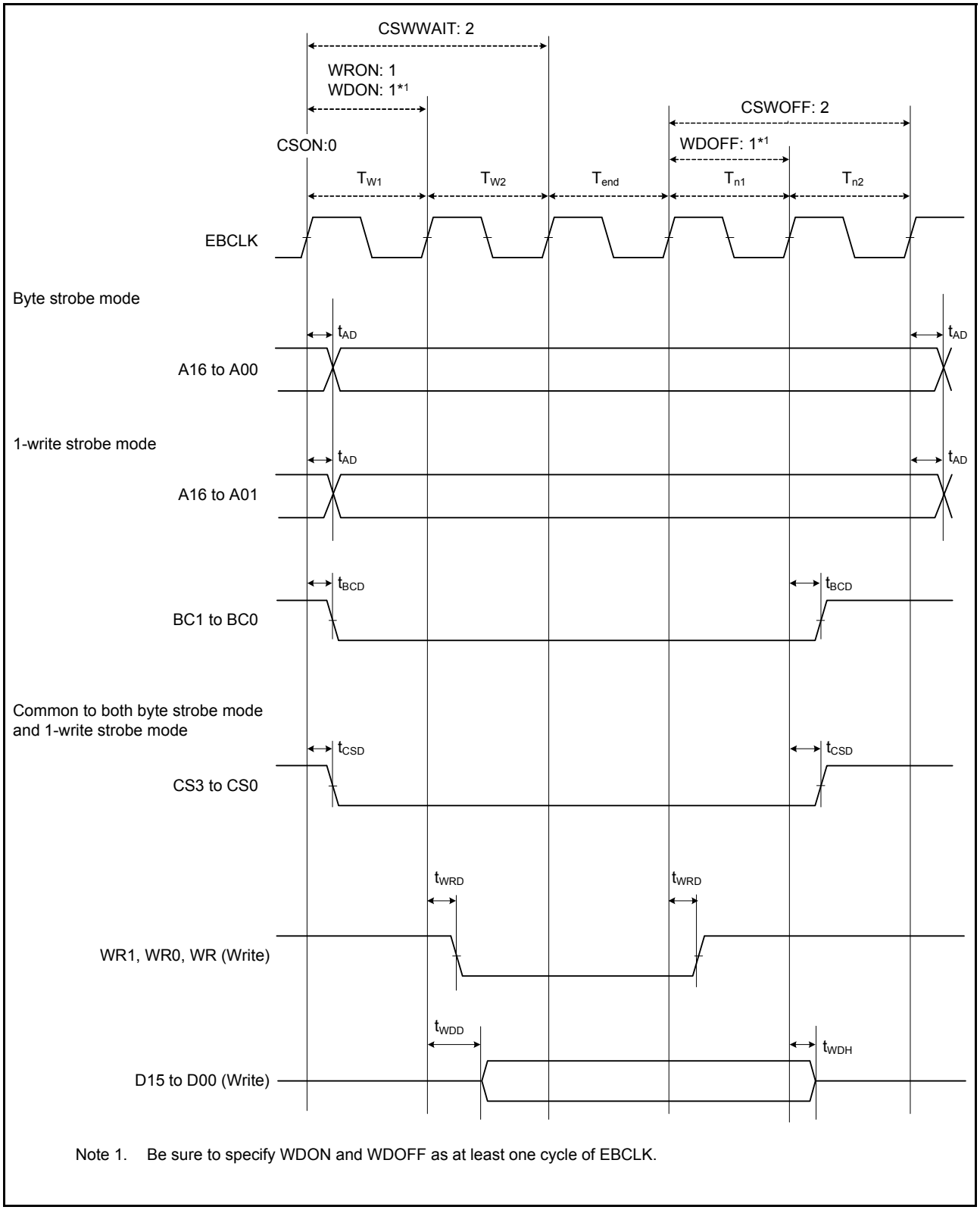


Figure 2.34 Reset input timing (2)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of EBCLK.

Figure 2.39 External bus timing/normal write cycle (bus clock synchronized)

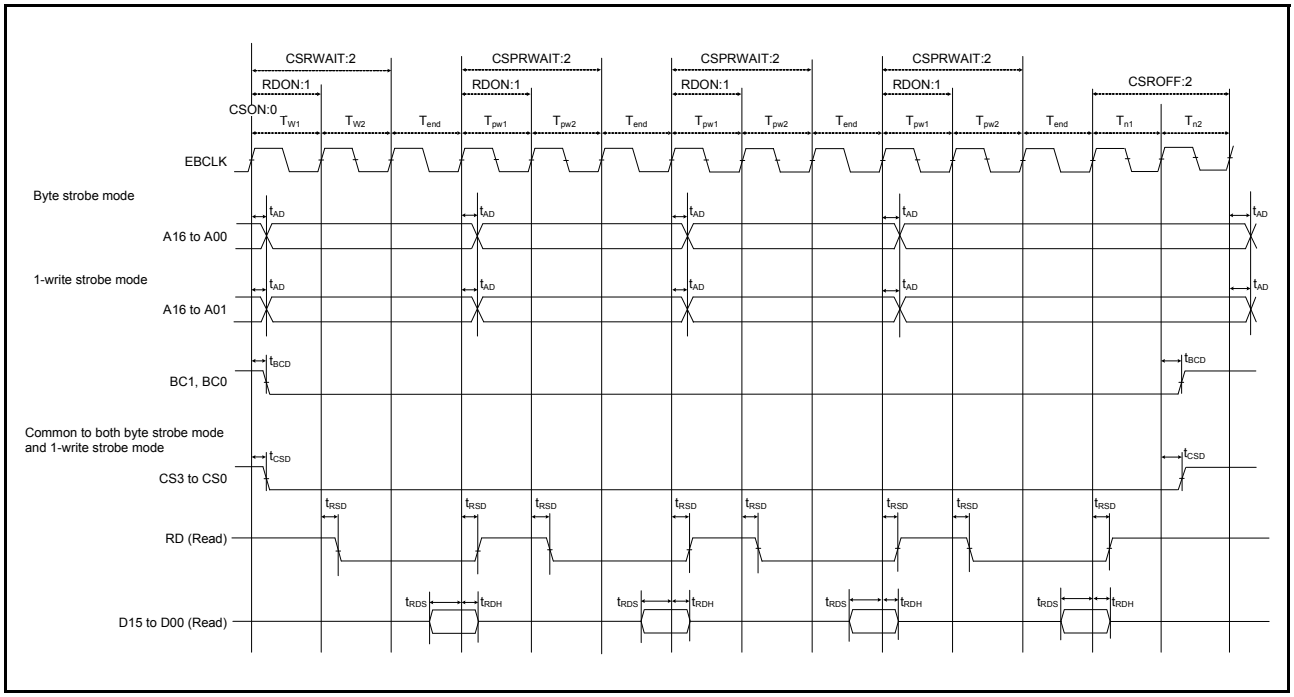
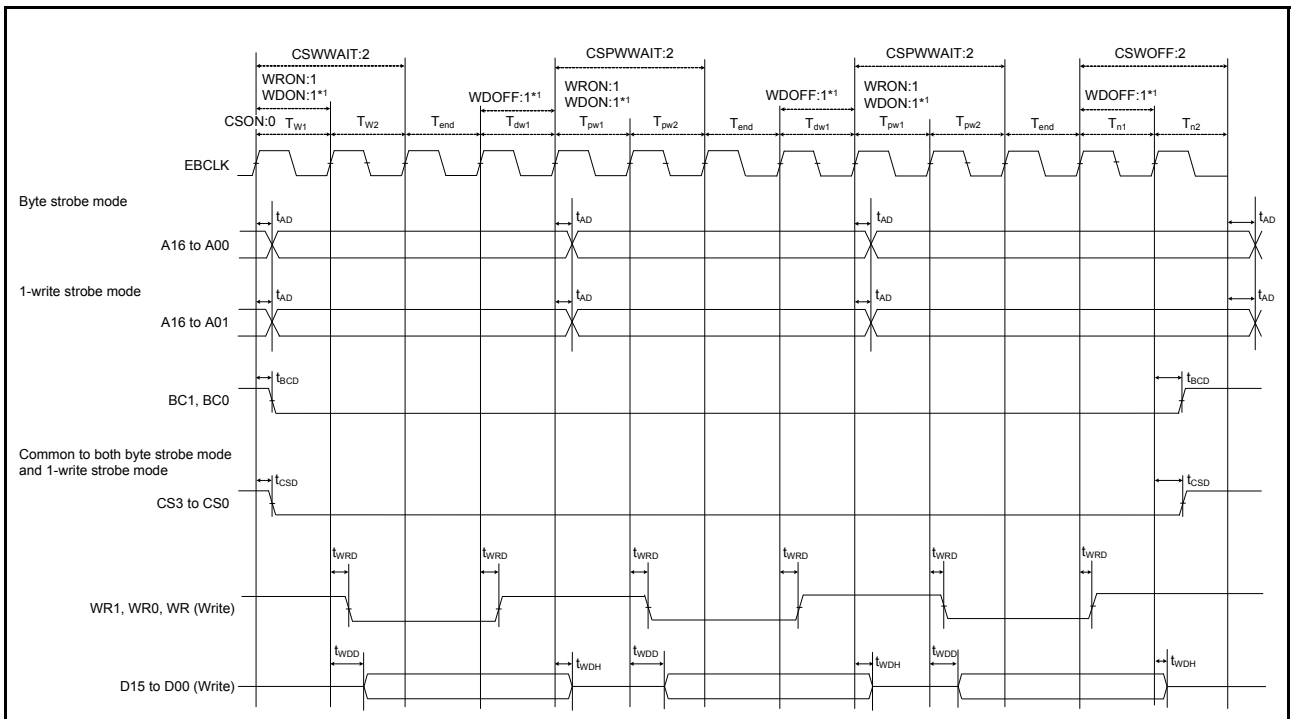


Figure 2.40 External bus timing/page read cycle (bus clock synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of EBCLK.

Figure 2.41 External bus timing/page write cycle (bus clock synchronized)

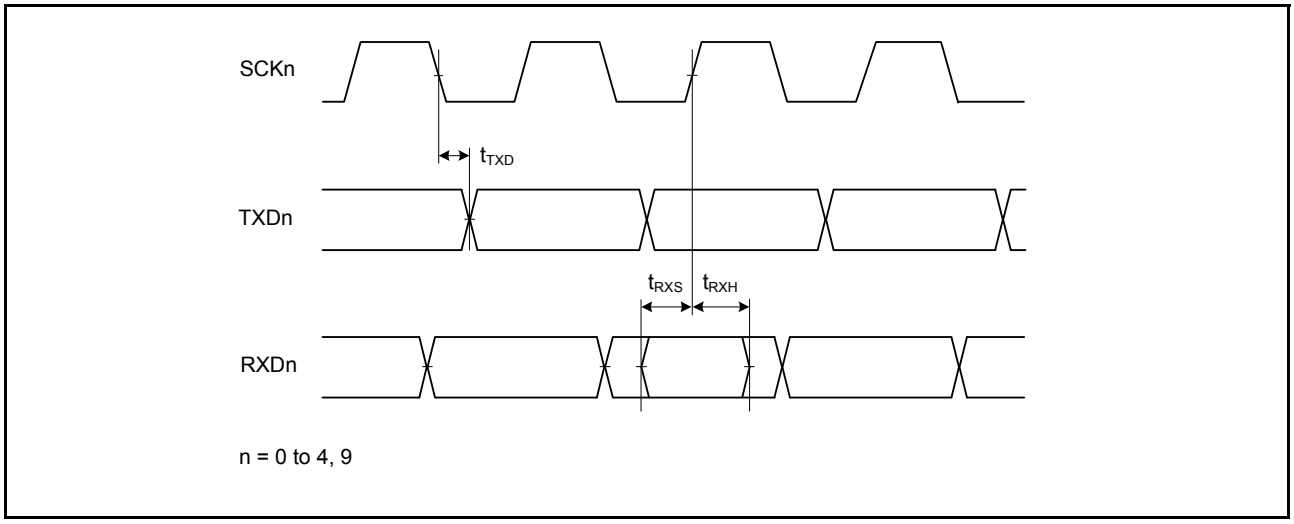


Figure 2.50 SCI input/output timing in clock synchronous mode

Table 2.38 SCI timing (2) (1/2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 1.6 to 5.5 V, VREFH0 = 2.7 V to AVCC0

Item				Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)			t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.51
	SCK clock cycle input (slave)				6	65536		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V or above	t_{SPCKr}, t_{SPCKf}	-	20	ns	
			1.6 V or above		-	30		
	Data input setup time	Master	2.7 V or above	t_{SU}	45	-	ns	Figure 2.52 to Figure 2.55
			2.4 V or above		55	-		
			1.8 V or above		80	-		
			1.6 V or above		105	-		
		Slave	2.7 V or above		40	-		
			1.6 V or above		45	-		
	Data input hold time	Master		t_H	33.3	-	ns	
		Slave			40	-		
	SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master	1.8 V or above	t_{OD}	-	40	ns	
			1.6 V or above		-	50		
		Slave	2.4 V or above		-	65		
			1.8 V or above		-	100		
			1.6 V or above		-	125		
	Data output hold time	Master	2.7 V or above	t_{OH}	–10	-	ns	
			2.4 V or above		–20	-		
			1.8 V or above		–30	-		
			1.6 V or above		–40	-		
		Slave			–10	-		
	Data rise and fall time	Master		t_{Dr}, t_{Df}	-	20	ns	
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

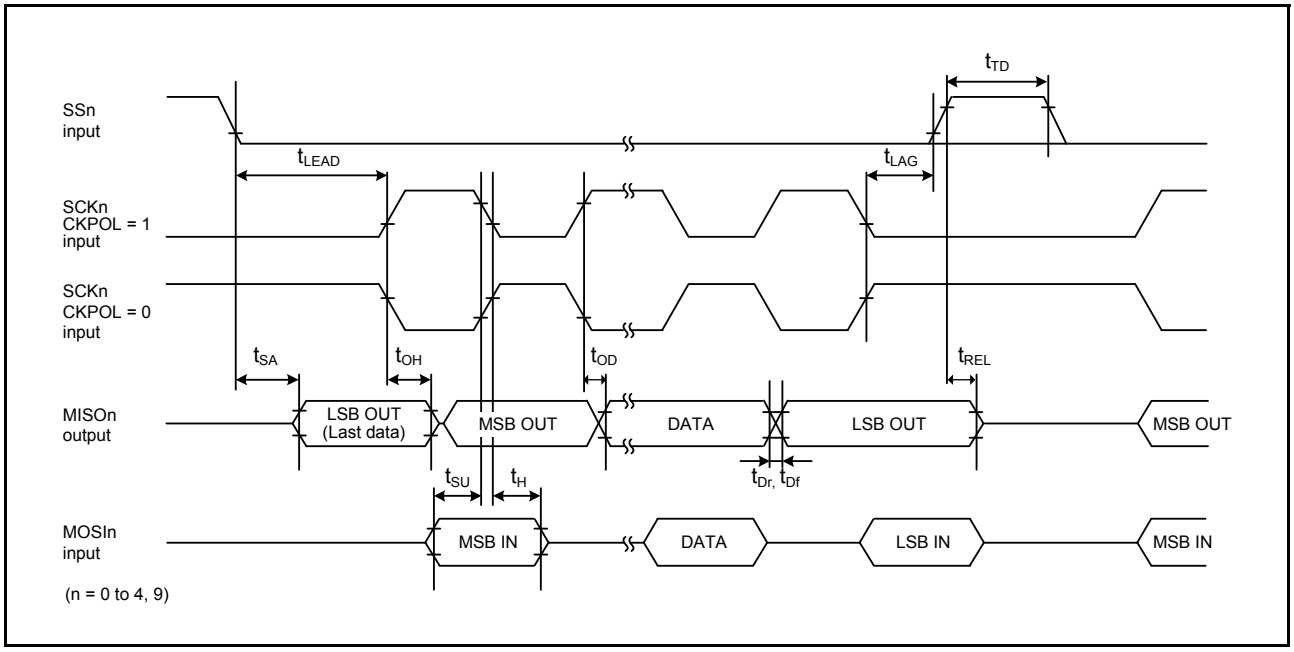


Figure 2.55 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.39 SCI timing (3)
Conditions: VCC = 2.7 to 5.5 V

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.56
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	-	300	ns	Figure 2.56
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	

Note 1. t_{IICcyc}: IIC internal reference clock (IICφ) Cycle, t_{Pcyc}: PCLKB cycle.
Note 2. Cb indicates the total capacity of the bus line.

2.3.15 CLKOUT Timing

Table 2.45 CLKOUT timing

Item			Symbol	Min	Max	Unit*1	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t_{Ccyc}	62.5	-	ns	Figure 2.72
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

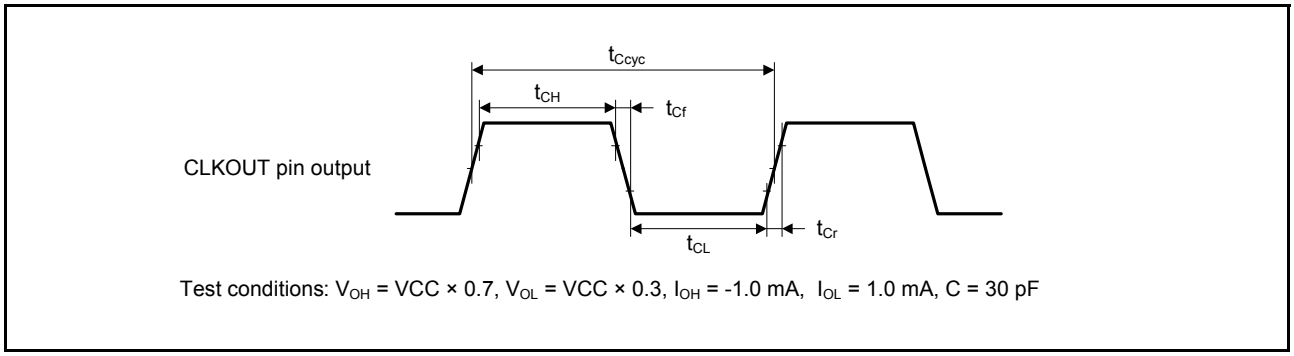


Figure 2.72 CLKOUT output timing

Table 2.48 A/D conversion characteristics (1) in high-speed mode (2/2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

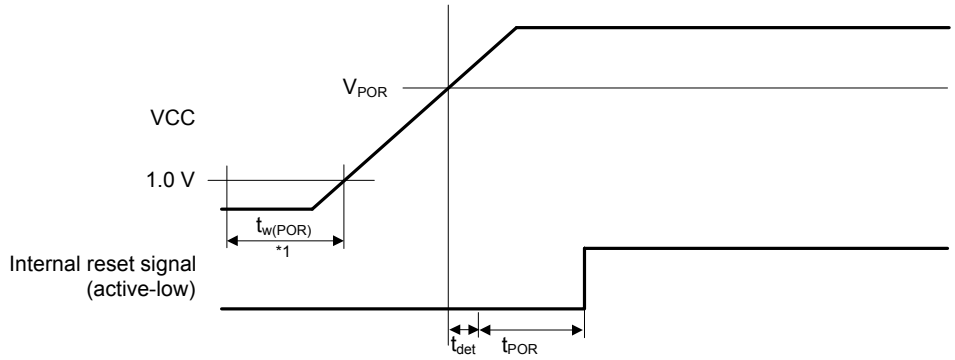
Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Table 2.49 A/D conversion characteristics (2) in high-speed mode (1/2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	48	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-



Note: $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(por)}$ for 1.0 ms or more.

Figure 2.81 Power-on reset timing

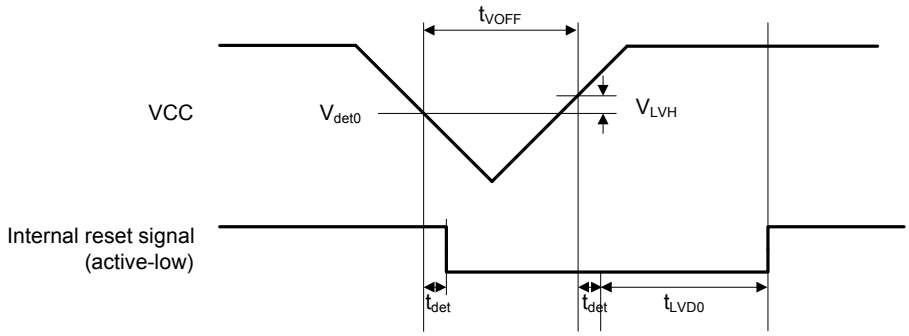


Figure 2.82 Voltage detection circuit timing (V_{det0})

2.13 Comparator Characteristics

Table 2.72 ACMPHS characteristics

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = 0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOCMP}	-	±5	±40	mV	-
Input voltage range	V_{ICMP}	0	-	AVCC0	V	-
Input signal cycle	t_{PCMP}	10	-	-	µs	-
Output delay time	t_d	-	50	100	ns	Input amplitude ± 100 mV
Stabilization wait time during input channel switching*1	t_{WAIT}	300	-	-	ns	Input amplitude ± 100 mV
Operation stabilization wait time*2	t_{CMP}	1	-	-	µs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	µs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period of time from when the comparator input channel is switched until the comparator is switched to output.
Note 2. Period of time from when the comparator operation is enabled (CMPCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.

Table 2.73 ACMPLP characteristics

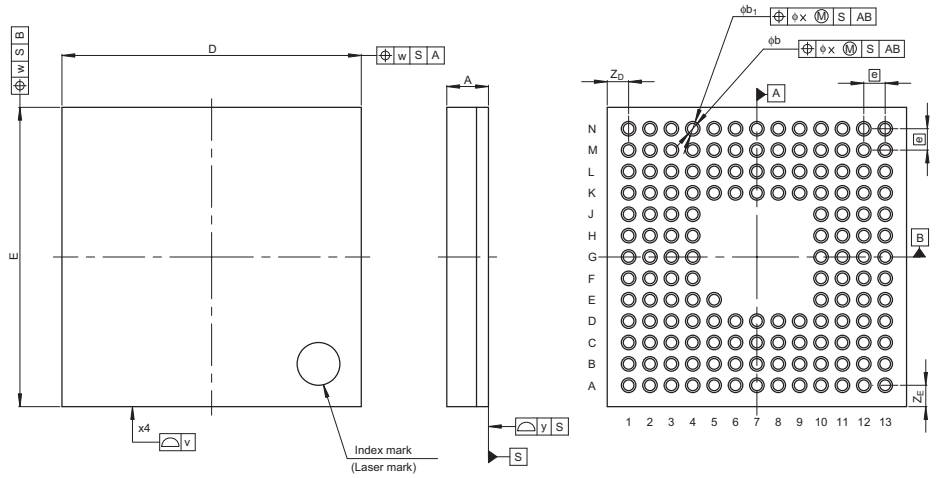
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		VREF	0	-	VCC –1.4	V	-
Input voltage range		VI	0	-	VCC	V	-
Output delay	High-speed mode	Td	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Low-speed mode		-	-	5	µs	
	Window mode		-	-	2	µs	
Offset voltage	High-speed mode	-	-	-	50	mV	-
	Low-speed mode	-	-	-	40	mV	-
	Window mode	-	-	-	60	mV	-
Internal reference voltage for window mode		VRFH	-	0.76 × VCC	-	V	-
		VRFL	-	0.24 × VCC	-	V	-
Operation stabilization wait time		T_{cmp}	100	-	-	µs	-

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g

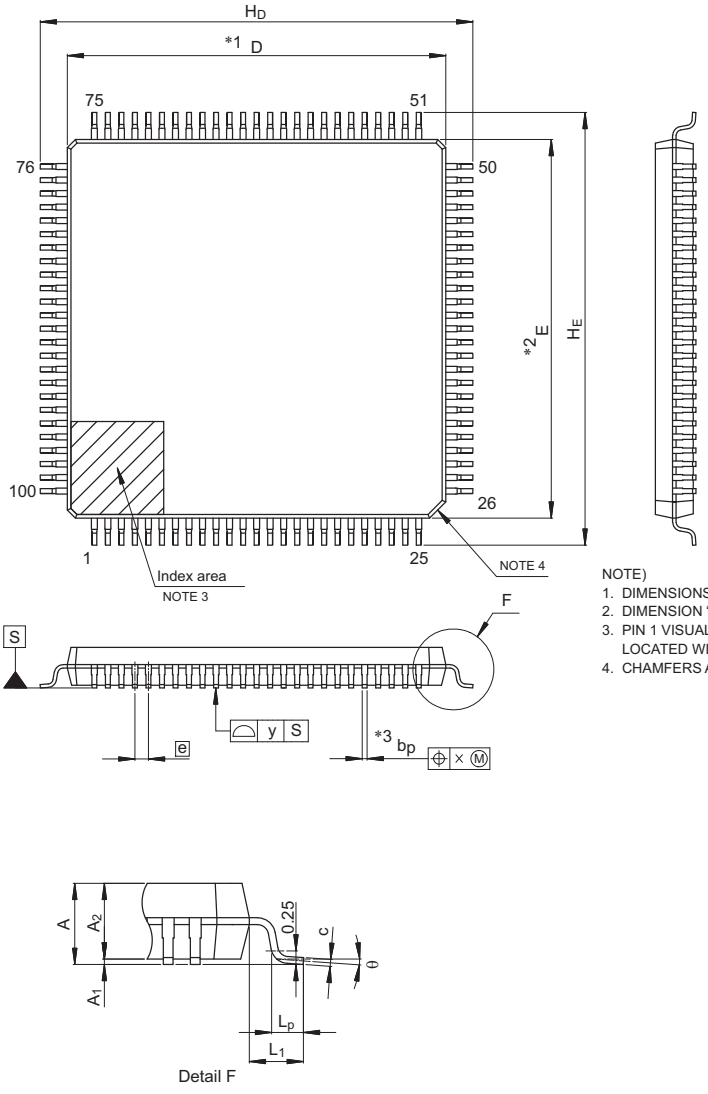


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.1 LGA 145-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 LQFP 100-pin

Revision History	S3A7 Datasheet

Rev.	Date	Chapter	Summary
0.80	Oct. 12, 2015	—	First Edition issued
0.85	Dec. 15, 2015	—	Second Edition issued
1.00	Feb. 23, 2016	section 1, Overview	Updated channel number of CTSU in Table 1.14, Function comparison
			Updated pin name of CTSU in section 1.5, Pin Functions
			Updated pin name of CTSU in section 1.7, Pin Lists
		section 2, Electrical Characteristics	Added section 2.17, Joint European Test Action Group (JTAG) and section 2.17.1, Serial Wire Debug (SWD) in section 2, Electrical Characteristics
			Updated input voltage in Table 2.1, Absolute maximum ratings
			Added section 2.2.5, I/O Pin Output Characteristics of Low Drive Capacity
			Updated Table 2.6, I/O I_{OH}, I_{OL} in section 2.2.3, I/O I_{OH}, I_{OL} to change from normal drive to low drive
			Changed Note 6 to Note 5. in Table 2.11, Operating and standby current (1)
			Updated the conditions in Table 2.13, Operating and standby current (3)
			Updated Note 2. in Table 2.17, Operation frequency value in high-speed operating mode
			Updated Note 2. in Table 2.18, Operation frequency value in middle-speed mode
			Removed the 2nd note from Table 2.19, Operation frequency value in low-speed mode
			Updated Note 2. in Table 2.20, Operation frequency value in low-voltage mode
			Updated Table 2.22, Clock timing
			Updated the condition of the I/O Ports in Table 2.35, I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing
			Removed the 2nd note from Table 2.37, SCI timing (1)
			Updated the conditions in Table 2.38, SCI timing (2)
			Updated Figure 2.59, SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)
			Added the conditions in Table 2.42, IIC timing
			Updated Figure 2.68, SSI data transmit/receive timing (SSICR.SCKP = 0)
			Updated the Quantization error in the following tables: · Table 2.48, A/D conversion characteristics (1) in high-speed mode · Table 2.49, A/D conversion characteristics (2) in high-speed mode · Table 2.50, A/D conversion characteristics (3) in high-speed mode · Table 2.51, A/D conversion characteristics (4) in low power mode · Table 2.52, A/D conversion characteristics (5) in low power mode
			Updated Table 2.55, 14-Bit A/D converter channel classification
			Updated Table 2.64, Battery Backup Function Characteristics
			Deleted VLCD = 0Dh to 13h in Table 2.70, Internal voltage boosting method LCD characteristics
			Updated the response time in Table 2.72, ACMPHS characteristics
			Added the temperature in Table 2.77, Code flash characteristics (3)
			Added the temperature in Table 2.80, Data flash characteristics (3)
		All	Deleted # from pin names