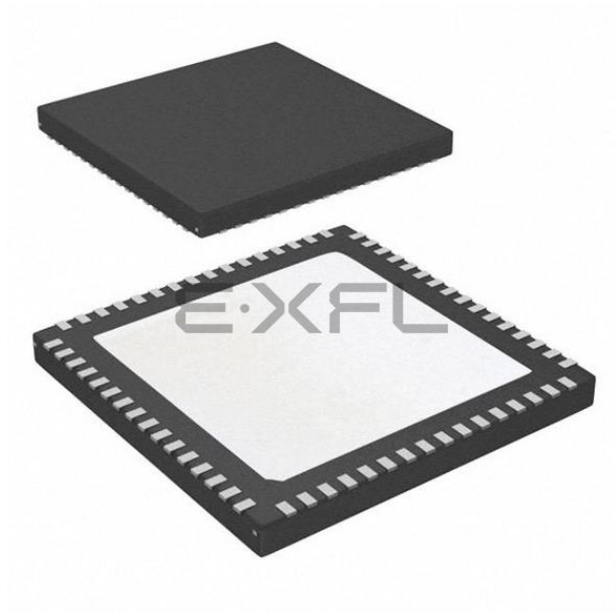
Renesas Electronics America Inc - R7FS3A77C3A01CNB#AC1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, MMC/SD, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a77c3a01cnb-ac1

Table 1.3 System (1/2)

Feature	Functional description
Operating mode	Two operating modes: - Single-chip mode - SCI/USB boot mode. See section 3, Operating Modes in User's Manual.
Reset	This MCU has 14 types of resets: • RES pin reset • Power-on reset • VBATT selected voltage power on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clock	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) is used to check the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Low Power Mode	This MCU has several functions for reducing power consumption, such as setting clock dividers, controlling EBCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Mode in User's Manual.
Battery Backup Function	This MCU has a battery backup function that can be partly powered by a battery. The battery powered area includes RTC/AGT/SOSC/LOCO/Wakeup Control/Backup Memory/VBATT_R Low Voltage Detection/Switch between VCC/VBATT. During normal operation, the battery powered area is powered by the main power supply which is the VCC pin. When a VCC voltage drop is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 12, Battery Backup Function in User's Manual.
Register Write Protection	The Register Write Protection function protects important registers from being overwritten due to software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	This MCU incorporates two memory protection units and provide a CPU stack pointer monitor function. See section 16, Memory Protection Unit (MPU) in User's Manual.

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pin.
	GTIOC0A to GTIOC9A, GTIOC0B to GTIOC9B	I/O	Input capture, Output capture, or PWM output pin.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable.
	AGTIO0, AGTIO1	I/O	External event input and pulse output.
	AGTO0, AGTO1	Output	Pulse output.
	AGTOA0, AGTOA1	Output	Output compare match A output.
	AGTOB0, AGTOB1	Output	Output compare match B output.
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
SCI	SCK0 to SCK4, SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0 to RXD4, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0 to TXD4, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0 to CTS4_RTS4, CTS9_RTS9	I/O	Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active LOW.
	SCL0 to SCL4, SCL9	I/O	Input/output pins for the IIC clock (simple IIC).
	SDA0 to SDA4, SDA9	I/O	Input/output pins for the IIC data (simple IIC).
	SCK0 to SCK4, SCK9	I/O	Input/output pins for the clock (simple SPI).
	MISO0 to MISO4, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI).
	MOSI0 to MOSI4, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI).
	SS0 to SS4, SS9	Input	Slave-select input pins (simple SPI), active LOW.
IIC	SCL0 to SCL2	I/O	Input/output pins for clock.
	SDA0 to SDA2	I/O	Input/output pins for data.
SSI	SSISCK0	I/O	SSI serial bit clock pin.
	SSISCK1		
	SSIWS0	I/O	Word select pins.
	SSIWS1		
	SSITXD0	Output	Serial data output pins.
	SSIRXD0	Input	Serial data input pins.
	SSIDATA1	I/O	Serial data input/output pins.
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock).

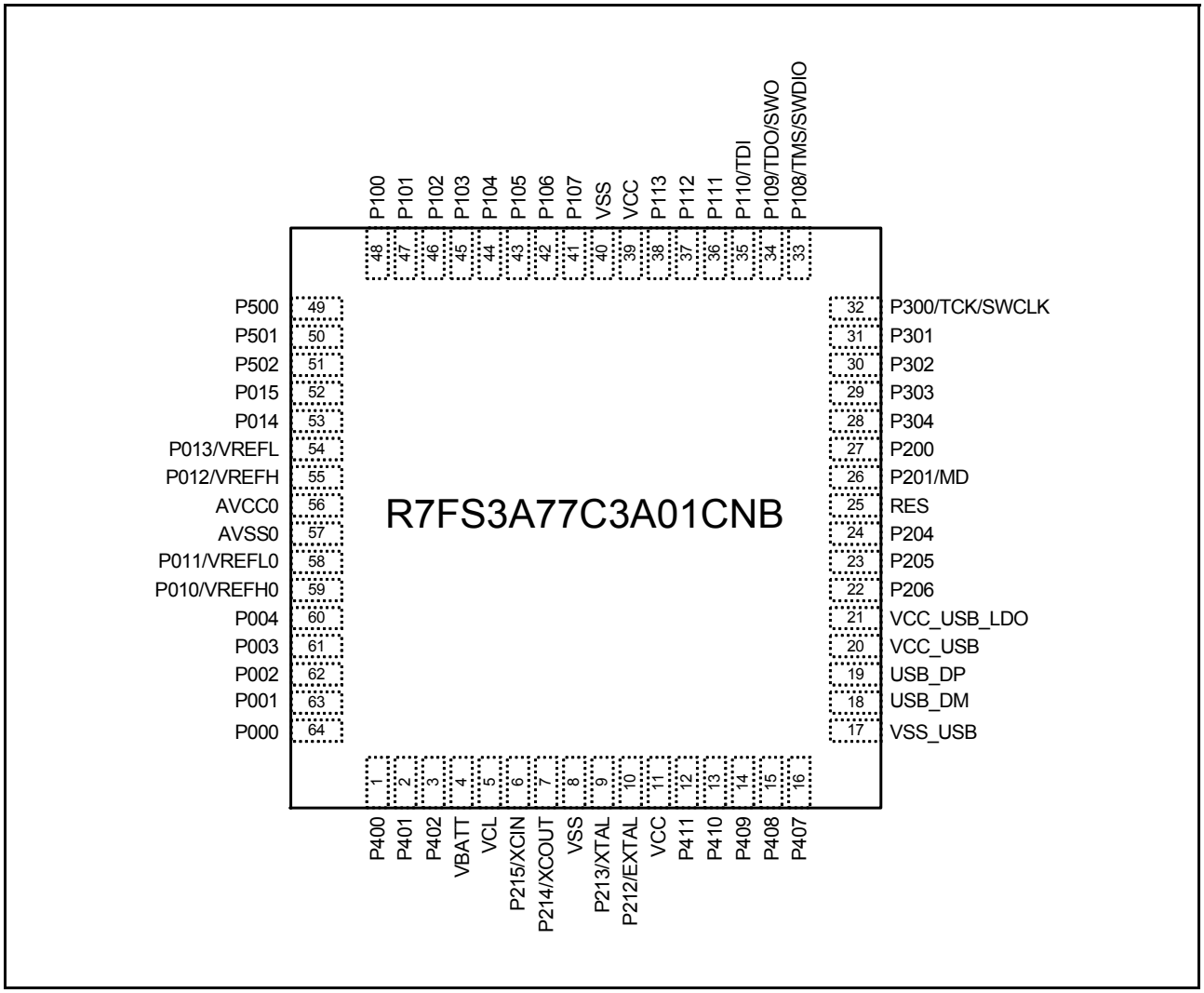


Figure 1.9 Pin assignment for QFN 64-pin (Upper perspective view)

1.7 Pin Lists

Pin number							Power, System, Clock, Debug, CAC, VBATT	I/O ports	External bus	Timers				Communication interfaces						Analogs			HMI		
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64				AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSI	SDHI	ADC14	DAC12, OPAMP	ACMPHS, ACMPLP	SLCDC	CTSU	Interrupt
N13	1	L11	1	J10	1	1		P400				GTIOC6A_A			SCK4_B	SCL0_A		AUDIO_CLK						TS20	IRQ0
L11	2	K11	2	J9	2	2		P401			GTETRGA_B	GTIOC6B_A		CTX0_B	CTS4_RTS4_B/SS4_B	SDA0_A								TS19	IRQ5
M13	3	J10	3	F6	3	3	VBATWIO0	P402		AGTIO0_B/AGTIO1_B			RTCIC0	CRX0_B										TS18	IRQ4
K11	4	J11	4	H10			VBATWIO1	P403		AGTIO0_C/AGTIO1_C		GTIOC3A_B	RTCIC1					SSISCK0_A						TS17	
L12	5	H9	5	G8			VBATWIO2	P404				GTIOC3B_B	RTCIC2					SSIWS0_A						TS16	
L13	6	H10	6	H9				P405				GTIOC1A_B						SSITXD0_A						TS15	
J10	7	H11	7	F7				P406				GTIOC1B_B						SSIRXD0_A						TS14	
H10	8	G6						P700				GTIOC5A_B												TS32	
K12	9	G7						P701				GTIOC5B_B												TS33	
K13	10	G8						P702				GTIOC6A_B												TS34	
J11	11							P703				GTIOC6B_B													
H11	12							P704																	
G11	13							P705																	
J12	14	G10	8	G9	4	4	VBATT																		
J13	15	G11	9	G10	5	5	VCL																		
H13	16	F11	10	F10	6	6	XCIN	P215																	
H12	17	F10	11	F9	7	7	XCOUT	P214																	
F12	18	G9	12	D9	8	8	VSS																		
G12	19	E10	13	E9	9	9	XTAL	P213			GTETRGC_A				TXD1_A/MOSI1_A/SDA1_A										IRQ2
G13	20	E11	14	E10	10	10	EXTAL	P212		AGTEE1	GTETRGD_A				RXD1_A/MISO1_A/SCL1_A										IRQ3
F13	21	F9	15	D10	11	11	VCC																		
G10	22							P713				GTIOC2A_B													
F11	23							P712				GTIOC2B_B													
E13	24							P711							CTS1_RTS1_B/SS1_B										
E12	25	F8						P710							SCK1_B									TS35	
F10	26	F7						P709							TXD1_B/MOSI1_B/SDA1_B									TS13	IRQ10
D13	27	E9	16	F8			CACREF_B	P708							RXD1_B/MISO1_B/SCL1_B			SSLA3_B						TS12	IRQ11
E11	28	D10	17	E8				P415										SSLA2_B						TS11	
D12	29	D11	18	E7				P414										SSLA1_B		SD0WP				TS10	
E10	30	E8	19	C9				P413			GTOUUP_B				CTS0_RTS0_B/SS0_B			SSLA0_B		SD0CLK				TS09	
C13	31	D9	20	C10				P412			GTOULO_B				SCK0_B		RSPCKA_B			SD0CMD				TS08	

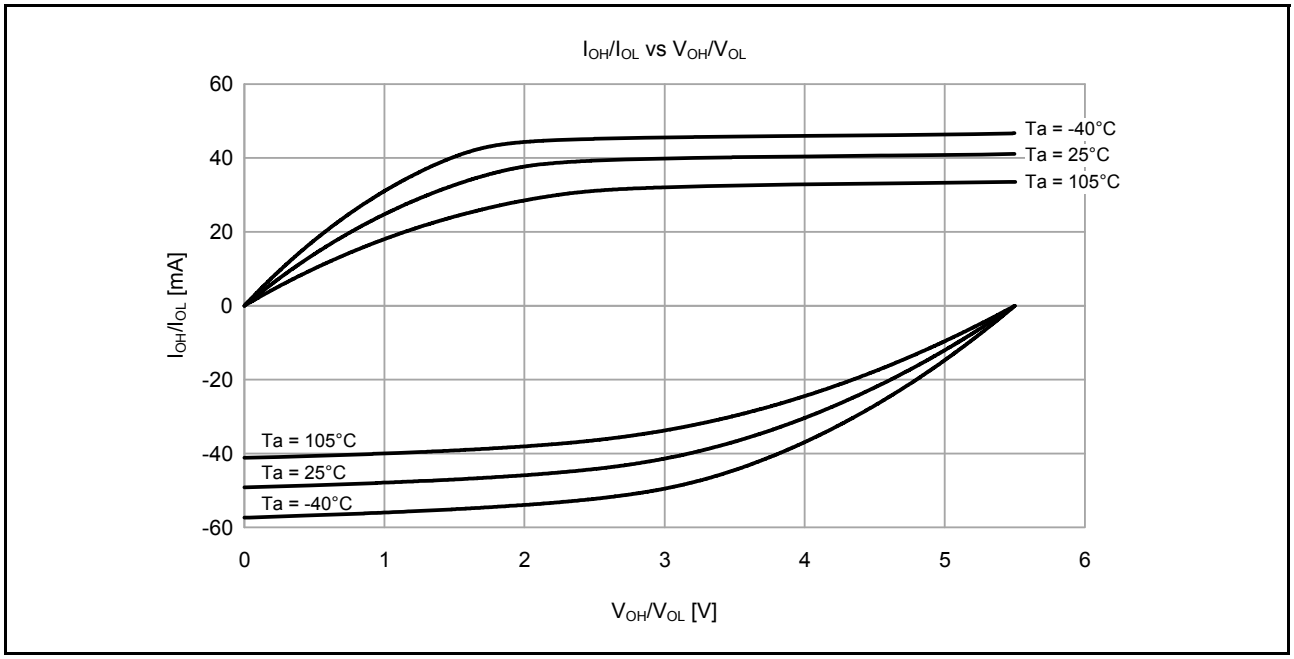


Figure 2.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When Low drive output is Selected (Reference Data)**

2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

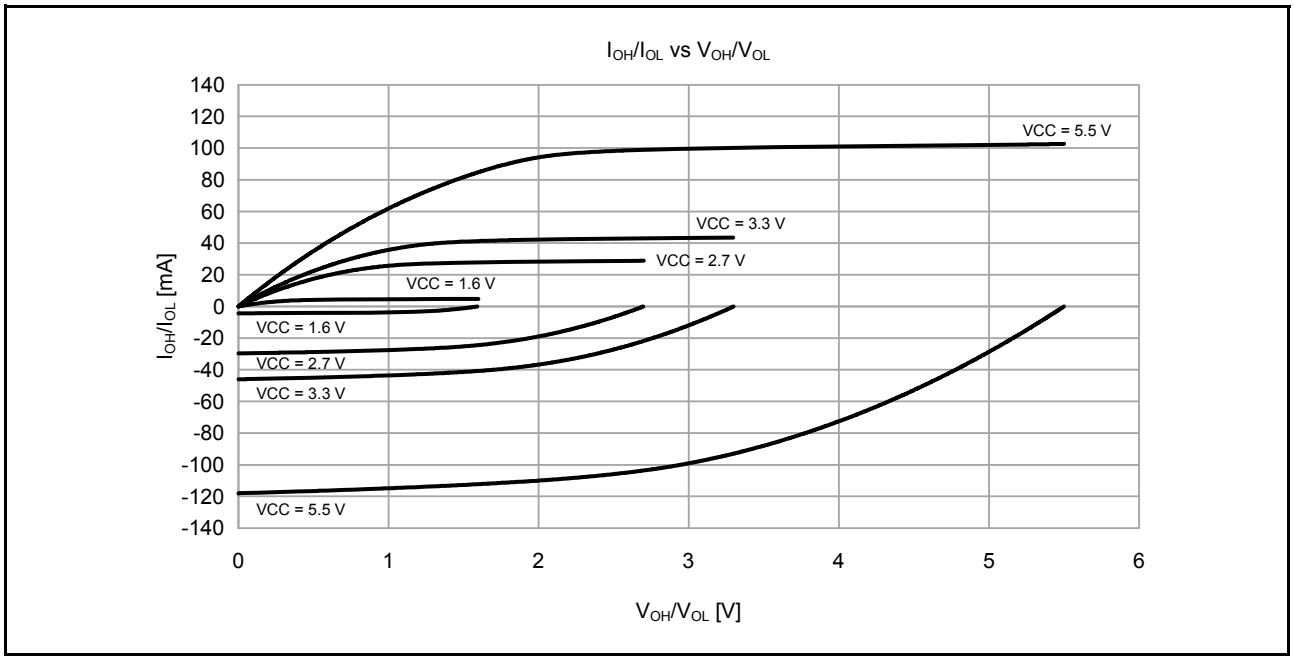


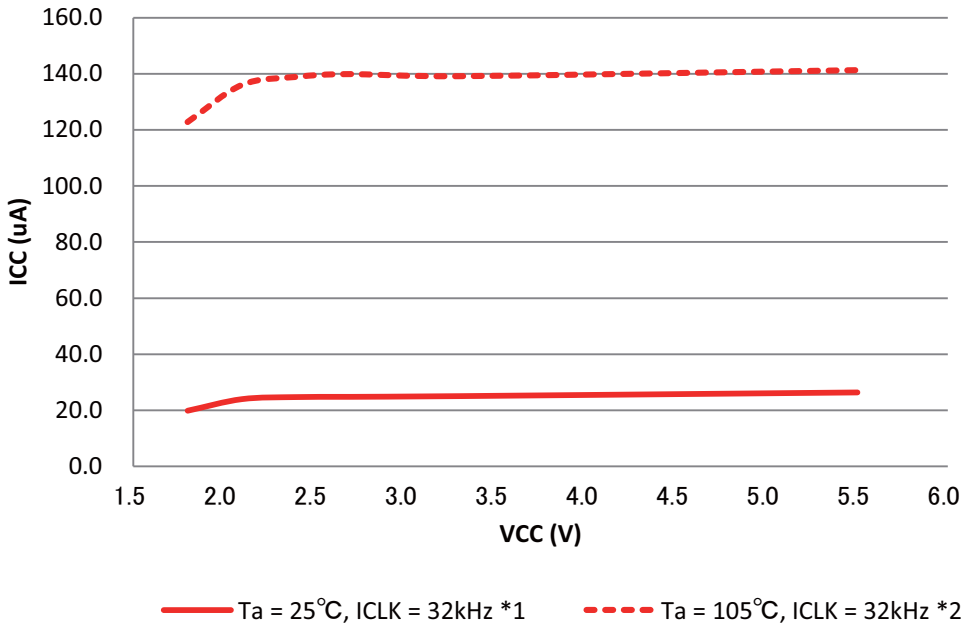
Figure 2.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at Ta = 25°C When Middle drive output is Selected (Reference Data)**

Table 2.11 Operating and standby current (1) (2/2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.7	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 1 MHz		1.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	3.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.4	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		1.3	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 4 MHz	I_{CC}	2.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		3.0	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		4.5	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	11.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		2.0	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		4.0	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	13.5	-	µA	*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		25.0	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	214.1		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		9.5	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		21.0	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 7. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.
Note 8. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK, BCLK, and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.21 Voltage dependency in Subosc-speed mode (reference data)

Table 2.12 Operating and standby current (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Item			Symbol	Typ*4	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.9	6.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
		T_a = 55°C		1.6	12.2		
		T_a = 85°C		4.8	27.1		
		T_a = 105°C		12.2	66.7		
		T_a = 25°C		1.1	7.5		PSMCR.PSMC[1:0] = 00b (All SRAM on)
		T_a = 55°C		2.2	17.0		
		T_a = 85°C		7.5	43.3		
		T_a = 105°C		19.6	105.9		
	Increment for RTC operation with low-speed on-chip oscillator*3			0.5	-		-
	Increment for RTC operation with sub-clock oscillator*3			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.6	-		SOMCR.SODRV[1:0] are 00b (Normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.
Note 4. VCC = 3.3 V.

Table 2.18 Operation frequency value in middle-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	EBCLK pin output	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	8	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

Table 2.19 Operation frequency value in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK)*1, *3	1.8 to 5.5 V		0.032768	-	1	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	1	
	External bus clock (BCLK)*3	1.8 to 5.5 V		-	-	1	
	EBCLK pin output	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.

Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.

Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

2.3.2 Clock Timing

Table 2.22 Clock timing (1/2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	VCC = 2.7 V or above	t_{Bcyc}	83.3	-	-	ns	Figure 2.26
	VCC = 1.8 V or above		125	-	-		
	VCC = 1.6 V or above		500	-	-		
EBCLK pin output high pulse width	VCC = 2.7 V or above	t_{CH}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output low pulse width	VCC = 2.7 V or above	t_{CL}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EBCLK pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 2.27
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	µs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	µs	Figure 2.28
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	µs	-

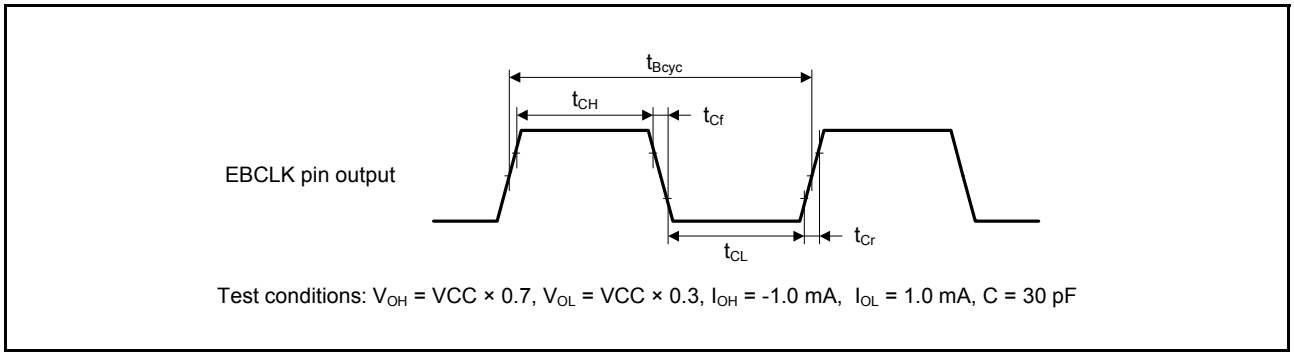


Figure 2.26 EBCLK pin output timing

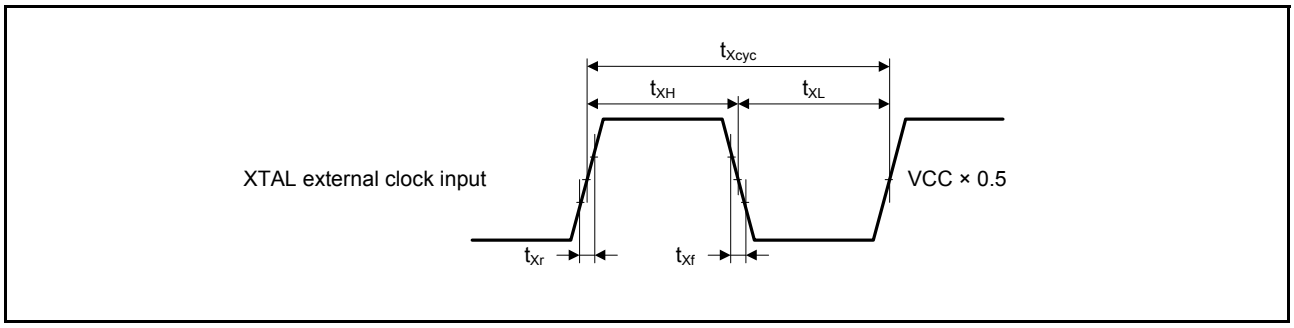


Figure 2.27 XTAL external clock input timing

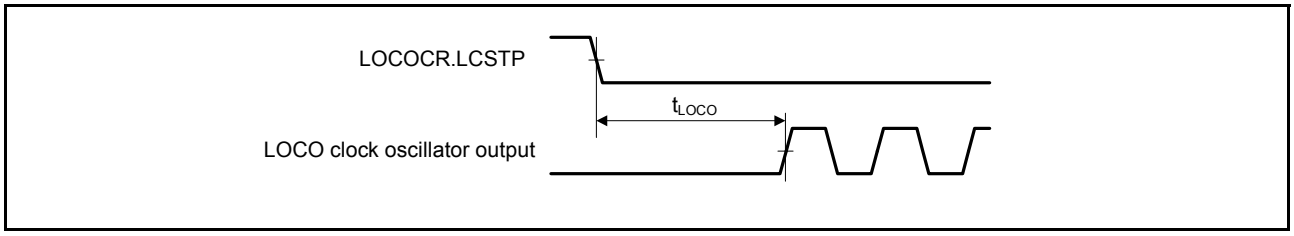


Figure 2.28 LOCO clock oscillation start timing

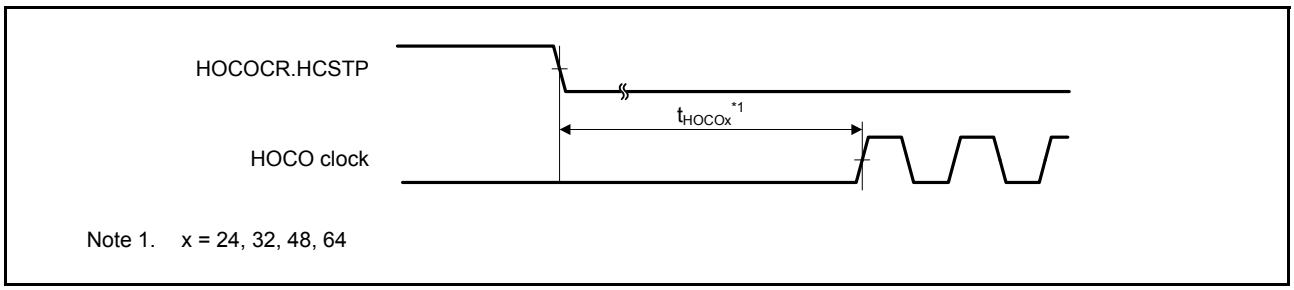


Figure 2.29 HOCO clock oscillation start timing (started by setting HOCOCR.HCSTP bit)

2.3.6 Bus Timing

Table 2.31 Bus timing (1)
Conditions: EBCLK pin ≤ 12 MHz (package with 145 to 100 pins) (BCLK: up to 24 MHz)
VCC = AVCC0 = 2.7 to 5.5 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

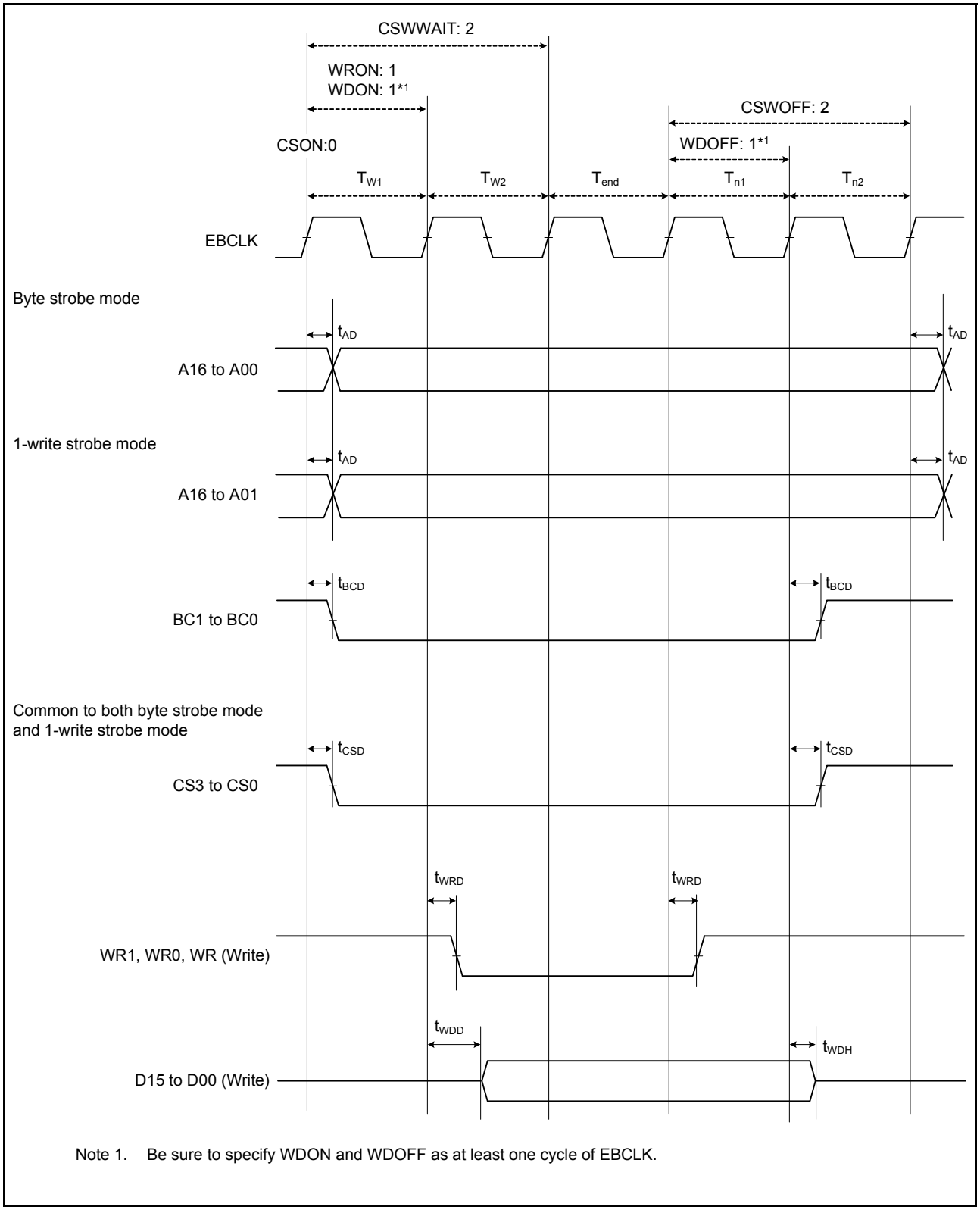
Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	37	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	37	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.32 Bus timing (2)
Conditions: EBCLK pin ≤ 8 MHz (package with 145 to 100 pins) (BCLK: up to 8 MHz)
VCC = AVCC0 = 2.4 to 2.7 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	45	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	45	-	ns	Figure 2.42
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.33 Bus timing (3)
Conditions: EBCLK pin ≤ 4 MHz (package with 145 to 100 pins) (BCLK: up to 4 MHz)
VCC = AVCC0 = 1.8 to 2.4 V
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	90	ns	Figure 2.38 to Figure 2.41
Byte control delay	t_{BCD}	-	90	ns	
CS delay	t_{CSD}	-	90	ns	
RD delay	t_{RSD}	-	90	ns	
Read data setup time	t_{RDS}	70	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	90	ns	
Write data delay	t_{WDD}	-	90	ns	
Write data hold time	t_{WDH}	0	-	ns	



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of EBCLK.

Figure 2.39 External bus timing/normal write cycle (bus clock synchronized)

Table 2.40 SPI timing (2/2)

Conditions: Middle drive output is selected in the Drive Strength Control in PmnPFS register

Item				Symbol	Min	Max	Unit*1	Test conditions
SPI	Data output delay	Master	2.7 V or above	t_{OD}	-	14	ns	Figure 2.58 to Figure 2.63 C = 30pF
			2.4 V or above		-	20		
			1.8 V or above		-	25		
			1.6 V or above		-	30		
		Slave	2.7 V or above		-	50		
			2.4 V or above		-	60		
			1.8 V or above		-	85		
			1.6 V or above		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	-		
	MOSI and MISO rise and fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
			1.6 V or above		-	30		
		Input			-	1	µs	
	SSL rise and fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
			1.6 V or above		-	30		
		Input			-	1	µs	
	Slave access time		2.7 V or above	t_{SA}	-	$2 \times t_{Pcyc} + 50$	ns	Figure 2.62 and Figure 2.63 C = 30pF
			2.4 V or above		-	$2 \times t_{Pcyc} + 60$		
			1.8 V or above		-	$2 \times t_{Pcyc} + 85$		
			1.6 V or above		-	$2 \times t_{Pcyc} + 110$		
	Slave output release time		2.7 V or above	t_{REL}	-	$2 \times t_{Pcyc} + 50$	ns	
			2.4 V or above		-	$2 \times t_{Pcyc} + 60$		
			1.8 V or above		-	$2 \times t_{Pcyc} + 85$		
			1.6 V or above		-	$2 \times t_{Pcyc} + 110$		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

Note 3. N is set as an integer from 1 to 8 by the SSLND register.

2.5 ADC14 Characteristics

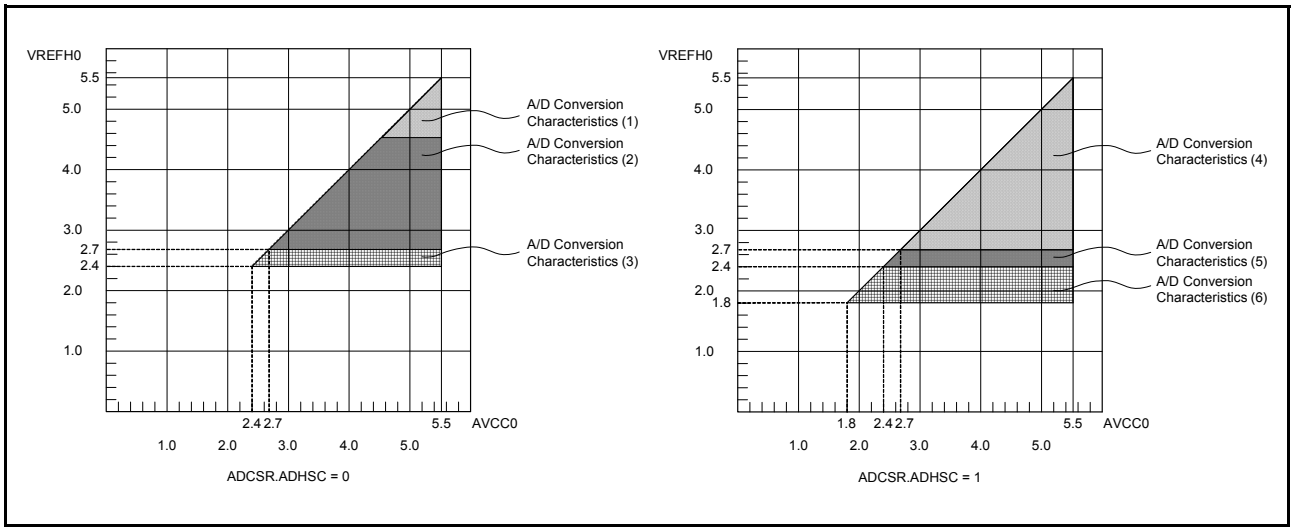


Figure 2.76 AVCC0 to VREFH0 voltage range

Table 2.48 A/D conversion characteristics (1) in high-speed mode (1/2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	64	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 2.49 A/D conversion characteristics (2) in high-speed mode (2/2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Table 2.50 A/D conversion characteristics (3) in high-speed mode (1/2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Item		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	32	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

2.6 DAC12 Characteristics

Table 2.57 D/A conversion characteristics (1)
Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V
Reference voltage = VREFH or VREFL selected

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	AVCC0 – 0.47	V	
DNL differential nonlinearity error	-	±0.5	±1.0	LSB	-
INL integral nonlinearity error	-	±2.0	±8.0	LSB	-
Offset error	-	-	±20	mV	-
Full-scale error	-	-	±20	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

Table 2.58 D/A conversion characteristics (2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = AVCC0 or AVSS0 selected

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	AVCC0 – 0.47	V	-
DNL differential nonlinearity error	-	±0.5	±2.0	LSB	-
INL integral nonlinearity error	-	±2.0	±8.0	LSB	-
Offset error	-	-	±30	mV	-
Full-scale error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

Table 2.59 D/A conversioncharacteristics (3)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V
Reference voltage = internal reference voltage selected

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	Vbgr	V	-
DNL differential nonlinearity error	-	±2.0	±16.0	LSB	-
INL integral nonlinearity error	-	±8.0	±16.0	LSB	-
Offset error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

2.9 POR and LVD Characteristics

Table 2.62 Power-on reset circuit and voltage detection circuit characteristics (1)
Conditions: VCC = AVCC0 = VCC_USB

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.80, Figure 2.81
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.82 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.83 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.84 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit (LVD2), it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol Vdet0_# denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

2.10 Battery Backup Function Characteristics

Table 2.64 Battery Backup Function Characteristics
Conditions: VCC = AVCC0 = 1.6V to 5.5V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0V

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup (falling)		$V_{DETBATT}$	1.99	2.09	2.19	V	Figure 2.85, Figure 2.86
Hysteresis width for switching to battery back up		V_{VBATTH}	-	100	-	mV	
VCC-off period for starting power supply switching		$t_{VOFFBATT}$	300	-	-	µs	-
Voltage detection level VBATT_Power-on reset (VBATT_POR)		$V_{VBATPOR}$	1.30	1.40	1.50	V	Figure 2.85, Figure 2.86
Wait time after VBATT_POR reset time cancellation		$t_{VBATPOR}$	-	-	3	mS	-
Level for detection of voltage drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 10b	$V_{DETBATLVD}$	2.11	2.2	2.29	V	Figure 2.87
	VBTLVDLVL[1:0] = 11b		1.92	2	2.08	V	
Hysteresis width for VBATT pin LVD		$V_{VBATLVDTH}$	-	50	-	mV	
VBATT pin LVD operation stabilization time		t_{d_vbat}	-	-	300	µs	Figure 2.87
VBATT pin LVD response delay time		t_{det_vbat}	-	-	350	µs	
Allowable voltage change rising/falling gradient		dt/dVCC	1.0	-	-	ms/V	-
VCC voltage level for access to the VBATT backup registers		$V_{\_BKBATT}$	1.8	-	-	V	-

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

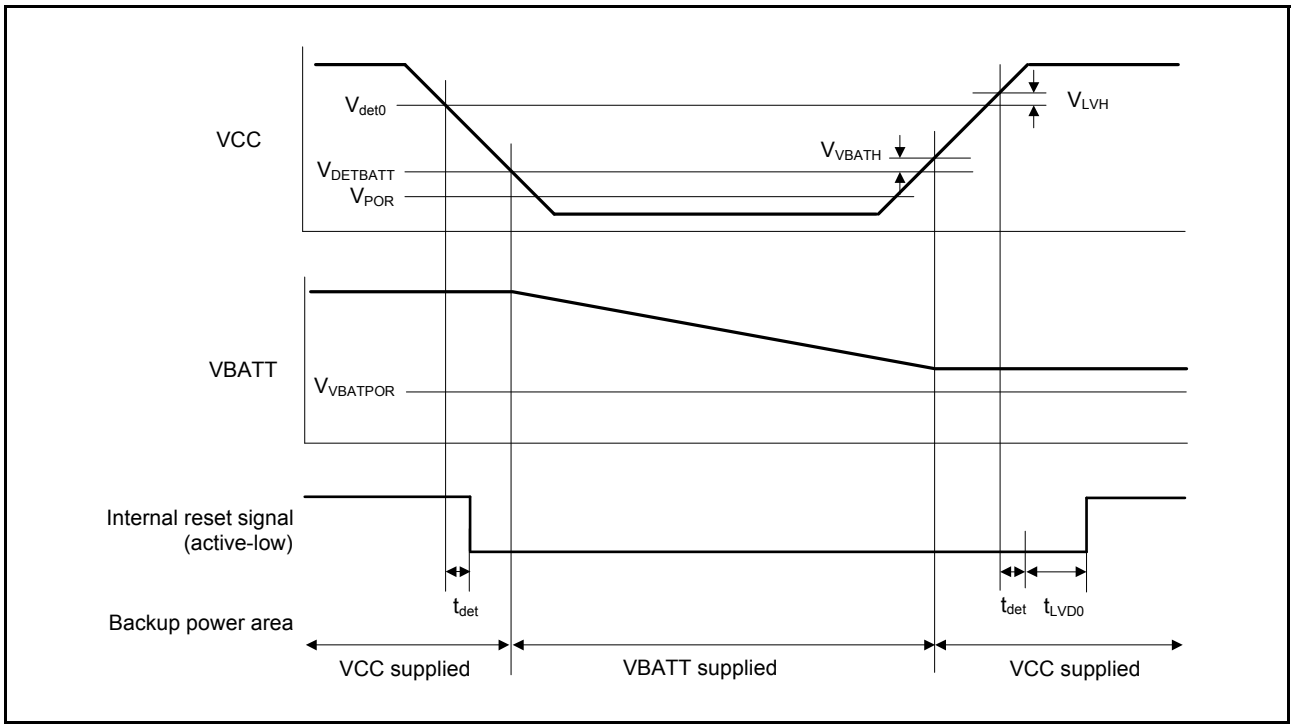
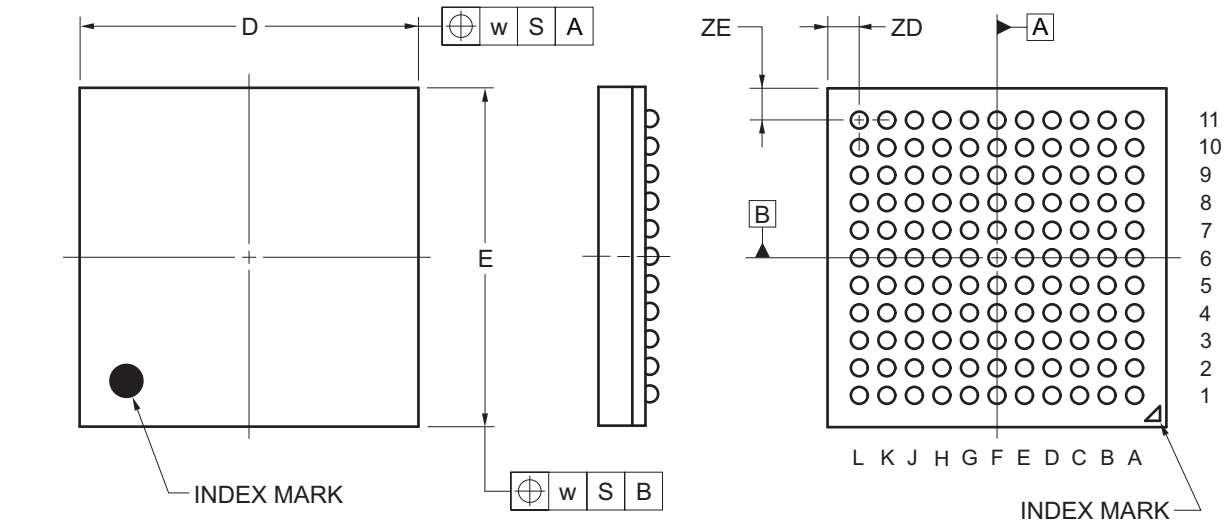
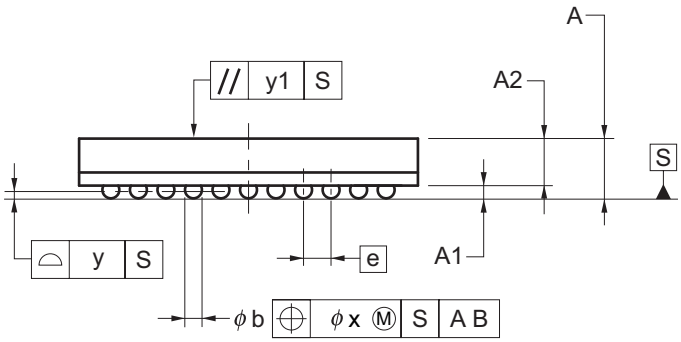


Figure 2.85 Power supply switching and LVD0 reset Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
-	PLBG0121JA-A	P121F1-65-CAH	-





(UNIT: mm)

ITEM	DIMENSIONS
D	8.00±0.10
E	8.00±0.10
w	0.20
A	1.21±0.10
A1	0.30±0.05
A2	0.91
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.75
ZE	0.75

Figure 1.3 BGA 121-pin

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.