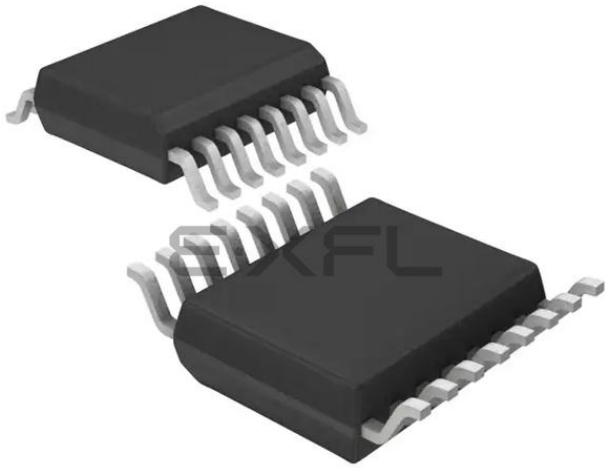

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Details	
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Core Processor	HC08
Core Size	8-Bit
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Number of I/O	-
Program Memory Size	6KB (6K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908ql3mdte

Revision History (Sheet 2 of 2)

Date	Revision Level	Description	Page Number(s)
March, 2004	2.0	Figure 2-2. Control, Status, and Data Registers Corrected reset state for the FLASH Block Protect Register. Corrected reset value for the Internal Oscillator Time Value	33 34
		Table 7-1. Instruction Set Summary — Added WAIT instruction	83
		11.8.1 Oscillator Status and Control Register — Revised description of ECGON bit for clarity	117
		Table 13-3. Interrupt Sources — Corrected address locations for SLIC, KBI, and ADC	140
		14.3.5 SLIC Wait (Core Specific) — Revised description for clarity	144
		14.3.7 SLIC Stop (Core Specific) — Revised description for clarity	144
		14.6.6.2 Byte Transfer Mode Operation — Revised definition of Receiver Buffer Overrun Error	156
		14.7.1 LIN Message Frame Header — Revised third paragraph of description	161
		14.14 Sleep and Wakeup Operation — Revised second paragraph of description	174
		15.8 Input/Output Signals — Corrected reference from PTA0/TCH) to PTB0/TCH0	196
		15.8.2 TIM Channel I/O Pins (PTB0/TCH0 and PTA1/TCH1) — Corrected reference to from PTA0/TCH) to PTB0/TCH0	196
		Figure 16-1. Block Diagram Highlighting BRK and MON Blocks — Added	206
		17.5 5-V DC Electrical Characteristics — Updated table notes	227
		17.8 5-V Oscillator Characteristics — Updated table notes	230
		17.9 3.3-V DC Electrical Characteristics — Updated table notes	231
June, 2004	3.0	Modular sections reworked for clarity.	Throughout
December, 2004	4.0	Updated to final Freescale format. Corrections per email review. Replaced ADC chapter with latest.	Throughout
		Table 1-3. Function Priority in Shared Pins — Updated entry for PTA2	23
		Figure 1-2. MCU Pin Assignments — Corrected pin assignments for the TSSOP packages.	21
		17.11 Oscillator Characteristics — Updated deviation from trimmed internal oscillator specifications.	210
		17.8 3.3-V DC Electrical Characteristics — Corrected capacitance values	208
		17.11 Oscillator Characteristics — Corrected Note 8	211
August, 2005	5.0	13.4.1 External Pin Reset — Corrected location of RSTEN bit from CONFIG1 to CONFIG2.	120
		13.4.2 Active Resets from Internal Sources — Corrected location of RSTEN bit from CONFIG1 to CONFIG2.	120
		Chapter 18 Ordering Information and Mechanical Specifications — Replaced case outlines with appropriate 98A drawing.	219
September, 2005	6.0	Figure 2-1. Memory Map — Corrected address labels.	26

Table of Contents

Chapter 15
Timer Interface Module (TIM)

Chapter 16
Development Support

- Power-on reset
- Memory mapped I/O registers
- Power saving stop and wait modes
- Available packages:
  – 16-pin small outline integrated circuit (SOIC) package
  – 16-pin thin shrink small outline package (TSSOP)

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908QL4.

1.4 Pin Functions

Table 1-2 provides a description of the pin functions.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001C	Keyboard Interrupt Polarity Register (KBIPR) See page 95.	Read:	0	0	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	IRQ Status and Control Register (INTSCR) See page 87.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0
$001E	Configuration Register 2 (CONFIG2)(1) See page 63.	Read:	IRQPUD	IRQEN	R	R	R	R	OSCENIN-STOP	RSTEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0(2)

1. One-time writable register after each reset.
2. RSTEN reset to 0 by a power-on reset (POR) only.

$001F	Configuration Register 1 (CONFIG1)(1) See page 64.	Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVITRIP	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0(2)	0	0	0

1. One-time writable register after each reset.
2. LVITRIP reset to 0 by a power-on reset (POR) only.

$0020	TIM Status and Control Register (TSC) See page 180.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$0021	TIM Counter Register High (TCNTH) See page 182.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	TIM Counter Register Low (TCNTL) See page 182.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	TIM Counter Modulo Register High (TMODH) See page 182.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	TIM Counter Modulo Register Low (TMODL) See page 182.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	TIM Channel 0 Status and Control Register (TSC0) See page 183.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 7)

AWUIE — Auto Wakeup Interrupt Enable Bit

This read/write bit enables the auto wakeup interrupt input to latch interrupt requests. Reset clears AWUIE.

1 = Auto wakeup enabled as interrupt input
0 = Auto wakeup not enabled as interrupt input

NOTE

KBIE5–KBIE0 bits are not used in conjuction with the auto wakeup feature. For a description of these bits, see 9.8.2 Keyboard Interrupt Enable Register (KBIER).

4.6.4 Configuration Register 2

The configuration register 2 (CONFIG2), is used to allow the bus clock source to run in STOP. In this case, the clock, BUSCLKX4 will be used to drive the AWU request generator.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IRQPUD	IRQEN	R	R	R	R	OSCENINSTOP	RSTEN
Reset:	0	0	0	0	0	0	0	0

Figure 4-5. Configuration Register 2 (CONFIG2)

OSCENINSTOP — Oscillator Enable in Stop Mode Bit

OSCENINSTOP, when set, will allow the bus clock source (BUSCLKX4) to generate clocks for the AWU in stop mode. See 11.8.1 Oscillator Status and Control Register for information on enabling the external clock sources.

1 = Oscillator enabled to operate during stop mode
0 = Oscillator disabled during stop mode

NOTE

IRQPUD, IRQEN, and RSTEN bits are not used in conjuction with the auto wakeup feature. For a description of these bits, see Chapter 5 Configuration Register (CONFIG).

4.6.5 Configuration Register 1

The configuration register 1 (CONFIG1), is used to select the period for the AWU. The timeout will be based on the COPRS bit along with the clock source for the AWU.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVITRIP	SSREC	STOP	COPD
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

Figure 4-6. Configuration Register 1 (CONFIG1)

The COP counter is a free-running 6-bit counter preceded by the 12-bit system integration module (SIM) counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after 262,128 or 8176 BUSCLKX4 cycles; depending on the state of the COP rate select bit, COPRS, in configuration register 1. With a 262,128 BUSCLKX4 cycle overflow option, the internal 12.8-MHz oscillator gives a COP timeout period of 20.48 ms. Writing any value to location $FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.

NOTE

Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the $\overline{\text{RST}}$ pin low (if the RSTEN bit is set in the CONFIG1 register) for 32 × BUSCLKX4 cycles and sets the COP bit in the reset status register (RSR). See 13.8.1 SIM Reset Status Register.

NOTE

Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

6.3 I/O Signals

The following paragraphs describe the signals shown in Figure 6-1.

6.3.1 BUSCLKX4

BUSCLKX4 is the oscillator output signal. BUSCLKX4 frequency is equal to the crystal frequency or the RC-oscillator frequency.

6.3.2 STOP Instruction

The STOP instruction clears the SIM counter.

6.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) (see Figure 6-2) clears the COP counter and clears stages 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector.

6.3.4 Power-On Reset

The power-on reset (POR) circuit in the SIM clears the SIM counter 4096 × BUSCLKX4 cycles after power up.

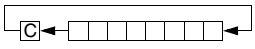
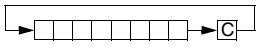
6.3.5 Internal Reset

An internal reset clears the SIM counter and the COP counter.

6.3.6 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register (CONFIG). See Chapter 5 Configuration Register (CONFIG).

Table 7-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

8.8 Registers

The IRQ status and control register (INTSCR) controls and monitors operation of the IRQ module. The INTSCR:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks the IRQ interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ}}$ interrupt pin

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF	0	IMASK	MODE
Write:						ACK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-3. IRQ Status and Control Register (INTSCR)

IRQF — IRQ Flag Bit

This read-only status bit is set when the IRQ interrupt is pending.

1 = $\overline{\text{IRQ}}$ interrupt pending
0 = $\overline{\text{IRQ}}$ interrupt not pending

ACK — IRQ Interrupt Request Acknowledge Bit

Writing a 1 to this write-only bit clears the IRQ latch. ACK always reads 0.

IMASK — IRQ Interrupt Mask Bit

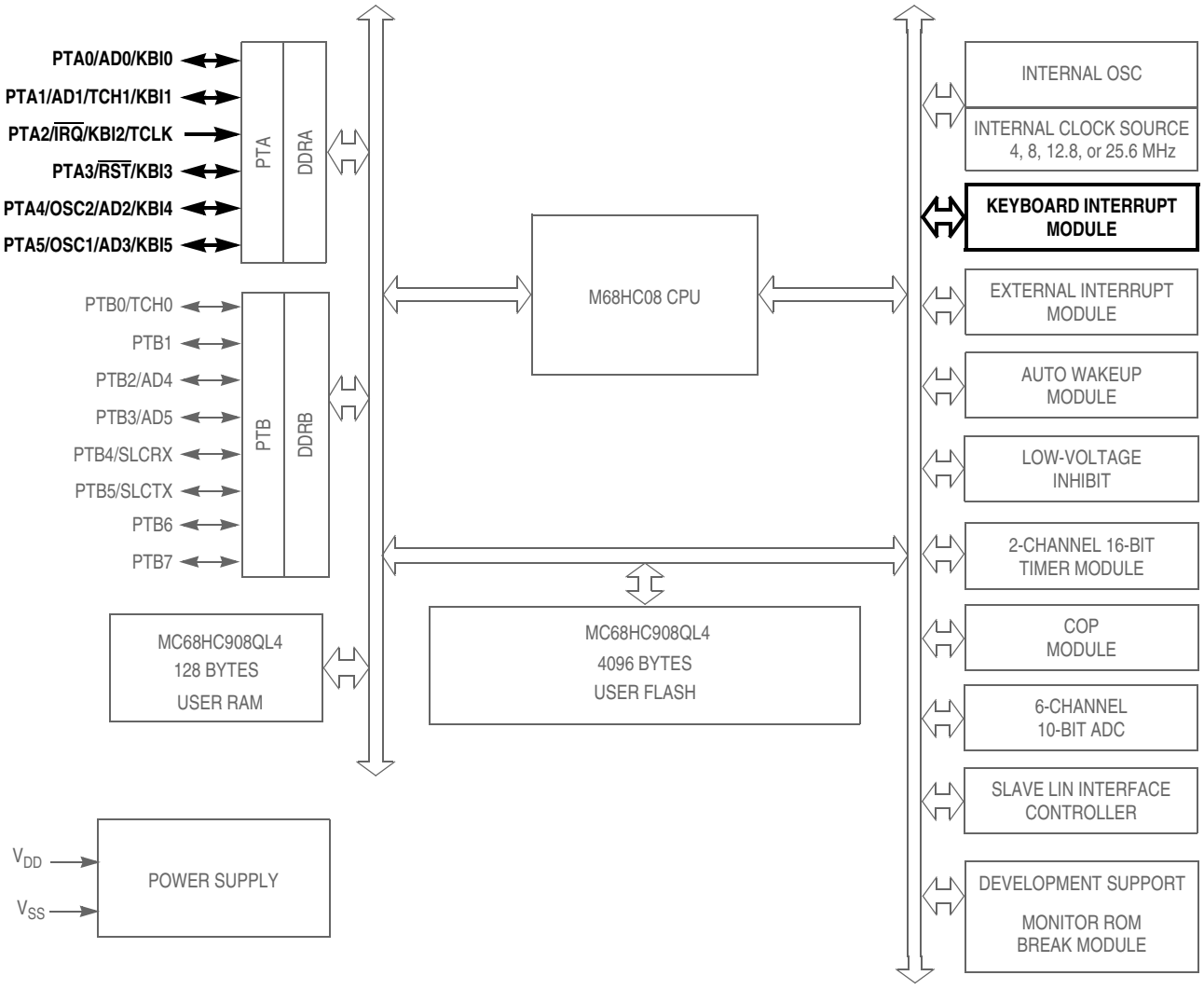
Writing a 1 to this read/write bit disables the IRQ interrupt request.

1 = IRQ interrupt request disabled
0 = IRQ interrupt request enabled

MODE — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

1 = $\overline{\text{IRQ}}$ interrupt request on falling edges and low levels
0 = $\overline{\text{IRQ}}$ interrupt request on falling edges only



RST, IRQ: Pins have internal pull up device
All port pins have programmable pull up device (pullup/down on port A)
PTA[0:5]: Higher current sink and source capability

Figure 9-1. Block Diagram Highlighting KBI Block and Pins

11.6 OSC During Break Interrupts

There are no status flags associated with the OSC module.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See BFCR in the SIM section of this data sheet.

To allow software to clear status bits during a break interrupt, write a 1 to BCFE. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to BCFE. With BCFE cleared (its default state), software can read and write registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is cleared. After the break, doing the second step clears the status bit.

11.7 I/O Signals

The OSC shares its pins with general-purpose input/output (I/O) port pins. See Figure 11-1 for port location of these shared pins.

11.7.1 Oscillator Input Pin (OSC1)

The OSC1 pin is an input to the crystal oscillator amplifier, an input to the RC oscillator circuit, or an input from an external clock source.

When the OSC is configured for internal oscillator, the OSC1 pin can be used as a general-purpose input/output (I/O) port pin or other alternative pin function.

11.7.2 Oscillator Output Pin (OSC2)

For the XTAL oscillator option**,** the OSC2 pin is the output of the crystal oscillator amplifier.

When the OSC is configured for internal oscillator, external clock, or RC, the OSC2 pin can be used as a general-purpose I/O port pin or other alternative pin function. When the oscillator is configured for internal or RC, the OSC2 pin can be used to output BUSCLKX4.

Table 11-1. OSC2 Pin Function

Option	OSC2 Pin Function
XTAL oscillator	Inverting OSC1
External clock	General-purpose I/O or alternative pin function
Internal oscillator or RC oscillator	Controlled by OSC2EN bit OSC2EN = 0: General-purpose I/O or alternative pin function OSC2EN = 1: BUSCLKX4 output

12.2.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the six port A pins.

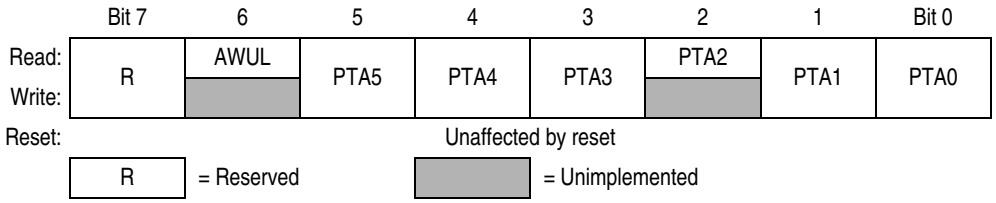


Figure 12-1. Port A Data Register (PTA)

PTA[5:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

AWUL — Auto Wakeup Latch Data Bit

This is a read-only bit which has the value of the auto wakeup interrupt request latch. The wakeup request signal is generated internally (see Chapter 4 Auto Wakeup Module (AWU)). There is no PTA6 port nor any of the associated bits such as PTA6 data register, pullup/down enable or direction.

12.2.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a 0 disables the output buffer.

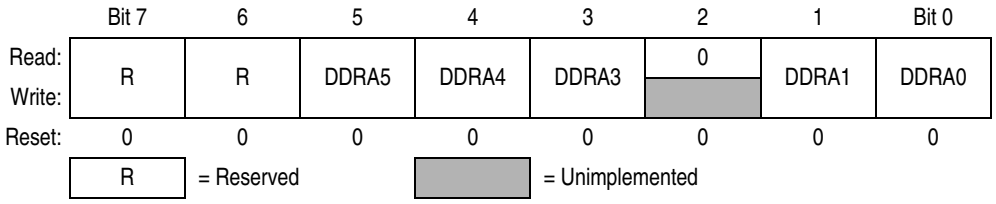


Figure 12-2. Data Direction Register A (DDRA)

DDRA[5:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[5:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

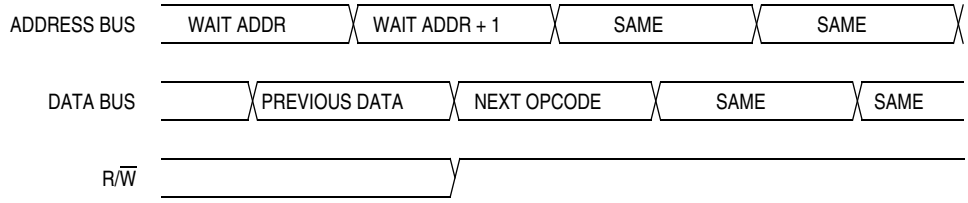
NOTE

Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.

Figure 12-3 shows the port A I/O logic.

13.7.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. Figure 13-14 shows the timing for wait mode entry.



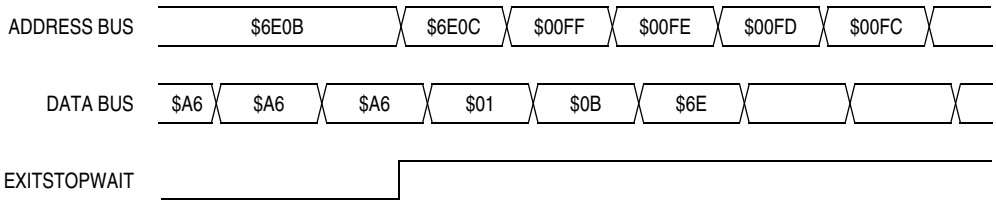
NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 13-14. Wait Mode Entry Timing

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

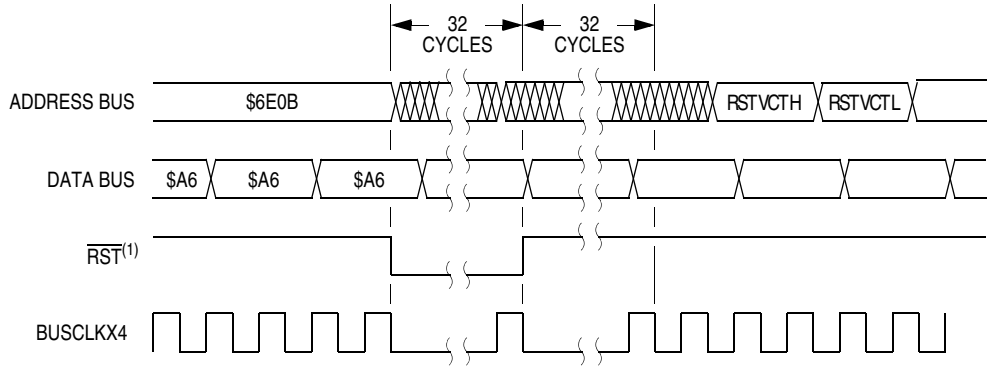
Wait mode can also be exited by a reset (or break in emulation mode). A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the configuration register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.

Figure 13-15 and Figure 13-16 show the timing for wait recovery.



NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt

Figure 13-15. Wait Recovery from Interrupt



1. $\overline{\text{RST}}$ is only available if the RSTEN bit in the CONFIG1 register is set.

Figure 13-16. Wait Recovery from Internal Reset

either transmit or receive these bytes, depending upon the user code interpretation of the identifier byte. Data is always transmitted into the data field least significant byte (LSB) first.

The SLIC module can automatically handle up to 64 bytes in extended LIN message frames without significantly changing program execution.

14.9.3 LIN Checksum Field

The checksum field is a data integrity measure for LIN message frames, used to signal errors in data consistency. The LIN 1.3 checksum calculation only covers the data field, but the SLIC module also supports an enhanced checksum calculation which also includes the identifier field. For more information on the checksum calculation, refer to 14.9.13 LIN Data Integrity Checking Methods.

14.9.4 SLIC Module Constraints

In designing a practical module, certain reasonable constraints must be placed on the LIN message traffic which are not necessarily explicitly specified in the LIN specification. The SLIC module presumes that:

- Timeout for no-bus-activity = 1 second.

14.9.5 SLCSV Interrupt Handling

Each change of state of the SLIC module is encoded in the SLIC state vector register (SLCSV). This is an efficient method of handling state changes, indicating to the user not only the current status of the SLIC module, but each state change will also generate an interrupt (if SLIC interrupts are enabled). For more detailed information on the SLCSV, please refer to 14.8.6 SLIC State Vector Register.

In the software diagrams in the following subsections, when an interrupt is shown, the first step must always be reading SLCSV to determine what is the current status of the SLIC module. Likewise, when the diagrams indicate to “EXIT ISR”, the final step to exiting the interrupt service routine is to clear the SLCF interrupt flag. This can only be done if the SLCSV has first been read, and in the case that data has been received (such as an ID byte or command message data) the SLCD has been read at least one time.

After SLCSV is read, it will switch to the next pending state, so the user must be sure it is copied only once into a software variable at the beginning of the interrupt service routine to avoid inadvertently clearing a pending interrupt source. Additional decisions based on this value must be made from the software variable, rather than from the SLCSV itself.

After exiting the ISR, normal application code may resume. If the diagram indicates to “RETURN TO IDLE,” it indicates that all processing for the current message frame has been completed. If an error was detected and the corresponding error code loaded into the SLCSV, any pending data in the data buffer will be flushed out and the SLIC returned to its idle state, seeking out the next message frame header.

14.9.6 SLIC Module Initialization Procedure

14.9.6.1 LIN Mode Initialization

The SLIC module does not require very much initialization, due to its self-synchronizing design. Because no prior knowledge of the bit rate is required to synchronize to the LIN bus, no programming of bit rate is required.

At initialization time, the user must configure:

- SLIC prescale register (SLIC digital receive filter adjustment).
- Wait clock mode operation.

The SLIC clock is the same as the CPU bus clock. The module is designed to provide better than 1% bit rate accuracy at the lowest value of the SLIC clock frequency and the accuracy improves as the SLIC clock frequency is increased. For this reason, it is advantageous to choose the fastest SLIC clock which is still within the acceptable operating range of the SLIC. Because the SLIC may be used with MCUs with internal oscillators, the tolerance of the oscillator must be taken into account to ensure that SLIC clock frequency does not exceed the bounds of the SLIC clock operating range. This is especially important if the user wishes to use the oscillator untrimmed, where process variations might result in MCU frequency offsets of ±25%.

The acceptable range of SLIC clock frequencies is 2–8 MHz to guarantee LIN operations with greater than 1.5% accuracy across the 1–20 kbps range of LIN bit rates. The user must ensure that the fastest possible SLIC clock frequency never exceeds 8 MHz or that the slowest possible SLIC clock never falls below 2 MHz under worst case conditions. This would include, for example, oscillator frequency variations due to untrimmed oscillator tolerance, temperature variation, or supply voltage variation.

To initialize the SLIC module into LIN operating mode, the user must perform the following steps prior to needing to receive any LIN message traffic. These steps assume the MCU has been reset either by a power-on reset (POR) or any other MCU reset mechanism.

The steps for SLIC Initialization for LIN operation are:

1. Write SLCC1 to clear INITREQ.
2. When INITACK = 0, write SLCC1 & SLCC2 with desired values for:
   a. SLCWCM — Wait clock mode (default = leaving SLIC clock running when in CPU wait).
3. Write SLCP to set up prescalers for:
   a. RXFP — Digital receive filter clock prescaler (default = SLIC divided by 3).
4. Enable the SLIC module by writing SLCC2:
   a. SLCE = 1 to place SLIC module into run mode.
   b. BTM = 0 to disable byte transfer mode (default).
5. Write SLCC1 to enable SLIC interrupts (if desired).

14.9.6.2 Byte Transfer Mode Initialization

Bit rate synchronization is handled automatically in LIN mode, using the synchronization data contained in each LIN message to derive the desired bit rate. In byte transfer mode (BTM = 1); however, the user must set up the bit rate for communications using the clock selection, prescaler, and SLCBT.

More information on byte transfer mode is described in 14.9.15 Byte Transfer Mode Operation, including the performance parameters on recommended maximum speeds, bit time resolution, and oscillator tolerance requirements.

After the desired settings of prescalers and bit time are determined, the SLIC Initialization for BTM operation is virtually identical to that of LIN operation.

The steps are:

1. Write SLCC1 to clear INITREQ.
2. When INITACK = 0, write SLCC2 with desired values for:
   a. SLCWCM — Wait clock mode (default = leaving SLIC clock running when in CPU wait).
3. Write SLCICP to set up prescalers for:
   a. RXFP — Digital receive filter clock prescaler (default = SLIC divided by 3).

NOTE

If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 15-5. TIM Counter High Register (TCNTH)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-6. TIM Counter Low Register (TCNTL)

15.8.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the counter. When the counter reaches the modulo value, the overflow flag (TOF) becomes set, and the counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Reset:	1	1	1	1	1	1	1	1

Figure 15-7. TIM Counter Modulo High Register (TMODH)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset:	1	1	1	1	1	1	1	1

Figure 15-8. TIM Counter Modulo Low Register (TMODL)

NOTE

Reset the counter before writing to the TIM counter modulo registers.

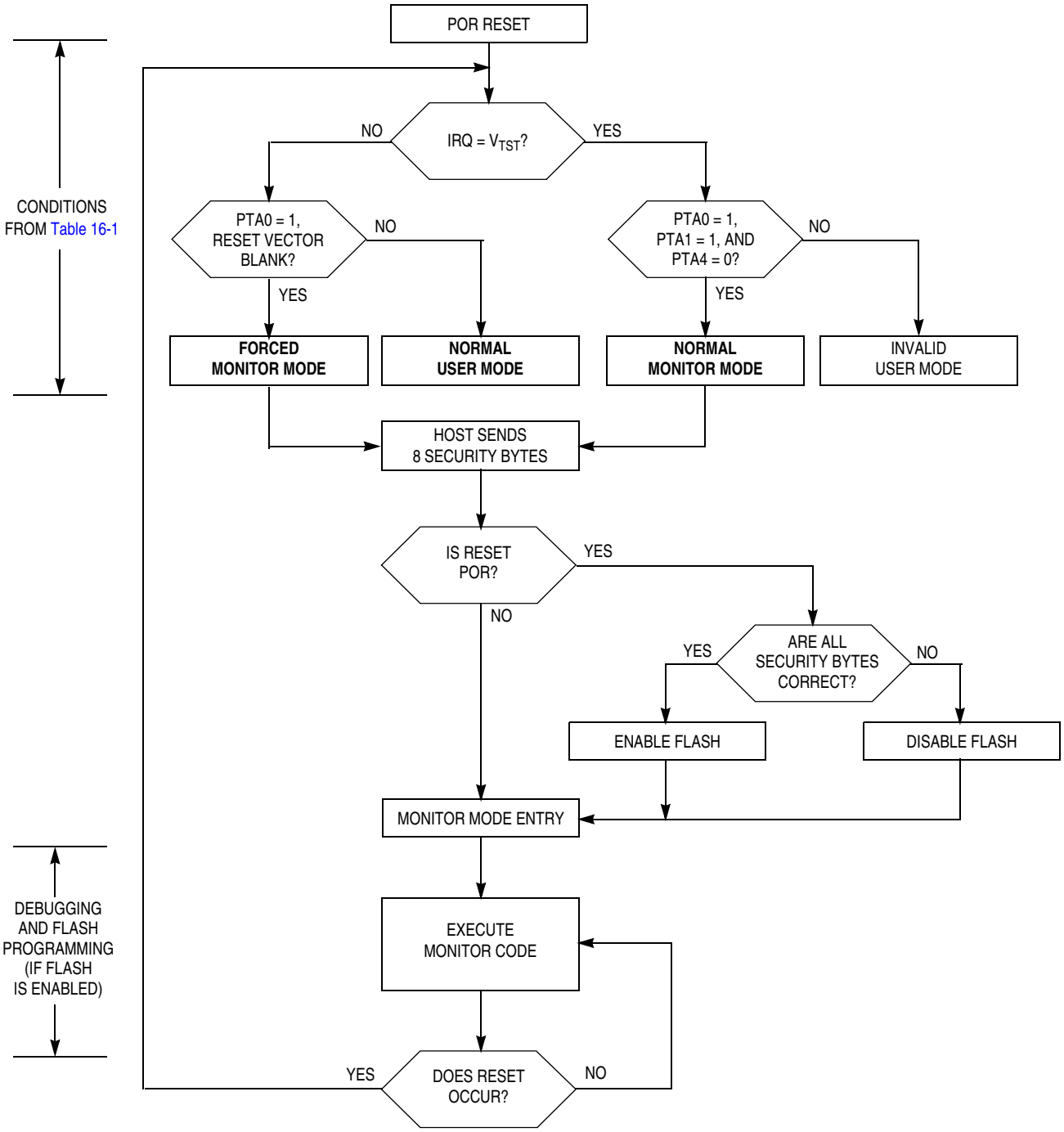


Figure 16-9. Simplified Monitor Mode Entry Flowchart

Characteristic	Conditions	Symbol	Min	Typ(1)	Max	Unit	Comment
Integral non-linearity	10-bit mode	INL	0	±0.5	—	LSB	
	8-bit mode		0	±0.3	—		
Zero-scale error	10-bit mode	E_{ZS}	0	±0.5	—	LSB	$V_{ADIN} = V_{SS}$
	8-bit mode		0	±0.3	—		
Full-scale error	10-bit mode	E_{FS}	0	±0.5	—	LSB	$V_{ADIN} = V_{DD}$
	8-bit mode		0	±0.3	—		
Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB	8-bit mode is not truncated
	8-bit mode		—	—	±0.5		
Input leakage error	10-bit mode	E_{IL}	0	±0.2	±5	LSB	Pad leakage(5) * R_{AS}
	8-bit mode		0	±0.1	±1.2		
Bandgap voltage input(6)		V_{BG}	1.17	1.245	1.32	V	

1. Typical values assume V_{DD} = 5.0 V, temperature = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Incremental I_{DD} added to MCU mode current.
3. Values are based on characterization results, not tested in production.
4. Reference the ADC module specification for more information on calculating conversion times.
5. Based on typical input pad leakage current.
6. LVI must be enabled, (LVIPWRD = 0, in CONFIG1). Voltage input to ADCH4:0 = $1A, an ADC conversion on this channel allows user to determine supply voltage.

Chapter 18
Ordering Information and Mechanical Specifications

18.1 Introduction

This section provides ordering information for the MC68HC908QL4, MC68HC908QL3, and MC68HC908QL2 along with the dimensions for:

- 16-pin small outline integrated circuit (SOIC) package
- 16-pin thin shrink small outline package (TSSOP)

18.2 MC Order Numbers

Table 18-1. MC Order Numbers

MC Order Number	**ADC**	**FLASH** Memory	**Package**
MC908QL4	Yes	4096 bytes	16-pins SOIC, and TSSOP
MC908QL3	No	4096 bytes	
MC908QL2	Yes	2048 bytes	

Temperature and package designators:
C = −40°C to +85°C
V = −40°C to +105°C
M = −40°C to +125°C
DW = Small outline integrated circuit package (SOIC)
DT = Thin shrink small outline package (TSSOP)

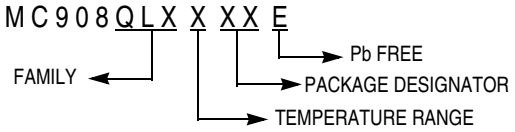


Figure 18-1. Device Numbering System

18.3 Package Dimensions

Refer to the following pages for detailed package dimensions.

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For information on Freescale.s Environmental Products program, go to http://www.freescale.com/epp.

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