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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77i058a25dl

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6. FUNCTIONAL DESCRIPTION

The W77IE58 is 8052 pin compatible and instruction set compatible. It includes the resources of the standard 8052 such as four 8-bit I/O Ports, three 16-bit timer/counters, full duplex serial port and interrupt sources.

The W77IE58 features a faster running and better performance 8-bit CPU with a redesigned core processor without wasted clock and memory cycles. it improves the performance not just by running at high frequency but also by reducing the machine cycle duration from the standard 8052 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. The W77IE58 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers. It can also adjust the duration of the MOVX instruction (access to off-chip data memory) between two machine cycles and nine machine cycles. This flexibility allows the W77IE58 to work efficiently with both fast and slow RAMs and peripheral devices. In addition, the W77IE58 contains on-chip 1KB MOVX SRAM, the address of which is between 0000H and 03FFH. It only can be accessed by MOVX instruction; this on-chip SRAM is optional under software control.

The W77IE58 is an 8052 compatible device that gives the user the features of the original 8052 device, but with improved speed and power consumption characteristics. It has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). While the original 8051 family was designed to operate at 12 clock periods per machine cycle, the W77IE58 operates at a much reduced clock rate of only 4 clock periods per machine cycle. This naturally speeds up the execution of instructions. Consequently, the W77IE58 can run at a higher speed as compared to the original 8052, even if the same crystal is used. Since the W77IE58 is a fully static CMOS design, it can also be operated at a lower crystal clock, giving the same throughput in terms of instruction execution, yet reducing the power consumption.

The 4 clocks per machine cycle feature in the W77IE58 is responsible for a three-fold increase in execution speed. The W77IE58 has all the standard features of the 8052, and has a few extra peripherals and features as well.

I/O Ports

The W77IE58 has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 and 3 act as I/O ports with alternate functions. Port 4 is only available on 44-pin PLCC/QFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. The P4.0 has an alternate function WAIT which is the wait state control signal. When wait state control signal is enabled, P4.0 is input only.

Serial I/O

The W77IE58 has two enhanced serial ports that are functionally similar to the serial port of the original 8052 family. However the serial ports on the W77IE58 can operate in different modes in order to obtain timing similarity as well. Note that the serial port 0 can use Timer 1 or 2 as baud rate generator, but the serial port 1 can only use Timer 1 as baud rate generator. The serial ports have the enhanced features of Automatic Address recognition and Frame Error detection.



Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0	
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	
Mnemonic: TH1 Address: 8Dh									
TH1.7-0: Timer 1 MSB									
Clock Control									
Bit:	7	6	5	4	3	2	1	0	
	WD1	WD0	T2M	T1M	TOM	MD2	MD1	MD0	
Mnemon	ic: CKCO	N			ŀ	Address: 8	3Eh		
WD1-0: Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.									
WD1 WD0 Interrupt time-out Reset time-out									
	0	0	2 ¹⁷		2 ¹⁷ + 512	2			

	1100	interrupt anno out	
0	0	2 ¹⁷	2 ¹⁷ + 512
0	1	2 ²⁰	2 ²⁰ + 512
1	0	2 ²³	2 ²³ + 512
1	1	2 ²⁶	2 ²⁶ + 512

- T2M: Timer 2 clock select: When T2M is set to 1, timer 2 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.
- Timer 1 clock select: When T1M is set to 1, timer 1 uses a divide by 4 clock, and when set to T1M: 0 it uses a divide by 12 clock.
- Timer 0 clock select: When T0M is set to 1, timer 0 uses a divide by 4 clock, and when set to TOM: 0 it uses a divide by 12 clock.
- MD2-0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The \overline{RD} or \overline{WR} strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

MD2	MD1	MD0	Stretch value	MOVX duration
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles (Default)
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles



WS: Wait State Signal Enable. Setting this bit enables the \overline{WAIT} signal on P4.0. The device will sample the wait state control signal \overline{WAIT} via P4.0 during MOVX instruction. This bit is time access protected.

Power Management Register

Bit:	7	6	5	4	3	2	1	0
	CD1	CD0	SWB	-	XTOFF	ALE-OFF	-	DME0
Mr	nemonic: P	MR				Address	C4h	

CD1,CD0: Clock Divide Control. These bit selects the number of clocks required to generate one machine cycle. There are three modes including divide by 4, 64 or 1024. Switching between modes must first go back devide by 4 mode. For instance, to go from 64 to 1024 clocks/machine cycle the device must first go from 64 to 4 clocks/machine cycle, and then from 4 to 1024 clocks/machine cycle.

CD1,	CD0	clocks/machine cycle
0	0	Reserved
0	1	4
1	0	64
1	1	1024

- SWB: Switchback Enable. Setting this bit allows an enabled external interrupt or serial port activity to force the CD1,CD0 to divide by 4 state (0,1). The device will switch modes at the start of the jump to interrupt service routine while a external interrupt is enabled and actually recongnized by microcontroller. While a serial port reception, the switchback occurs at the start of the instruction following the falling edge of the start bit.
- XTOFF: Crystal Oscillator Disable. Setting this bit disables the external crystal oscillator. This bit can only be set to 1 while the microcontroller is operating from the RC oscillator. Clearing this bit restarts the crystal oscillator, the XTUP (STATUS.4) bit will be set after crystal oscillator warmed-up has completed.
- ALE0FF: This bit disables the expression of the ALE signal on the device pin during all on-board program and data memory accesses. External memory accesses will automatically enable ALE independent of ALEOFF.

0 = ALE expression is enable; 1 = ALE expression is disable

DME0: This bit determines the on-chip MOVX SRAM to be enabled or disabled. Set this bit to 1 will enable the on-chip 1KB MOVX SRAM.



Timer2 MSB

-	-									
	Bit:	7	6	5	4	3	2	1	0	
		TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	
	Mnemonic: TH2 Address: CDh									
TH2:	Timer 2 MSB									
Program Status Word										
	Bit:	7	6	5	4	3	2	1	0	
		CY	AC	F0	RS1	RS0	OV	F1	Р	
	Mnemoni	c: PSW				ŀ	Address: [D0h		
CY:	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.									
AC:	Auxiliary carry: S	et when th	e previou	s operatio	on resulted	d in a carr	y from the	high ord	ər nibble.	
F0:	User flag 0: General purpose flag that can be set or cleared by the user.									
PS 1-0). Register hank se	lact hite								

RS.1-0: Register bank select bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

- OV: Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
- User Flag 1: General purpose flag that can be set or cleared by the user by software. F1:
- P: Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	SMOD_1	POR	-	-	WDIF	WTRF	EWT	RWT
Mnem	onic: WDCO	N		Address: [08h			

SMOD 1: This bit doubles the Serial Port 1 baud rate in mode 1, 2, and 3 when set to 1.

- POR: Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
- WDIF: Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.



- WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.
- EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.
- RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC

Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

Extended Interrupt Enable



EIE.7-5: Reserved bits, will read high.

EWDI: Enable Watchdog timer interrupt.

EX5: External Interrupt 5 Enable.

- EX4: External Interrupt 4 Enable.
- EX3: External Interrupt 3 Enable.
- EX2: External Interrupt 2 Enable.



INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	Х	Х	Х	CLR C	0		
ADDC	Х	Х	Х	CPL C	Х		
SUBB	Х	Х	Х	ANL C, bit	Х		
MUL	0	Х		ANL C, bit	Х		
DIV	0	Х		ORL C, bit	Х		
DA A	Х			ORL C, bit	Х		
RRC A	Х			MOV C, bit	Х		
RLC A	Х			CJNE	Х		
SETB C	1						

Table 2. Instructions that affect Flag settings

A "X" indicates that the modification is as per the result of instruction.

Table 3. Instruction Timing for W77IE58

INSTRUCTION	HEX OP-CODE	BYTES	W77IE58 MACHINE CYCLES	W77IE58 CLOCK CYCLES	8032 CLOCK CYCLES	W77IE58 VS. 8032 SPEED RATIO
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	ЗA	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3



Table 3. Instruction Timing for W77IE58, continued

INSTRUCTION	HEX OP-CODE	BYTES	W77IE58 MACHINE CYCLES	W77IE58 CLOCK CYCLES	8032 CLOCK CYCLES	W77IE58 VS. 8032 SPEED RATIO
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
CPL C	В3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
DEC DPTR	A5	1	2	8	-	-
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3



INSTRUCTION	HEX OP-CODE	BYTES	W77IE58 MACHINE CYCLES	W77IE58 CLOCK CYCLES	8032 CLOCK CYCLES	W77IE58 VS. 8032 SPEED RATIO
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2

Table 3. Instruction Timing for W77IE58, continued



7.2 Instructiion Timing

The instruction timing for the W77IE58 is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W77IE58 and the standard 8032. In the W77IE58 each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W77IE58 does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all opcodes in the W77IE58 are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8032, the MOVX instruction is always two machine cycles long. However in the W77IE58, the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The RD and WR strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three. four or five machine cycle instructions. Note that in the W77IE58, based on the number of machine cycles, there are five different types, while in the standard 8032 there are only three. However, in the W77IE58 each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8032. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8032 in terms of clock periods.



Figure 3. Single Cycle Instruction Timing



Table 4	. Data	Memory	Cycle	Stretch	Values
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M2	M1	МО	MACHINE CYCLES	RD OR WR STROBE WIDTH IN CLOCKS	RD OR WR STROBE WIDTH @ 25 MHZ
0	0	0	2	2	80 nS
0	0	1	3(default)	4	160 nS
0	1	0	4	8	320 nS
0	1	1	5	12	480 nS
1	0	0	6	16	640 nS
1	0	1	7	20	800 nS
1	1	0	8	24	960 nS
1	1	1	9	28	1120 nS



Figure 8. Data Memory Write with Stretch Value = 0



SOURCE	FLAG	PRIORITY LEVEL
External Interrupt 2	IE2	8
External Interrupt 3	IE3	9
External Interrupt 4	IE4	10
External Interrupt 5	IE5	11
Watchdog Timer	WDIF	12 (lowest)

Table 7. Priority structure of interrupts, continued

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are

- 1. An interrupt of equal or higher priority is not currently being serviced.
- 2. The current polling cycle is the last machine cycle of the instruction currently being executed.
- 3. The current instruction does not involve a write to IP, IE, EIP or EIE registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These vector address for the different sources are as follows

Source	Vector Address	Source	Vector Address
Timer 0 Overflow	000Bh	External Interrupt 0	0003h
Timer 1 Overflow	001Bh	External Interrupt 1	0013h
Timer 2 Interrupt	002Bh	Serial Port	0023h
External Interrupt 2	0043h	Serial Port 1	003Bh
External Interrupt 4	0053h	External Interrupt 3	004Bh
Watchdog Timer	0063h	External Interrupt 5	005Bh

 Table 8. Vector locations for interrupt sources

The vector table is not evenly spaced; this is to accommodate future expansions to the device family.



Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W77IE58 is performing a write to IE, IP, EIE or EIP and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP, EIE or EIP access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

8. PROGRAMMABLE TIMERS/COUNTERS

The W77IE58 has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

Timer/Counters 0 & 1

The W77IE58 has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.



When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the " C/\overline{T} " bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

8.1.1 Time-Base Selection

The W77IE58 gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W77IE58 and the standard 8051 can be matched. This is the default mode of operation of the W77IE58 timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

MODE 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx} = 1$. When C/\overline{T} is set to 0, then it will count clock cycles, and if C/\overline{T} is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.





Figure 16. 16-Bit Auto-reload Up/Down Counter

8.1.6 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request. T2OE bit must be cleared in this mode.



Figure 17. Baud Rate Generator Mode



Figure 19. Watchdog Timer

The Watchdog timer should first be restarted by using RWT. This ensures that the timer starts from a known state. The RWT bit is used to restart the watchdog timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The watchdog timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (CKCON.7 and CKCON.6). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the watchdog timer waits for an additional 512 clock cycles. If the Watchdog Reset EWT (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no RWT, a system reset due to Watchdog timer will occur. This will last for two machine cycles, and the Watchdog timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the watchdog timer which will allow the code to run without any watchdog timer interrupts. Now the watchdog timer reset is enabled and the watchdog interrupt may be disabled. If any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

The watchdog time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occur 512 clocks after the time-out has occurred.



Example 1: Valid access						
-	MOV	TA, #0AAh	3 M/C			
	MOV	TA, #055h	3 M/C			
	MOV	WDCON, #00h	3 M/C			
Exampl	e 2: Vali	d access				
	MOV	TA, #0AAh	3 M/C			
	MOV	TA, #055h	3 M/C			
	NOP		1 M/C			
	SETB	EWT	2 M/C			
Exampl	e 3: Vali	d access				
	MOV	TA,#0AAh	3M/C			
	MOV	TA,#055h	3M/C			
	ORL	WDCON, #0000	00010B 3M/C			
Exampl	e 4: Inva	alid access				
	MOV	TA, #0AAh	3 M/C			
	MOV	TA, #055h	3 M/C			
	NOP		1 M/C			
	NOP		1 M/C			
	CLR	POR	2 M/C			
Example 5: Invalid Access						
	MOV	TA, #0AAh	3 M/C			
	NOP		1 M/C			
	NOP MOV	TA, #055h	1 M/C 3 M/C			

In the first two examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 3, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 4, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window in not opened at all, and the write to the protected bit fails.

Note: M/C = Machine Cycles



10. ON-CHIP FLASH EPROM CHARACTERISTICS

The W77IE58 has several modes to program the on-chip ROM. All these operations are configured by the pins RST, ALE, $\overrightarrow{\text{PSEN}}$, A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3), $\overrightarrow{\text{CE}}$ (P3.6), $\overrightarrow{\text{OE}}$ (P3.7), A0(P1.0) and VPP($\overrightarrow{\text{EA}}$). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

Output Disable Condition

When the \overline{OE} is set to high, no data output appears on the D7...D0.

Program Operation

This operation is used to program the data to on-chip ROM and the security bits. Program operation is done when the VPP is reach to VCP (12.5V) level, \overline{CE} set to low, and \overline{OE} set to high.

Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the on-chip ROM cells and the security bits from 0 to 1. This erase operation is done when the VPP is reach to VEP level, \overline{CE} set to low, and \overline{OE} set to high.

Erase Verify Operation

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if VPP = VEP(14.5V), \overline{CE} is high and \overline{OE} is low.

Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When $P3.6(\overline{CE}) = VIH$, $P3.7(\overline{OE}) = VIH$, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.



MOVX Characteristics Using Stretch Memory Cycles, continued

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRETCH
RD Low to Valid Data In	t _{RLDV}		2.0 t _{CLCL} - 20 t _{MCS} - 20	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Hold after Read	t _{RHDX}	0		nS	
Data Float after Read	t _{RHDZ}		t _{CLCL} - 5 2.0 t _{CLCL} - 5	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
ALE Low to Valid Data In	t _{LLDV}		2.5 t _{CLCL} - 5 t _{MCS} + 2 t _{CLCL} - 40	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 0 Address to Valid Data In	t _{AVDV1}		3.0 t _{CLCL} - 20 2.0 t _{CLCL} - 5	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
ALE Low to RD or WR Low	t _{LLWL}	0.5 t _{CLCL} - 5 1.5 t _{CLCL} - 5	0.5 t _{CLCL} + 5 1.5 t _{CLCL} + 5	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 0 Address to \overline{RD} or \overline{WR} Low	t _{AVWL}	t _{CLCL} - 5 2.0 t _{CLCL} - 5		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 2 Address to \overline{RD} or \overline{WR} Low	t _{AVWL2}	1.5 t _{CLCL} - 5 2.5 t _{CLCL} - 5		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Valid to WR Transition	t _{QVWX}	-5 1.0 t _{CLCL} - 5		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Hold after Write	t _{WHQX}	t _{CLCL} - 5 2.0 t _{CLCL} - 5		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
RD Low to Address Float	t _{RLAZ}		0.5 t _{CLCL} - 5	nS	
RD or WR high to ALE high	t _{WHLH}	0 1.0 t _{CLCL} - 5	10 1.0 t _{CLCL} + 5	nS	$t_{MCS} = \overline{0}$ $t_{MCS} > 0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

M2	M1	MO	MOVX CYCLES	T _{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t _{CLCL}
0	1	0	4 machine cycles	8 t _{CLCL}
0	1	1	5 machine cycles	12 t _{CLCL}
1	0	0	6 machine cycles	16 t _{CLCL}
1	0	1	7 machine cycles	20 t _{CLCL}
1	1	0	8 machine cycles	24 t _{CLCL}
1	1	1	9 machine cycles	28 t _{CLCL}



Timing Waveforms, continued

Data Memory Write Cycle





15. PACKAGE DIMENSIONS

15.1 40-pin DIP



15.2 44-pin PLCC

