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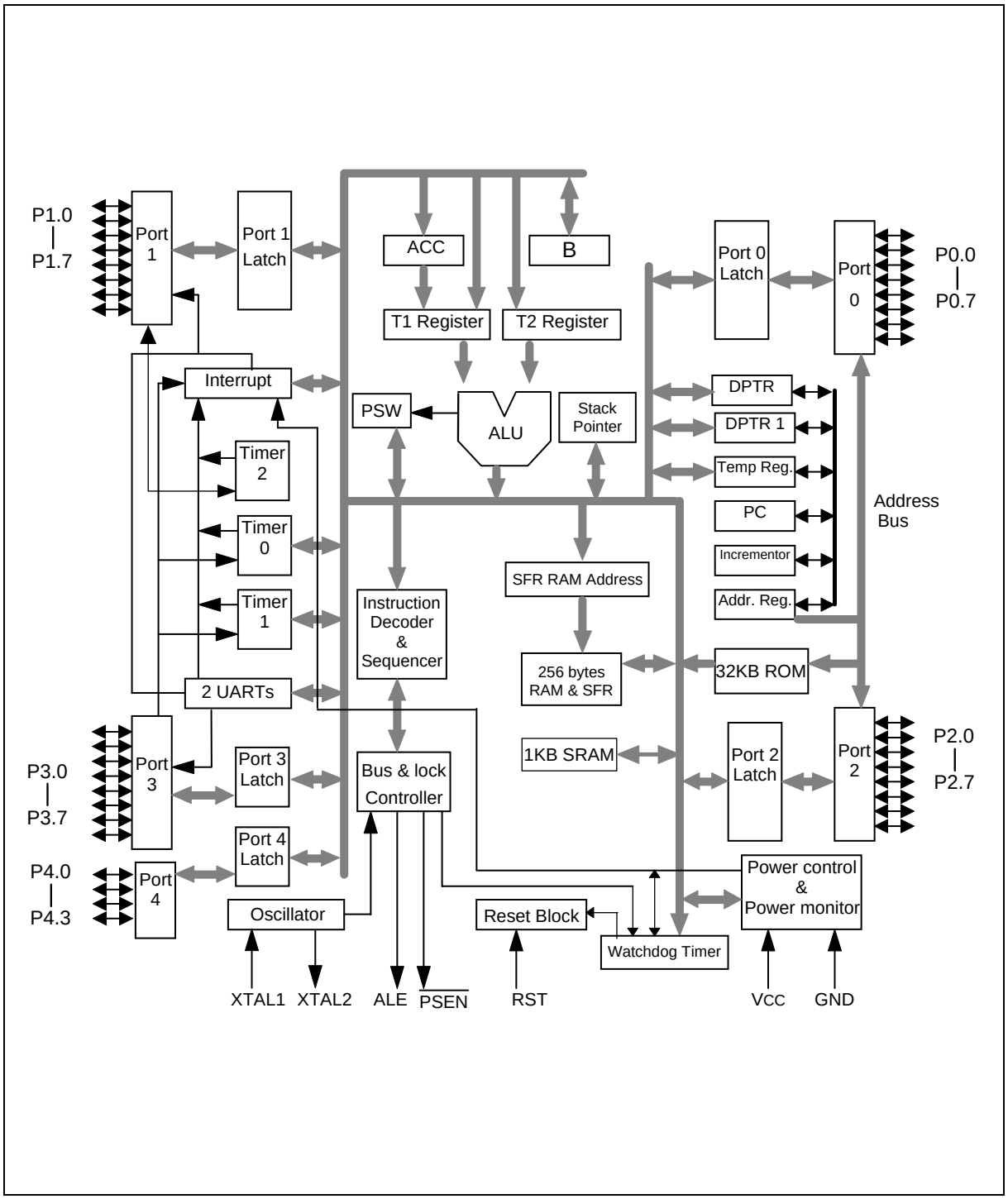
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77i058a25pl

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

The W77IE58 is 8052 pin compatible and instruction set compatible. It includes the resources of the standard 8052 such as four 8-bit I/O Ports, three 16-bit timer/counters, full duplex serial port and interrupt sources.

The W77IE58 features a faster running and better performance 8-bit CPU with a redesigned core processor without wasted clock and memory cycles. it improves the performance not just by running at high frequency but also by reducing the machine cycle duration from the standard 8052 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. The W77IE58 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers. It can also adjust the duration of the MOVX instruction (access to off-chip data memory) between two machine cycles and nine machine cycles. This flexibility allows the W77IE58 to work efficiently with both fast and slow RAMs and peripheral devices. In addition, the W77IE58 contains on-chip 1KB MOVX SRAM, the address of which is between 0000H and 03FFH. It only can be accessed by MOVX instruction; this on-chip SRAM is optional under software control.

The W77IE58 is an 8052 compatible device that gives the user the features of the original 8052 device, but with improved speed and power consumption characteristics. It has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). While the original 8051 family was designed to operate at 12 clock periods per machine cycle, the W77IE58 operates at a much reduced clock rate of only 4 clock periods per machine cycle. This naturally speeds up the execution of instructions. Consequently, the W77IE58 can run at a higher speed as compared to the original 8052, even if the same crystal is used. Since the W77IE58 is a fully static CMOS design, it can also be operated at a lower crystal clock, giving the same throughput in terms of instruction execution, yet reducing the power consumption.

The 4 clocks per machine cycle feature in the W77IE58 is responsible for a three-fold increase in execution speed. The W77IE58 has all the standard features of the 8052, and has a few extra peripherals and features as well.

I/O Ports

The W77IE58 has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 and 3 act as I/O ports with alternate functions. Port 4 is only available on 44-pin PLCC/QFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. The P4.0 has an alternate function $\overline{\text{WAIT}}$ which is the wait state control signal. When wait state control signal is enabled, P4.0 is input only.

Serial I/O

The W77IE58 has two enhanced serial ports that are functionally similar to the serial port of the original 8052 family. However the serial ports on the W77IE58 can operate in different modes in order to obtain timing similarity as well. **Note that the serial port 0 can use Timer 1 or 2 as baud rate generator, but the serial port 1 can only use Timer 1 as baud rate generator**. The serial ports have the enhanced features of Automatic Address recognition and Frame Error detection.

Timers

The W77IE58 has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W77IE58 has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

Interrupts

The Interrupt structure in the W77IE58 is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W77IE58 provides 12 interrupt resources with two priority level, including six external interrupt sources, timer interrupts, serial I/O interrupts.

Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the W77IE58, there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

Power Management

Like the standard 80C52, the W77IE58 also has IDLE and POWER DOWN modes of operation. The W77IE58 provides a new Economy mode which allow user to switch the internal clock rate divided by either 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial ports and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

On-chip Data SRAM

The W77IE58 has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. The on-chip MOVX SRAM is enabled by setting the DME0 bit in the PMR register. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H–FFFFH access to the external memory.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

Data Pointer Low1

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

This is the low byte of the new additional 16-bit data pointer that has been added to the W77IE58. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

Data Pointer High1

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

This is the high byte of the new additional 16-bit data pointer that has been added to the W77IE58. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

Data Pointer Select

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

DPS.0: This bit is used to select either the DPL, DPH pair or the DPL1, DPH1 pair as the active Data Pointer. When set to 1, DPL1, DPH1 will be selected, otherwise DPL, DPH will be selected.

DPS.1-7: These bits are reserved, but will read 0.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SM0D	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

SMOD : This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.

SMOD0: Framing Error Detection Enable: When SMOD0 is set to 1, then SCON.7(SCON1.7) indicates a Frame Error and acts as the FE(FE_1) flag. When SMOD0 is 0, then SCON.7(SCON1.7) acts as per the standard 8052 function.

GF1-0: These two bits are general purpose user flags.

PD: Setting this bit causes the W77IE58 to go into the POWER DOWN mode. In this mode all the clocks are stopped and program execution is frozen.

IDL: Setting this bit causes the W77IE58 to go into the IDLE mode. In this mode the clocks to the CPU are stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Condtrol

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

TF1: Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.

TR1: Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.

TF0: Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

TR0: Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

IE1: Interrupt 1 edge detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT1: Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

IE0: Interrupt 0 edge detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT0: Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

SM0/FE: Serial port 0, Mode 0 bit or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.

SM1: Serial port Mode bit 1:

SM0	SM1	Mode	Description	Length	Baud rate
0	0	0	Synchronous	8	4/12 Tclk
0	1	1	Asynchronous	10	variable
1	0	2	Asynchronous	11	64/32 Tclk
1	1	3	Asynchronous	11	variable

SM2: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8: This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8: In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.

TI: Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI: Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

TF2: Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.

EXF2: Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 overflow will cause this flag to set based on the CP / $\overline{RL2}$, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.

RCLK: Receive Clock Flag: This bit determines the serial port 0 time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

TCLK: Transmit Clock Flag: This bit determines the serial port 0 time-base when transmitting data in modes 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

EXEN2: Timer 2 External Enable. This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, otherwise a negative transition detected on the T2EX pin will result in capture or reload.

TR2: Timer 2 Run Control. This bit enables/disables the operation of timer 2. Clearing this bit will halt the timer 2 and preserve the current count in TH2, TL2.

C / $\overline{T2}$: Counter/Timer Select. This bit determines whether timer 2 will function as a timer or a counter. Independent of this bit, the timer will run at 2 clocks per tick when used in baud rate generator mode. If it is set to 0, then timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5), otherwise it will count negative edges on T2 pin.

CP / $\overline{RL2}$:Capture/Reload Select. This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will be ignored and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX pin if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX pin if EXEN2 = 1.

Timer 2 Mode Control

Bit:	7	6	5	4	3	2	1	0
	HC5	HC4	HC3	HC2	T2CR	-	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

Extended Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	EX5	EX4	EX3	EX2

Mnemonic: EIE Address: E8h

EIE.7-5: Reserved bits, will read high.

EWDI: Enable Watchdog timer interrupt.

EX5: External Interrupt 5 Enable.

EX4: External Interrupt 4 Enable.

EX3: External Interrupt 3 Enable.

EX2: External Interrupt 2 Enable.

Table 2. Instructions that affect Flag settings

INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

Table 3. Instruction Timing for W77IE58

INSTRUCTION	HEX OP-CODE	BYTES	W77IE58 MACHINE CYCLES	W77IE58 CLOCK CYCLES	8032 CLOCK CYCLES	W77IE58 VS. 8032 SPEED RATIO
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3

Table 3. Instruction Timing for W77IE58, continued

INSTRUCTION	HEX OP-CODE	BYTES	W77IE58 MACHINE CYCLES	W77IE58 CLOCK CYCLES	8032 CLOCK CYCLES	W77IE58 VS. 8032 SPEED RATIO
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5

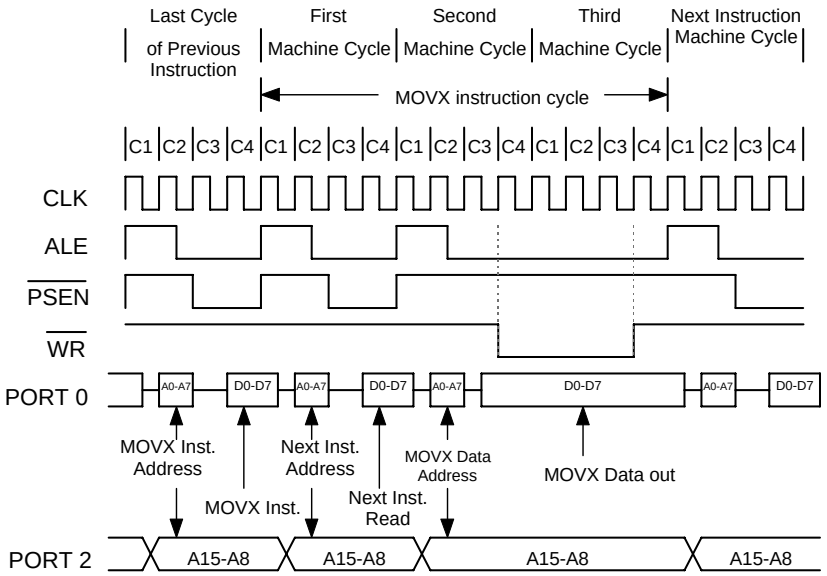


Figure 9. Data Memory Write with Stretch Value = 1

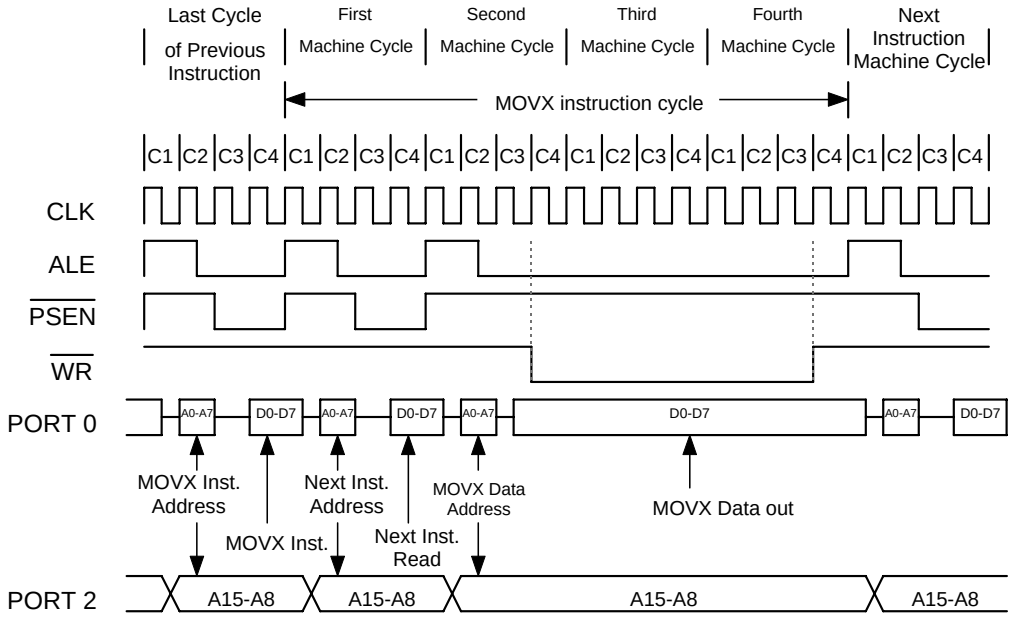


Figure 10. Data Memory Write with Stretch Value = 2

Economy Mode

The power consumption of microcontroller relates to operating frequency. The W77IE58 offers a Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64 or 1024 clocks per machine cycle. It keeps the CPU operating at a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, but all clocked peripherals such as watchdog timer are still running at a rate of clock/4. In the Economy mode, all clocked peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide a lower power consumption than idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0(PMR.6), CD1(PMR.7) decides the instruction cycle rate as below:

CD1	CD0	Clocks/Machine cycle
0	0	Reserved
0	1	4 (default)
1	0	64
1	1	1024

The selection of instruction rate is going to take effect after a delay of one instruction cycle. Switching to divide by 64 or 1024 mode must first go from divide by 4 mode. This means software can not switch directly between clock/64 and clock/1024 mode. The CPU has to return clock/4 mode first, then go to clock/64 or clock/1024 mode.

The W77IE58 allows the user to use internal RC oscillator instead of external crystal. Setting the XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or RC oscillator as the clock source. When invoking RC oscillator in Economy mode, software may set the XTOFF bit to turn off the crystal amplifier for saving power. The CPU would run at the clock rate of approximately 2–4 MHz divided by 4, 64 or 1024. The RC oscillator is not precise so that can not be invoked to the operation which needs the accurate time-base such as serial communication. The RGMD(EXIF.2) indicates current clock source. When switching the clock source, CPU needs one instruction cycle delay to take effect new setting. If crystal amplifier is disabled and RC oscillator is present clock source, software must first clear the XTOFF bit to turn on crystal amplifier before switch to crystal operation. Hardware will set the XTUP bit (STATUS.4) once the crystal is warm-up and ready for use. It is unable to set XT/$\overline{RG}$ bit to 1 if XTUP = 0.

In Economy mode, the serial port can not receive/transmit data correctly because the baud rate is changed. In some systems, the external interrupts may require the fastest process such that the reducing of operating speed is restricted. In order to solve these dilemmas, the W77IE58 offers a switchback feature which allows the CPU back to clock/4 mode immediately when triggered by serial operation or external interrupts. The switchback feature is enabled by setting the SWB bit (PMR.5). A serial port reception/transmission or qualified external interrupt which is enabled and acknowledged without block conditions will cause CPU to return to divide by 4 mode. For the serial port reception, a switchback is generated by a falling edge associated with start bit if the serial port reception is enabled. When a serial port transmission, an instruction which writes a byte of data to serial port buffer will cause a switchback to ensure the correct transmission. The switchback feature is unaffected by serial port interrupt flags. After a switchback is generated, the software can manually return the CPU to Economy mode. Note that the modification of clock control bits CD0 and CD1 will be ignored during serial port transmit/receive when switchback is enabled. The Watchdog timer reset, power-on/fail reset or external reset will force the CPU to return to divide by 4 mode.

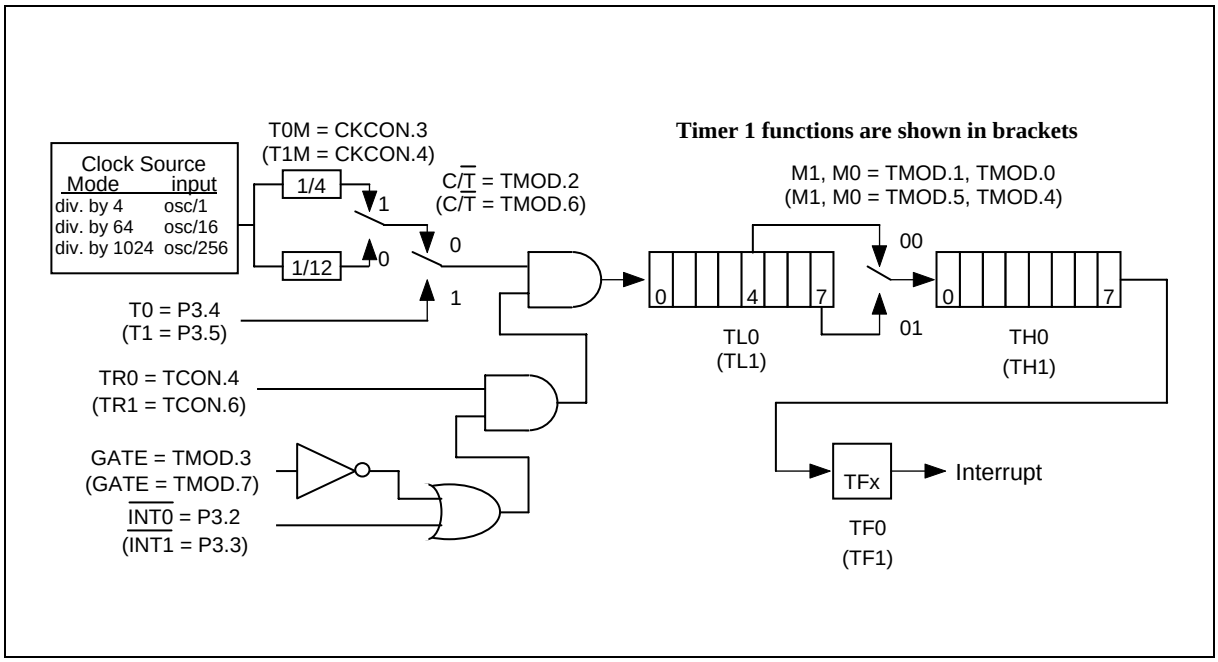


Figure 11. Timer/Counter Mode 0 & Mode 1

MODE 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

MODE 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

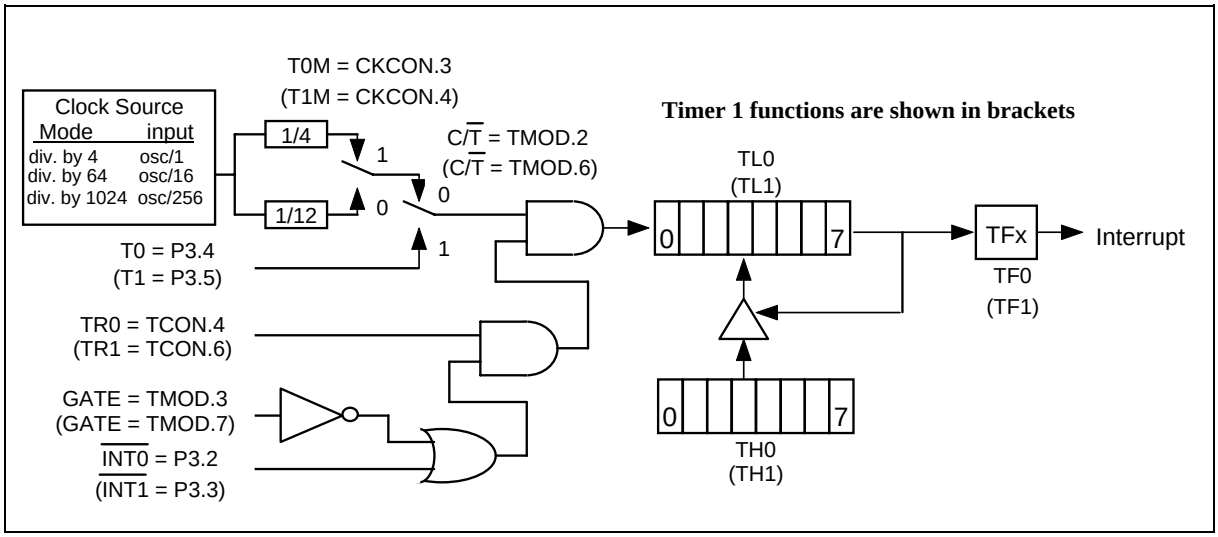


Figure 12. Timer/Counter Mode 2.

MODE 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits C / $\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2., but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

8.1.2 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 or 4 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

Timer/Counter2 Setting

MODE	RCLK+TCLK	CP/RL2	T2OE
Auto-reload	0	0	0
Capture	0	1	x
Baud Rate Generator	1	x	0
Clock Out Mode	x	0	1

Example 1: Valid access

```
MOV   TA, #0AAh      3 M/C
MOV   TA, #055h      3 M/C
MOV   WDCON, #00h    3 M/C
```

Note: M/C = Machine Cycles

Example 2: Valid access

```
MOV   TA, #0AAh      3 M/C
MOV   TA, #055h      3 M/C
NOP                  1 M/C
SETB  EWT            2 M/C
```

Example 3: Valid access

```
MOV   TA,#0AAh       3M/C
MOV   TA,#055h       3M/C
ORL   WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
MOV   TA, #0AAh      3 M/C
MOV   TA, #055h      3 M/C
NOP                  1 M/C
NOP                  1 M/C
CLR   POR            2 M/C
```

Example 5: Invalid Access

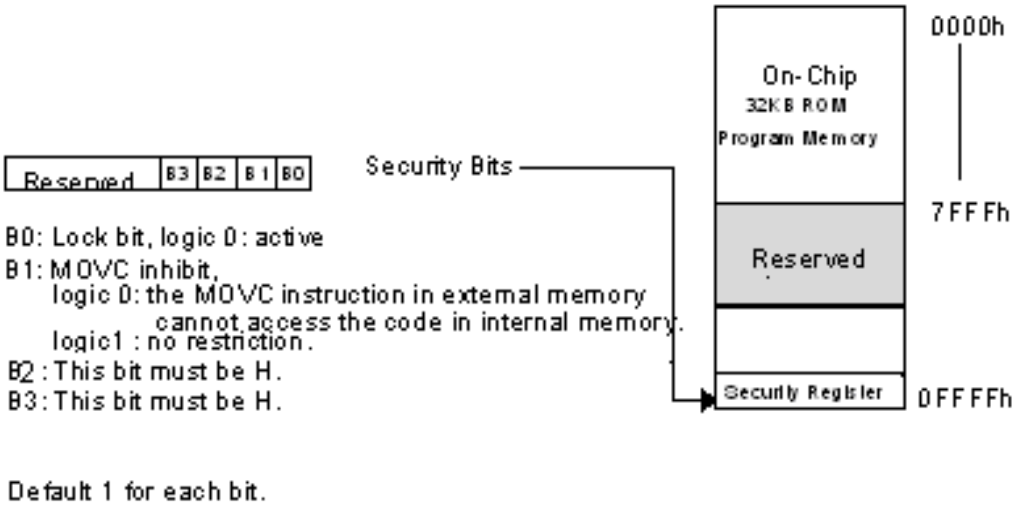
```
MOV   TA, #0AAh      3 M/C
NOP                  1 M/C
MOV   TA, #055h      3 M/C
SETB  EWT            2 M/C
```

In the first two examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 3, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 4, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window in not opened at all, and the write to the protected bit fails.

11. SECURITY BITS

During the on-chip ROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W77IE58 has several Special Setting Registers, including the Security Register, which can not be accessed in normal mode. These registers can only be accessed from the ROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the ROM operation mode by address #0FFFFh.



Special Setting Registers

B0: Lock bit

This bit is used to protect the customer's program code in the W77IE58. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the ROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

D.C. Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.2	V_{DD} +0.2	V	V_{DD} = 3.0V
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	V_{DD} +0.2	V	V_{DD} = 3.0V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.40	V	V_{DD} = 3V, I_{OL} = +4 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +10 mA
		-	0.40	V	V_{DD} = 3V, I_{OL} = +6 mA
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -120 μA V_{DD} = 3.0V, I_{OH} = -45 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -8 mA V_{DD} = 3.0V, I_{OH} = -3 mA

Notes:

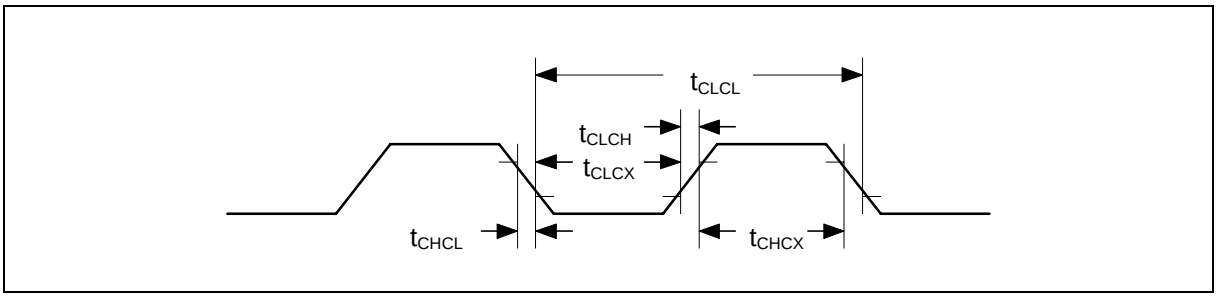
*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

12.3 A.C. Characteristics



Note: Duty cycle is 50%.

External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	20	-	-	nS	
Clock Low Time	t_{CLCX}	20	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

MOVX Characteristics Using Stretch Memory Cycles, continued

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRETCH
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		2.0 t_{CLCL} - 20 t_{MCS} - 20	nS	t_{MCS} = 0 t_{MCS}>0
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		t_{CLCL} - 5 2.0 t_{CLCL} - 5	nS	t_{MCS} = 0 t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		2.5 t_{CLCL} - 5 t_{MCS} + 2 t_{CLCL} - 40	nS	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		3.0 t_{CLCL} - 20 2.0 t_{CLCL} - 5	nS	t_{MCS} = 0 t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	0.5 t_{CLCL} - 5 1.5 t_{CLCL} - 5	0.5 t_{CLCL} + 5 1.5 t_{CLCL} + 5	nS	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	t_{CLCL} - 5 2.0 t_{CLCL} - 5		nS	t_{MCS} = 0 t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	1.5 t_{CLCL} - 5 2.5 t_{CLCL} - 5		nS	t_{MCS} = 0 t_{MCS}>0
Data Valid to WR Transition	t_{QVWX}	-5 1.0 t_{CLCL} - 5		nS	t_{MCS} = 0 t_{MCS}>0
Data Hold after Write	t_{WHQX}	t_{CLCL} - 5 2.0 t_{CLCL} - 5		nS	t_{MCS} = 0 t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		0.5 t_{CLCL} - 5	nS	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 1.0 t_{CLCL} - 5	10 1.0 t_{CLCL} + 5	nS	t_{MCS} = 0 t_{MCS}>0

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

M2	M1	M0	MOVX CYCLES	T_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logic Symbols

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{\text{PSEN}}$
Q	Output Data	R	$\overline{\text{RD}}$ signal
V	Valid	W	$\overline{\text{WR}}$ signal
X	No longer a valid state	Z	Tri-state

Typical Application Circuits, continued

14.2 Expanded External Data Memory and Oscillator

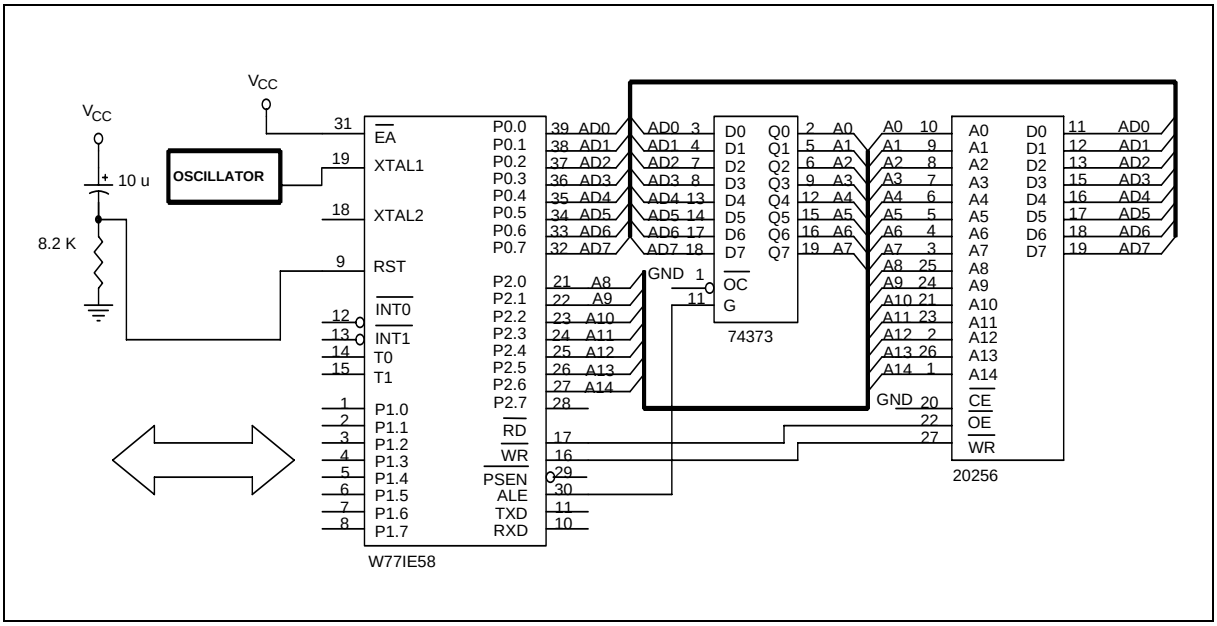


Figure B