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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ll36clh

1 Addendum for Revision 7

Table 1. MC9S08LL64 Data Sheet Rev 7 Addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 3.7, “Supply Current Characteristics”/Table 9/Page 23</td><td>In the table, for numbers 3 and 4, change “LPS” to “LPR”.</td></tr>
<tr><td>Section 3.12, “ADC Characteristics”/Page 33</td><td>Add the following data of the ADC conversion clock frequency:
<table>
<tr><th>Characteristic</th><th>Conditions</th><th>Symb</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="3">ADC Conversion Clock Frequency</td><td>ADLPC=0, ADHSC=1</td><td rowspan="3">f_{ADCK}</td><td>1.0</td><td>—</td><td>8</td><td rowspan="3">MHz</td></tr>
<tr><td>ADLPC=0, ADHSC=0</td><td>1.0</td><td>—</td><td>5</td></tr>
<tr><td>ADLPC=1, ADHSC=0</td><td>1.0</td><td>—</td><td>2.5</td></tr>
</table></td></tr>
</table>

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release. Correct errors in the following sections: • Section 3.7, “Supply Current Characteristics” • Section 3.12, “ADC Characteristics”	07/2012

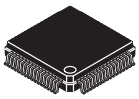
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LL64
Rev. 7, 4/2012

An Energy Efficient Solution by Freescale

MC9S08LL64 Series

Covers: MC9S08LL64 and MC9S08LL36



64-LQFP
Case 840F

80-LQFP
Case 917A

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 3.6 V to 2.1 V across temperature range of –40 °C to 85 °C
  - Up to 20 MHz at 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual array flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes
  - Reduced-power wait mode
  - Low-power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Very low-power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to time-of-day (TOD) module
  - 6 μs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 20 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset; illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes
- Peripherals
  - LCD — Up to 8×36 or 4×40 LCD driver with internal charge pump and option to provide an internally-regulated LCD reference that can be trimmed for contrast control
  - ADC —10-channel, 12-bit resolution; up to 2.5 μs conversion time; automatic compare function; temperature sensor; operation in stop3; fully functional from 3.6 V to 1.8 V
  - IIC — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; broadcast mode; 10-bit addressing
  - ACMP — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - SCIx — Two full-duplex non-return to zero (NRZ) modules (SCI1 and SCI2); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - SPI — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - TPMx — Two 2-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - TOD — (Time-of-day) 8-bit, quarter second counter with match register; external clock source for precise time base, time-of-day, calendar, or task scheduling functions
  - VREFx — Trimmable via an 8-bit register in 0.5 mV steps; automatically loaded with room temperature value upon reset; can be enabled to operate in stop3 mode; trim register is not available in stop modes.
- Input/Output
  - Dedicated accurate voltage reference output pin, 1.15 V output (VREFOx); trimmable with 0.5 mV resolution
  - Up to 39 GPIOs, two output-only pins
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - 14mm × 14mm 80-pin LQFP, 10 mm × 10 mm 64-pin LQFP

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Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
3	03/2009	Incorporated revisions for customer release.
4	08/2009	Completed all the TBDs; corrected Pin out in the Figure 2, Figure 3 and Table 2; updated V_{OH}, $\|I_{In}\|$, $\|I_{OZ}\|$, R_{PU}, R_{PD}, added $\|I_{INT}\|$ in the Table 8; updated Table 9; updated ERREFSTEN and added LCD in the Table 10; updated f_{ADACK}, E_{TUE}, DNL, INL, E_{ZS} and E_{FS} in the Table 18. updated V Room Temp in the Table 19.
5	1/2010	Added 80-pin LQFP package information for MC9S08LL36.
6	6/2011	Changed the ERREFSTEN to EREFSTEN, updated the VREFOx to 1.15 V Added LCD specification in the Table 10.
7	4/2012	Updated $\|I_{In}\|$ in the Table 8.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual —MC9S08LL64RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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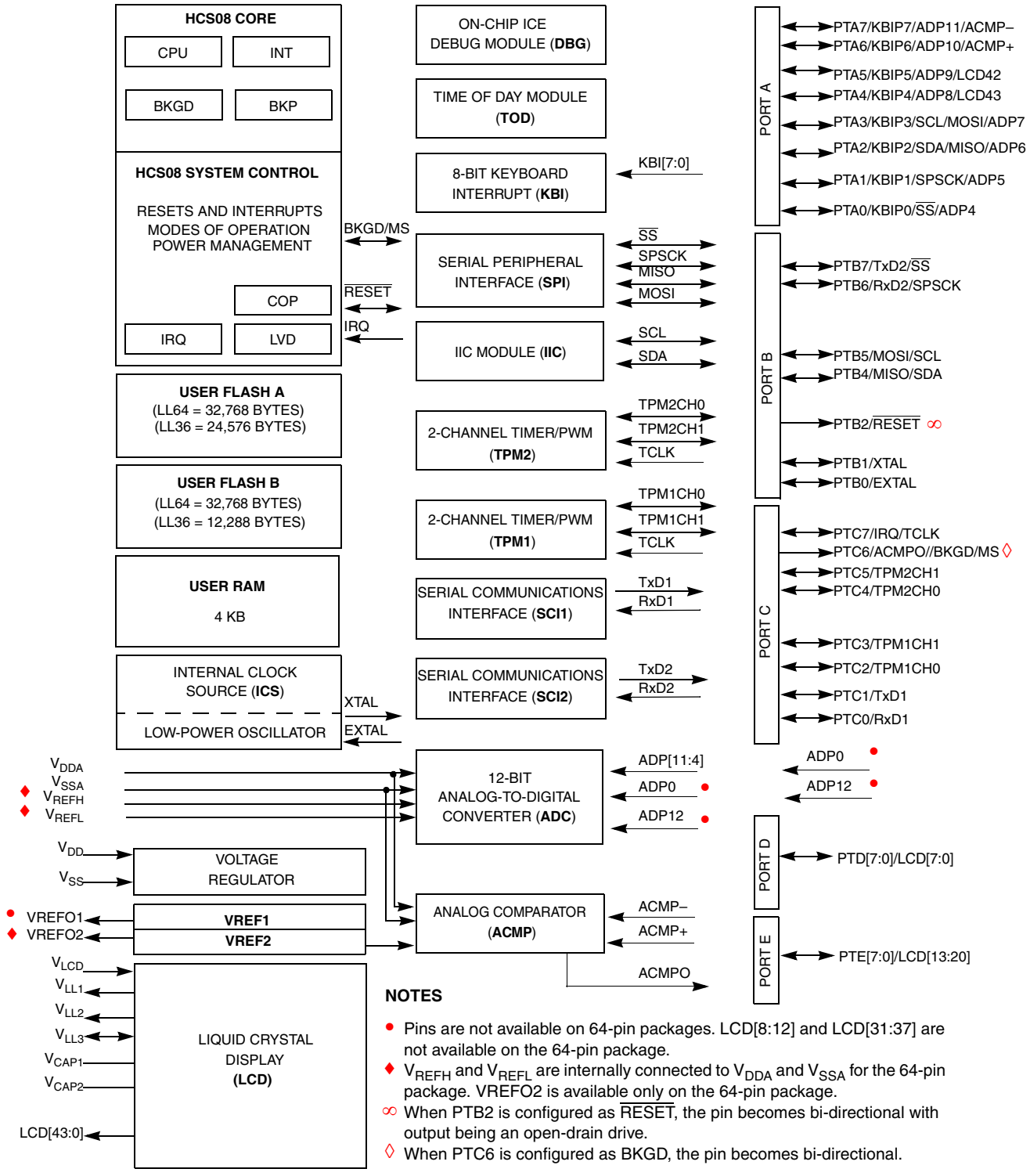


Figure 1. MC9S08LL64 Series Block Diagram

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LL64 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 6. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

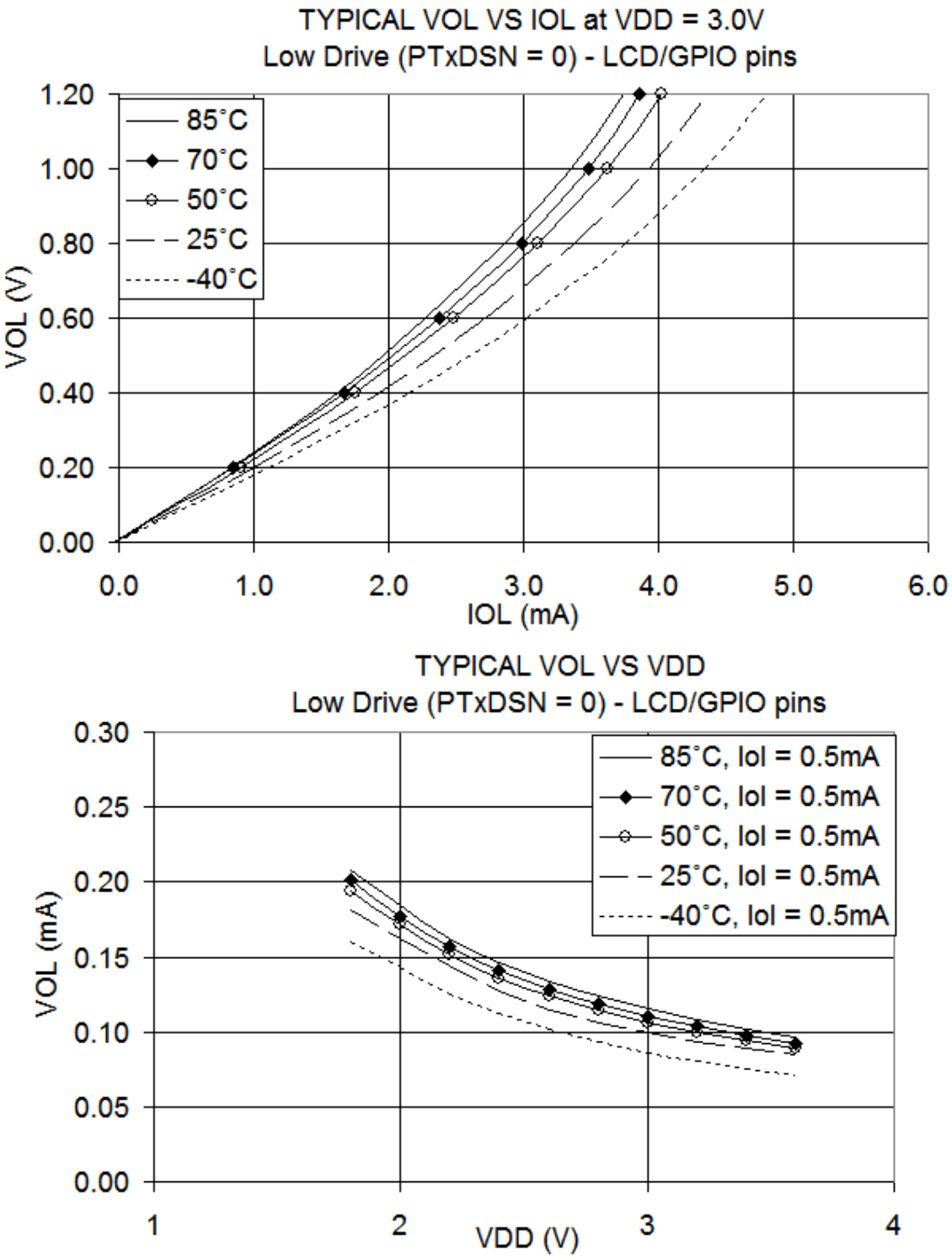


Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

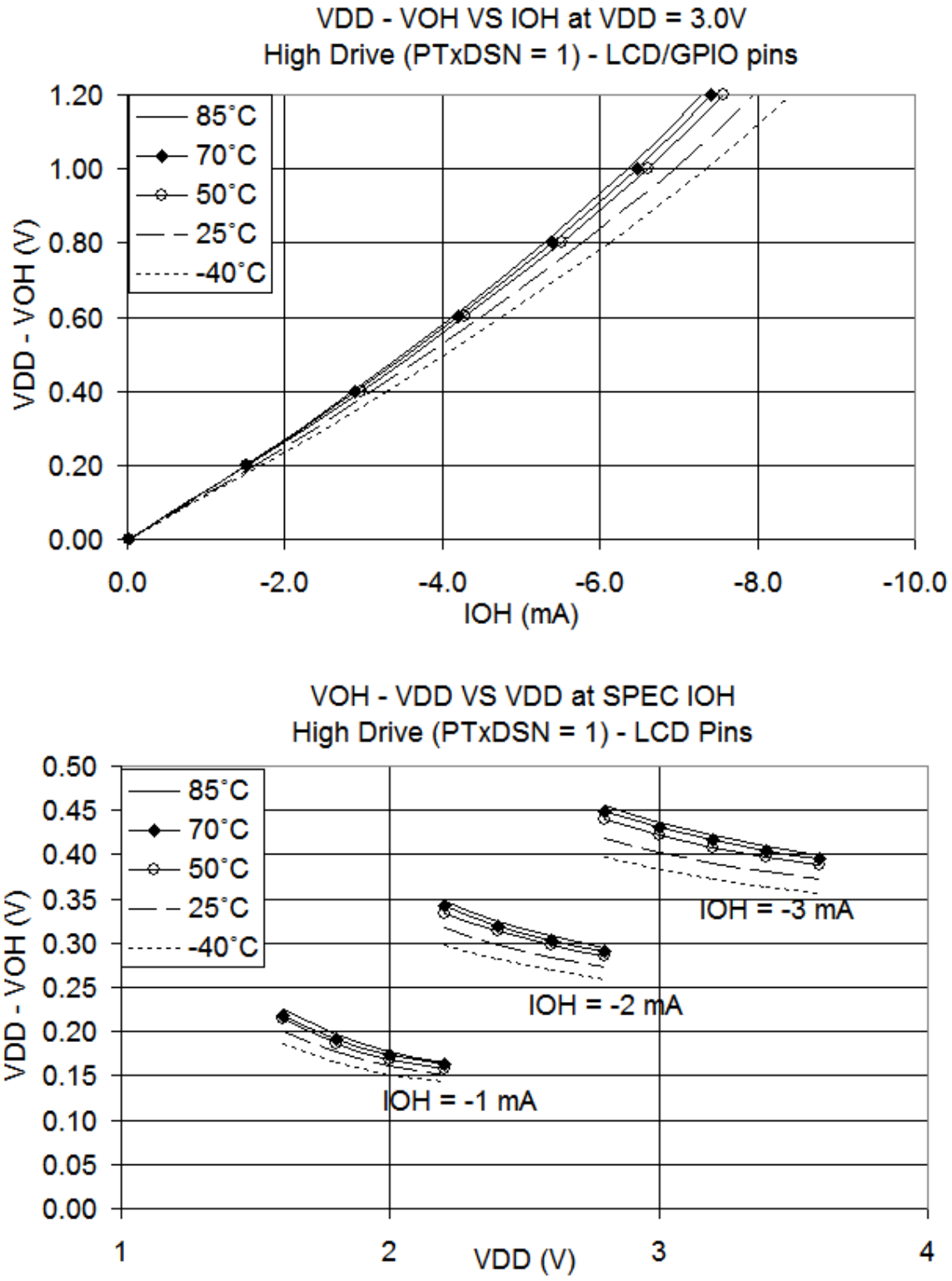


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	T	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	13.75	17.9	mA	–40 to 85
	T			10 MHz		7	—		
	T			1 MHz		2	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	8.9	—	mA	–40 to 85
	T			10 MHz		5.5	—		
	T			1 MHz		0.9	—		
3	T	Run supply current LPS=0, all modules on	RI_{DD}	16 kHz FBILP	3	185	—	µA	–-40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	25	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	4.57	6	mA	–40 to 85
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.4	1.3	µA	–40 to 25
	C					4	6		70
	P					8.5	13		85
	C				2	0.35	1		–40 to 25
	C					3.9	5		70
	C					7.7	10		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.65	1.8	µA	–40 to 25
	C					5.7	8		70
	P					12.2	20		85
	C				2	0.6	1.5		–40 to 25
	C					5	6.8		70
	C					11.5	14		85

[1] Typical values are measured at 25 °C. Characterized, not tested

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	± 0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

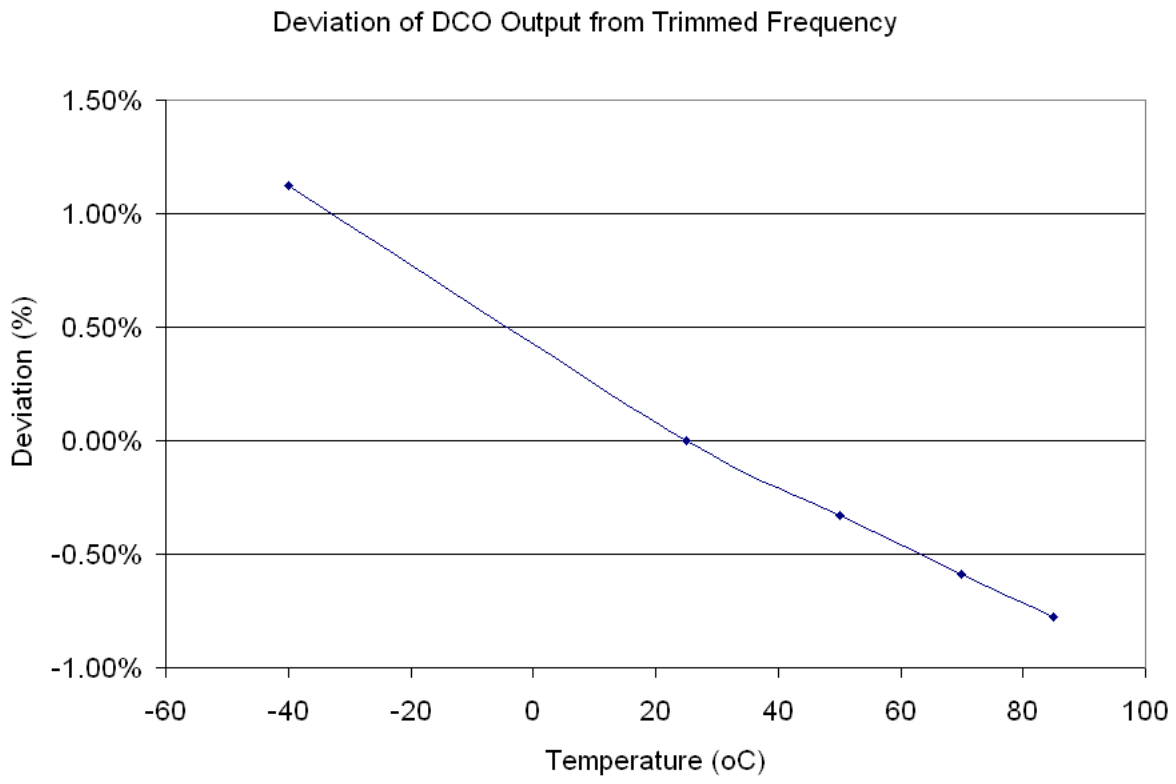


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \leq 2.1V$ $V_{DD} > 2.1V$	f_{Bus}	 dc dc	 — —	 10 20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

6 Except for LCD pins in open drain mode.

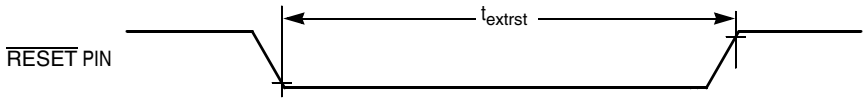


Figure 17. Reset Timing

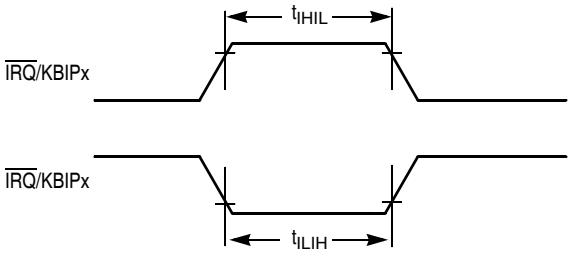


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

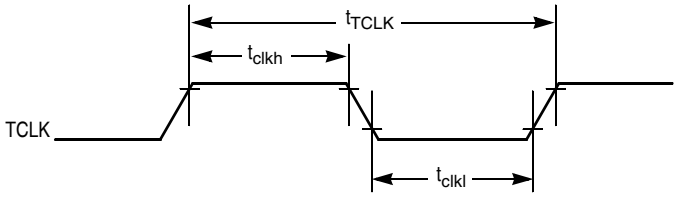


Figure 19. Timer External Clock

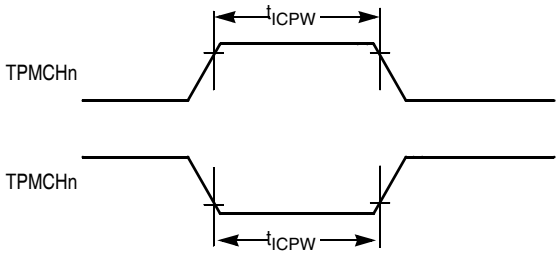


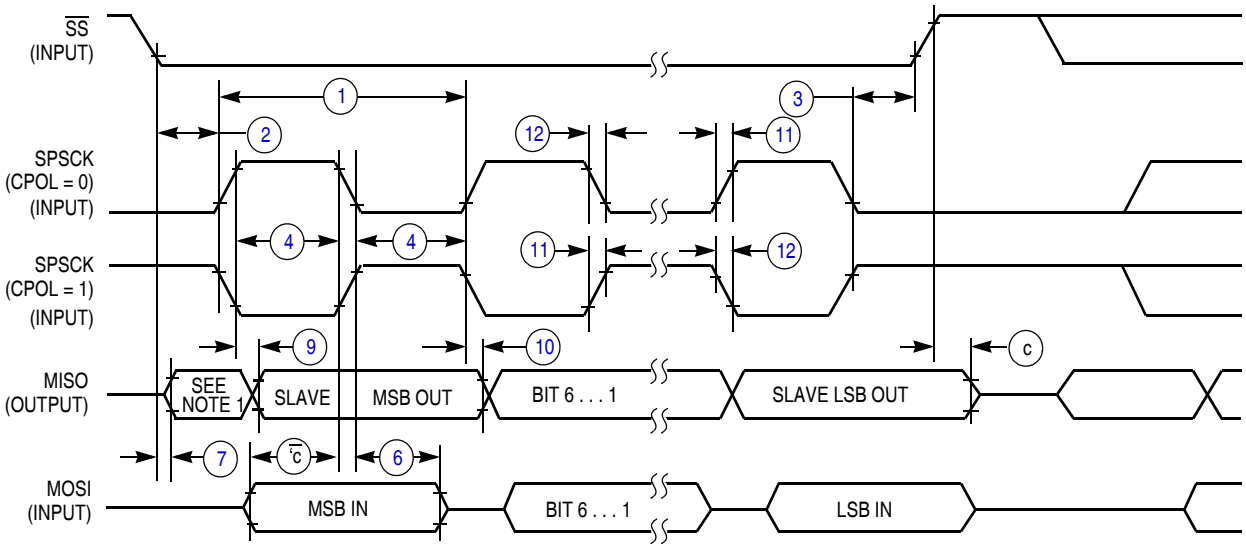
Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns



NOTE:
1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

No	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.8	—	3.6	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	P	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
6	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
7	C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 12-Bit ADC Operating Conditions

No.	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V
		Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply current	ADLPC = 1 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	200	—	μA	
2	Supply current	ADLPC = 1 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	280	—	μA	
3	Supply current	ADLPC = 0 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	370	—	μA	
4	Supply current	ADLPC = 0 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	0.61	—	mA	
5	Supply current	Stop, reset, module off		I_{DDA}	—	0.01	0.8	μA	
6	ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low power (ADLPC = 1)			1.25	2	3.3		
7	Sample time	Single/first continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	6	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	10	—		
8	Sample time	Subsequent continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	4	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	8	—		

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
9	Sample time	Subsequent Continuous or Single/First Continuous ADLSMP = 1							
		ADHSC = 0 ADLSMP = 1 ADLSTS = 00	C	ts	—	24	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 01	C	ts	—	16	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 10	C	ts	—	10	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 11	C	ts	—	6	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 00	C	ts	—	28	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 01	C	ts	—	20	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 10	C	ts	—	14	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 11	C	ts	—	10	—		
10	Total unadjusted error	12-bit mode $3.6 > V_{DDA} > 2.7V$	T	E_{TUE}	—	–2.5 to 3.25	±4	LSB[2]	Includes quantization
		12-bit mode, $2.7 > V_{DDA} > 1.8V$	T			±3.25	–5.5 to 6.5		
		10-bit mode	T		—	±1	±2.5		
		8-bit mode	T		—	±0.5	±1.0		
11	Differential non-linearity	12-bit mode	T	DNL	—	–1 to 1.75	–1.5 to 2.5	LSB[2]	
		10-bit mode[3]	T		—	±0.5	±1.0		
		8-bit mode[3]	T		—	±0.3	±0.5		

3.14 LCD Specifications

Table 20. LCD Electricals, 3-V Glass

No.	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	D	LCD supply voltage	V_{LCD}	.9	1.5	1.8	V
2	D	LCD frame frequency	f_{Frame}	28	30	58	Hz
3	D	LCD charge pump capacitance	C_{LCD}	—	100	100	nF
4	D	LCD bypass capacitance	C_{BYLCD}	—	100	100	nF
5	D	LCD glass capacitance	C_{glass}	—	2000	8000	pF
6	D	V_{IREG} HRefSel = 0	V_{IREG}	.89	1.00	1.15	V
7		V_{IREG} HRefSel = 1		1.49	1.67	1.85[1]	
8	D	V_{IREG} trim resolution	Δ_{RTRIM}	1.5	—	—	% V_{IREG}
9	D	V_{IREG} ripple HRefSel = 0	—	—	—	.1	V
10		V_{IREG} ripple HRefSel = 1	—	—	—	.15	
11	D	V_{LCD} buffered adder[2]	I_{Buff}	—	1		µA

1 V_{IREG} Max can not exceed V_{DD} –.15 V
2 VSUPPLY = 10, BYPASS = 0

3.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 21. Flash Characteristics

No.	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
5	P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	D	Byte program current[3]	R_{IDDBP}	—	4	—	mA

Table 22. Device Numbering System

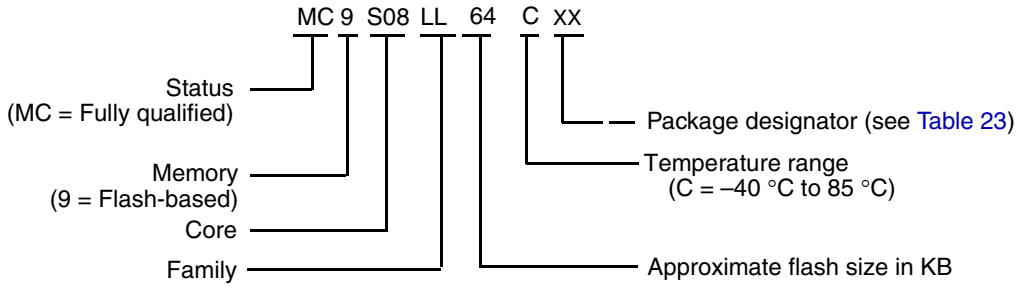
Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08LL64	64 KB	4000	80 LQFP
	64 KB	4000	64 LQFP
MC9S08LL36	36 KB	4000	80 LQFP
	36 KB	4000	64 LQFP

1 See Table 1 for a complete description of modules included on each device.

2 See Table 23 for package information.

4.1 Device Numbering System

Example of the device numbering system:



4.2 Package Information

Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W

4.3 Mechanical Drawings

Table 23 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LL64 series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 23, or
- Open a browser to the Freescale website (http://www.freescale.com), and enter the appropriate document number (from Table 23) in the “Enter Keyword” search box at the top of the page.

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