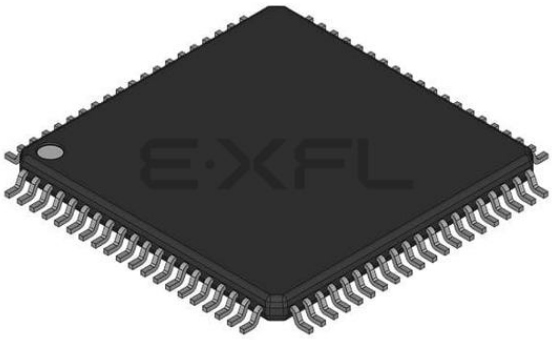

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08ll36clk

Freescale Semiconductor
Data Sheet Addendum

MC9S08LL64AD
Rev. 1, 08/2012

MC9S08LL64 Data Sheet Addendum

by: Automotive and Industrial Solutions Group

This document describes corrections to the *MC9S08LL64 Series Data Sheet*, order number MC9S08LL64. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MC9S08LL64 Series Data Sheet* is Revision 7.

Table of Contents

Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
3	03/2009	Incorporated revisions for customer release.
4	08/2009	Completed all the TBDs; corrected Pin out in the Figure 2, Figure 3 and Table 2; updated V_{OH}, $\|I_{In}\|$, $\|I_{OZ}\|$, R_{PU}, R_{PD}, added $\|I_{INT}\|$ in the Table 8; updated Table 9; updated ERREFSTEN and added LCD in the Table 10; updated f_{ADACK}, E_{TUE}, DNL, INL, E_{ZS} and E_{FS} in the Table 18. updated V Room Temp in the Table 19.
5	1/2010	Added 80-pin LQFP package information for MC9S08LL36.
6	6/2011	Changed the ERREFSTEN to EREFSTEN, updated the VREFOx to 1.15 V Added LCD specification in the Table 10.
7	4/2012	Updated $\|I_{In}\|$ in the Table 8.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual —MC9S08LL64RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

freescale semiconductor

1 Devices in the MC9S08LL64 Series

Table 1 summarizes the feature set available in the MC9S08LL64 series of MCUs.

Table 1. MC9S08LL64 Series Features by MCU and Package

Feature	MC9S08LL64		MC9S08LL36	
Package	**80-pin LQFP**	**64-pin LQFP**	**80-pin LQFP**	**64-pin LQFP**
FLASH	64 KB (32,768 and 32,768 Arrays)		36 KB (24,576 and 12,288 Arrays)	
RAM	4000		4000	
ACMP	yes		yes	
ADC	10-ch	8-ch	10-ch	8-ch
IIC	yes		yes	
IRQ	yes		yes	
KBI	8		8	
SCI1	yes		yes	
SCI2	yes		yes	
SPI	yes		yes	
TPM1	2-ch		2-ch	
TPM2	2-ch		2-ch	
TOD	yes		yes	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO1	yes	no	yes	no
VREFO2	no	yes	no	yes
I/O pins[1]	39	37	39	37

[1] The 39 I/O pins include two output-only pins and 18 LCD GPIO.

The block diagram in Figure 1 shows the structure of the MC9S08LL64 series MCU.

2 Pin Assignments

This section shows the pin assignments for the This section shows the pin assignments for the MC9S08LL64 series devices.

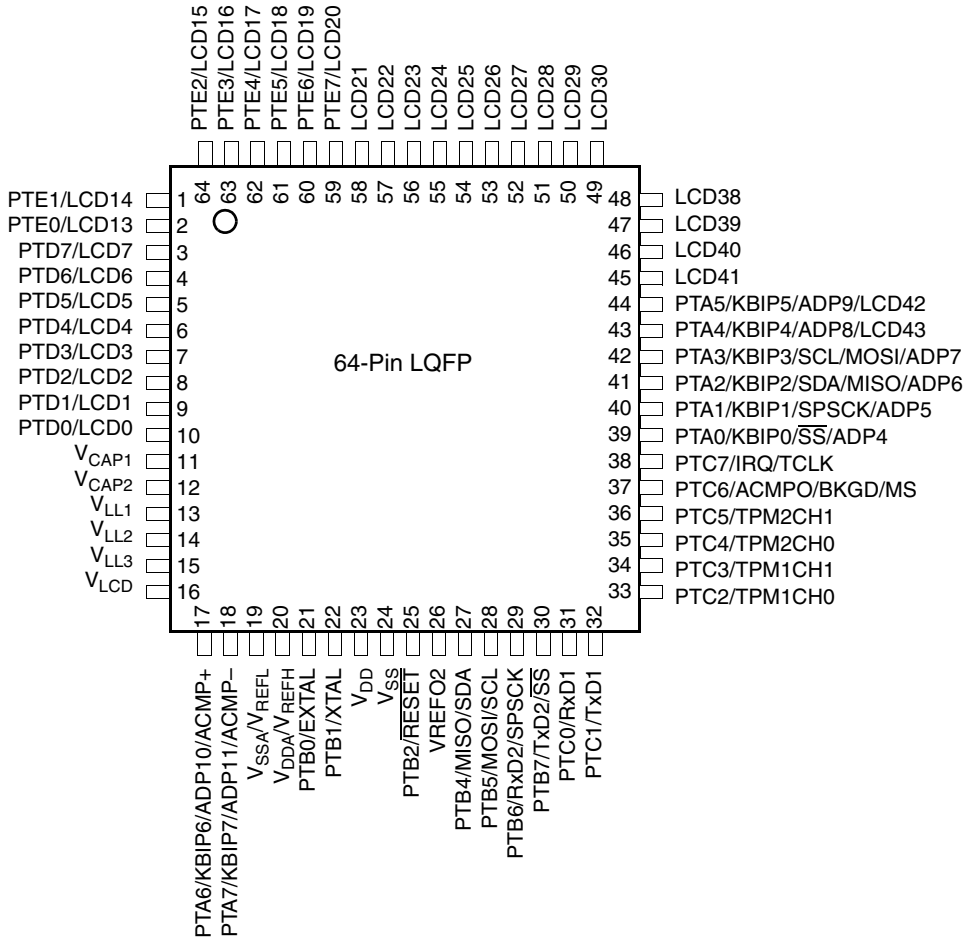

Figure 2. 64-Pin LQFP

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
44	36	PTC5	TPM2CH1			
45	37	PTC6	ACMPO	BKGD	MS	
46	38	PTC7	IRQ	TCLK		
47	39	PTA0	KBIP0		$\overline{SS}$	ADP4
48	40	PTA1	KBIP1		SPSCK	ADP5
49	41	PTA2	KBIP2	SDA	MISO	ADP6
50	42	PTA3	KBIP3	SCL	MOSI	ADP7
51	43	PTA4	KBIP4	ADP8	LCD43	
52	44	PTA5	KBIP5	ADP9	LCD42	
53	45	LCD41				
54	46	LCD40				
55	47	LCD39				
56	48	LCD38				
57		LCD37				
58		LCD36				
59		LCD35				
60		LCD34				
61		LCD33				
62		LCD32				
63		LCD31				
64	49	LCD30				
65	50	LCD29				
66	51	LCD28				
67	52	LCD27				
68	53	LCD26				
69	54	LCD25				
70	55	LCD24				
71	56	LCD23				
72	57	LCD22				
73	58	LCD21				
74	59	PTE7	LCD20			
75	60	PTE6	LCD19			
76	61	PTE5	LCD18			
77	62	PTE4	LCD17			
78	63	PTE3	LCD16			
79	64	PTE2	LCD15			
80	1	PTE1	LCD14			

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	55	°C/W
64-pin LQFP		73	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	42	°C/W
64-pin LQFP		54	

The average chip-junction temperature (T_J) in °C can be obtained from:

Table 6. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current — all input only pins except for LCD only pins (LCD 8-12, 21-41)	$\lvert I_{In} \rvert$	V_{In} = V_{DD}	—	0.025	1	µA
				V_{In} = V_{SS}	—	0.025	1	µA
		Input leakage current — LCD only pins (LCD 8-12, 21-41)		V_{In} = V_{DD}	—	100	150	µA
				V_{In} = V_{SS}	—	0.025	1	µA
12	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	µA
13	P	Total leakage current[3] — Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	3	µA
14	P	Pullup, Pulldown resistors — all non-LCD pins when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors — LCD/GPIO pins when enabled	R_{PU}, R_{PD}		35	—	77	kΩ
16	D	DC injection current[4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current[4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
18	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
19	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	2.0	V
20	D	POR re-arm time	t_{POR}		10	—	—	µs
21	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
22	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
23	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
24	P	Bandgap Voltage Reference[8]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 All I/O pins except for LCD pins in Open Drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

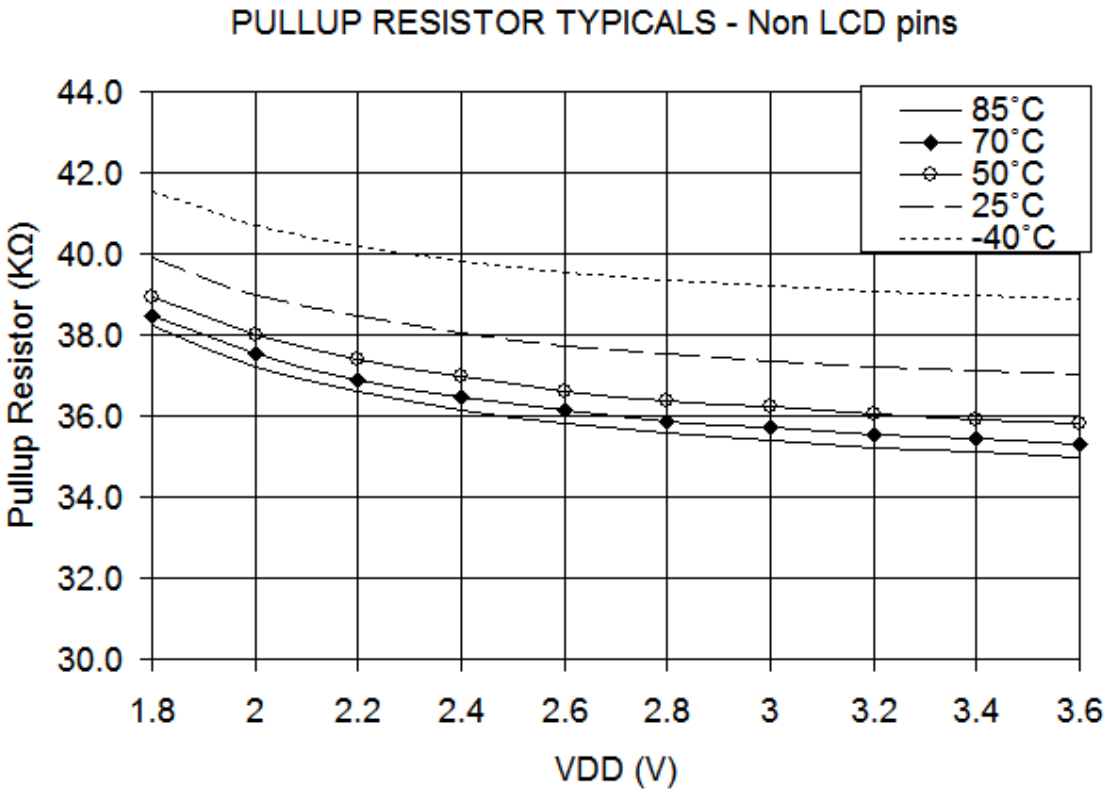

Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

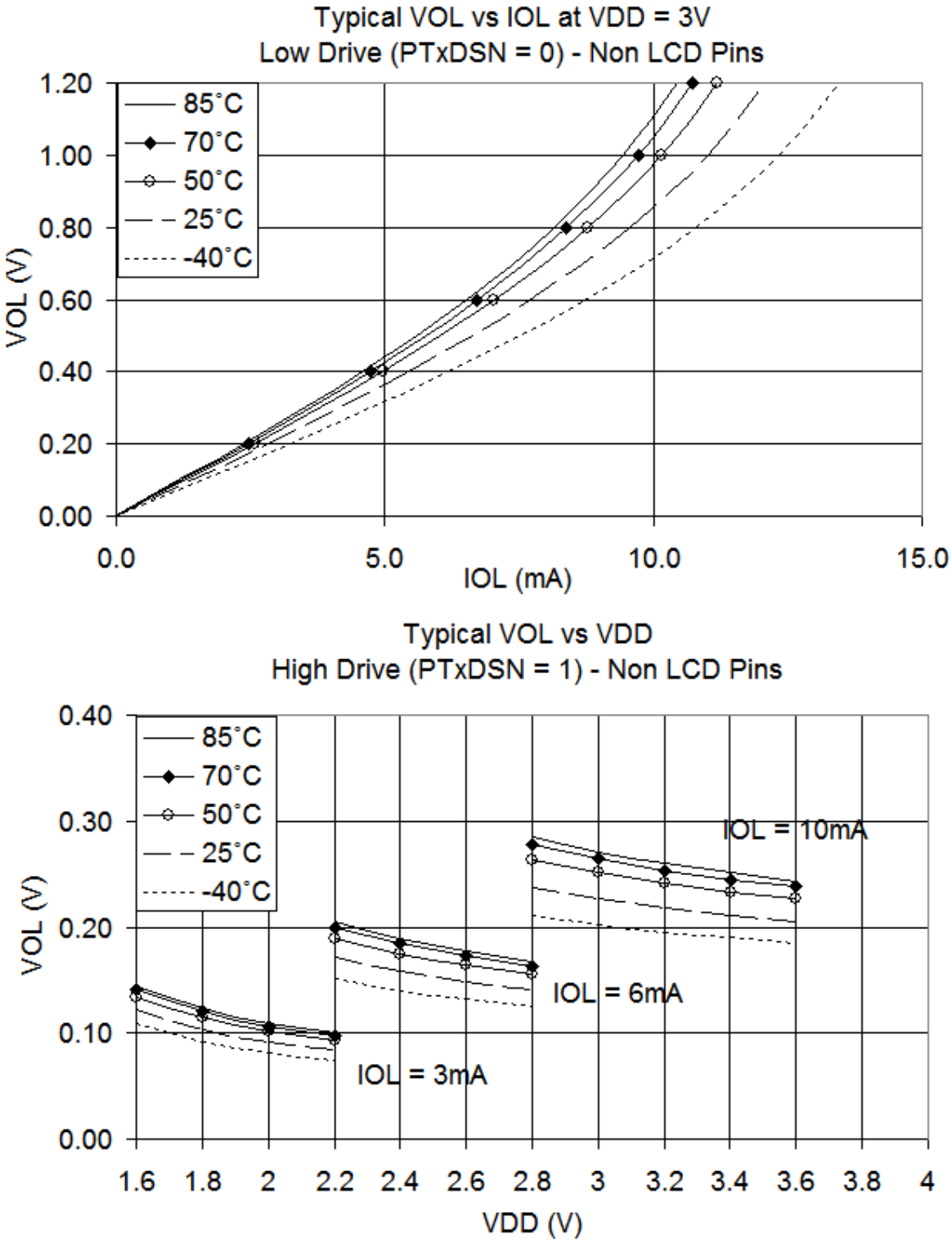

Figure 6. Typical Low-Side Driver (Sink) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

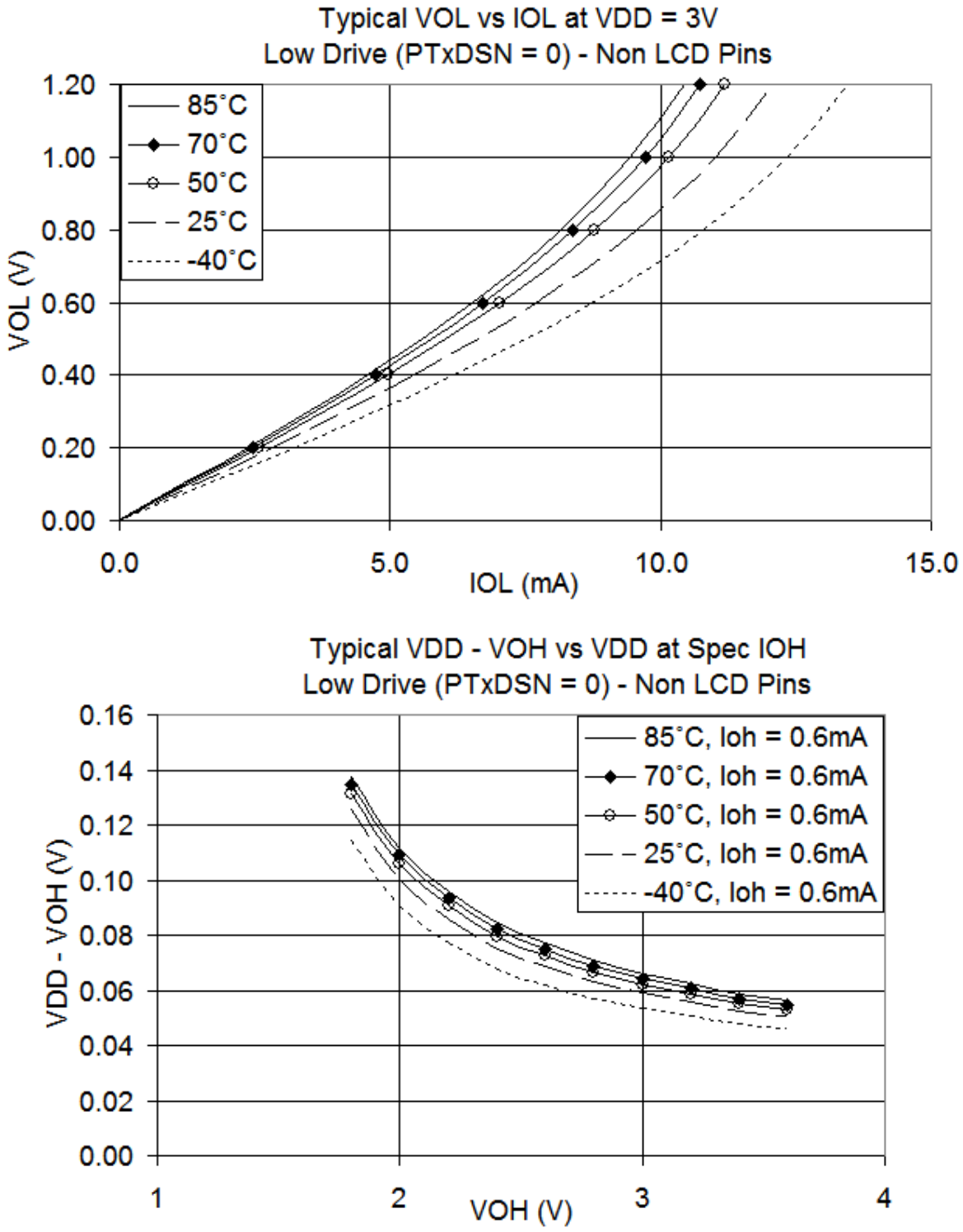

Figure 7. Typical High-Side (Source) Characteristics (Non LCD Pins)— Low Drive (PTxDSn = 0)

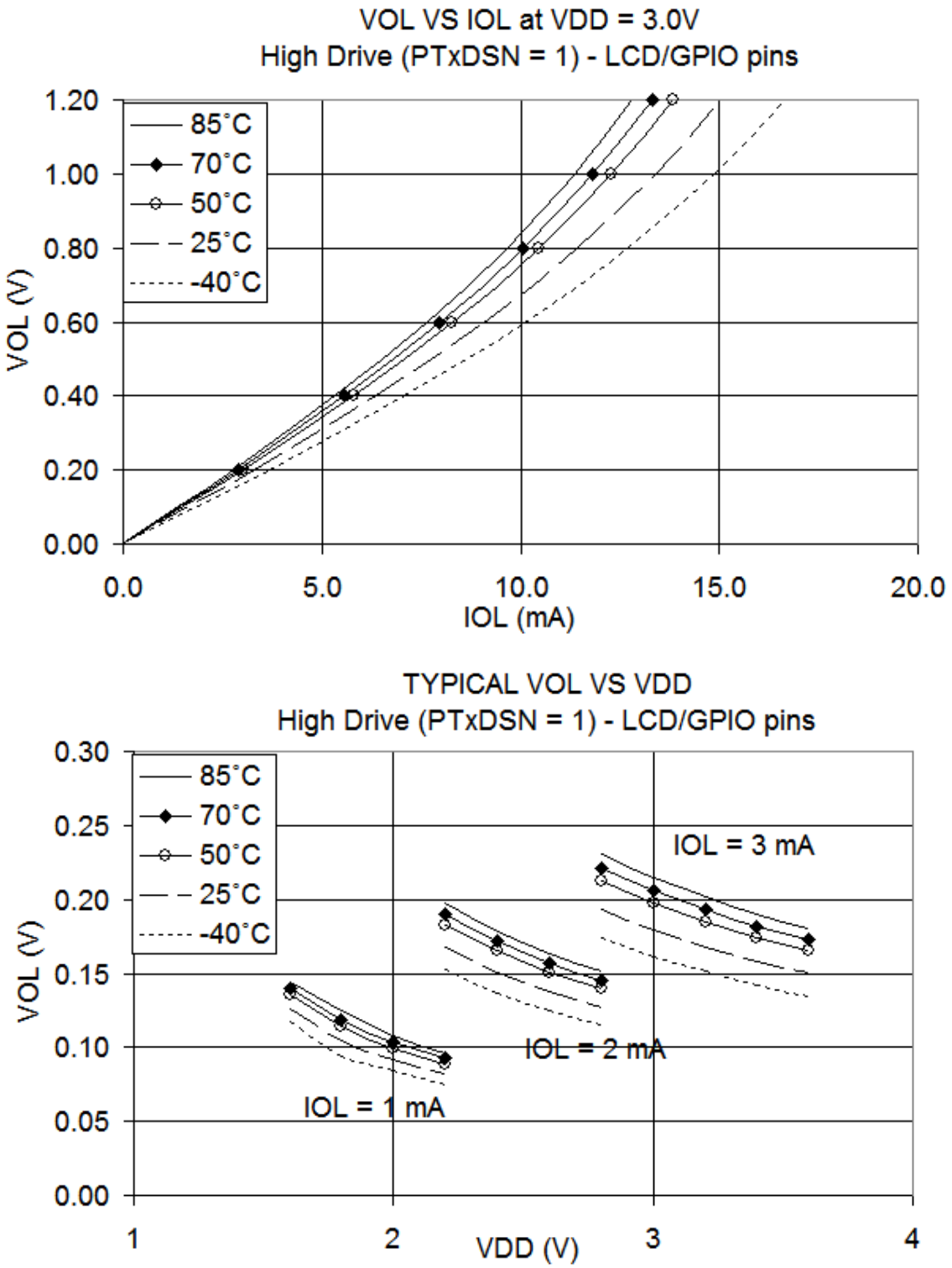

Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

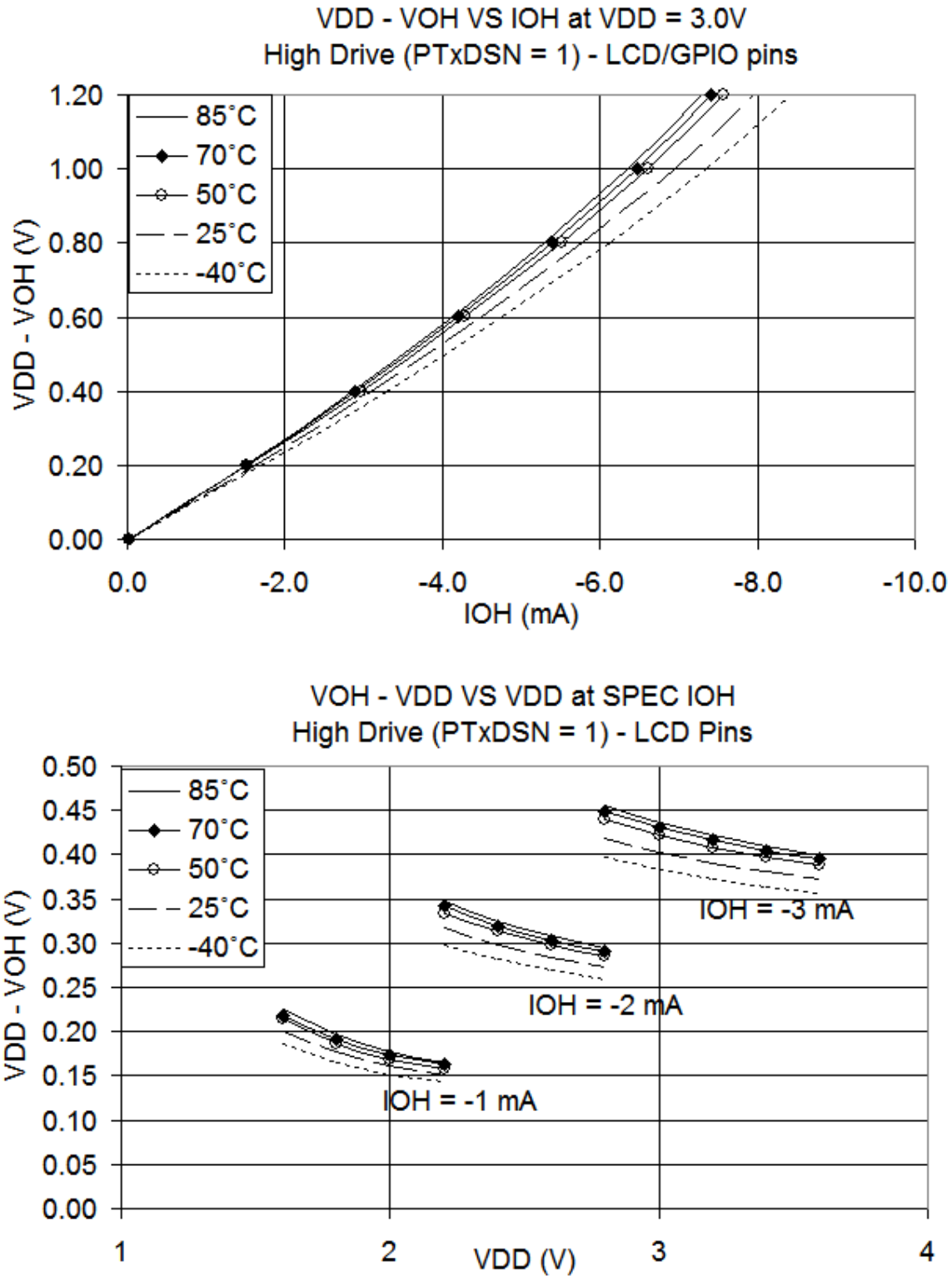

Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

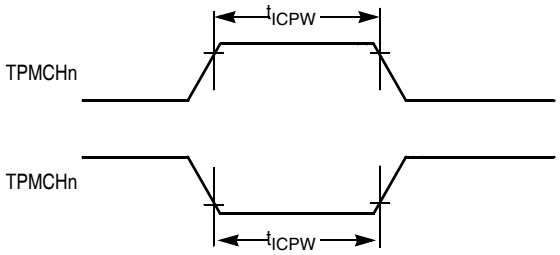

Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns

Table 17. 12-Bit ADC Operating Conditions (continued)

No.	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
2	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV
3	Reference voltage high	—	V_{REFH}	1.8	V_{DDA}	V_{DDA}	V
4	Reference voltage low	—	V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V
5	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
6	Input capacitance	8/10/12-bit modes	C_{ADIN}	—	4	5	pF
7	Input resistance	—	R_{ADIN}	—	5	7	kΩ

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

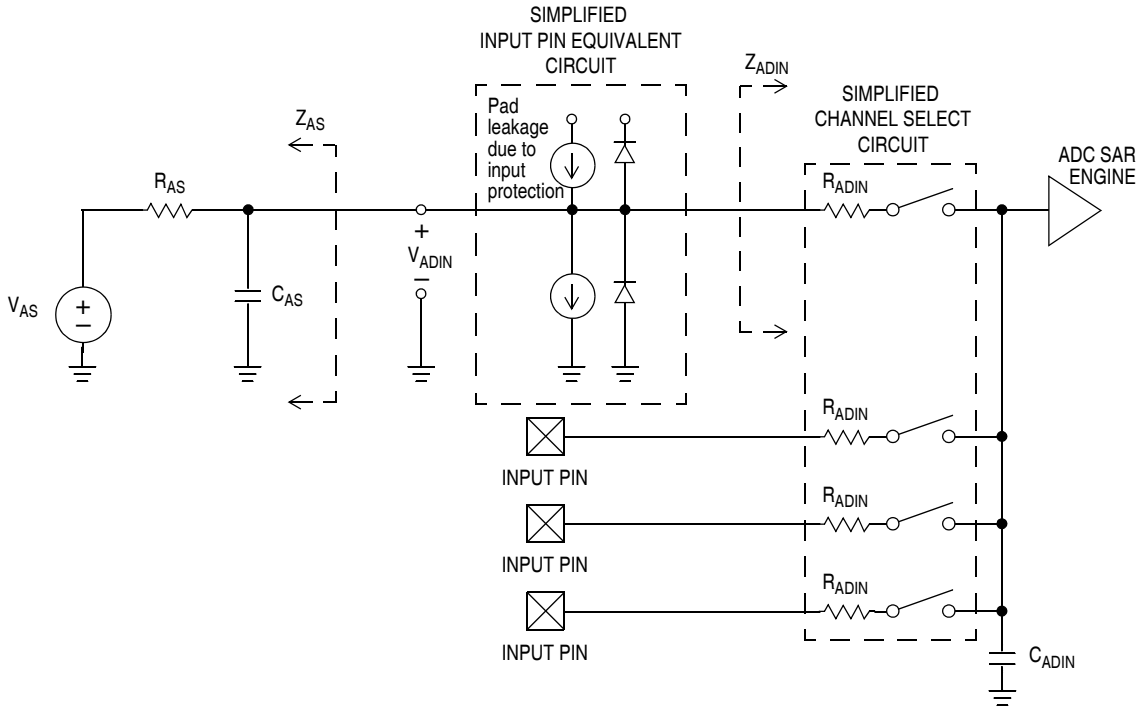

Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply current	ADLPC = 1 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	200	—	μA	
2	Supply current	ADLPC = 1 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	280	—	μA	
3	Supply current	ADLPC = 0 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	370	—	μA	
4	Supply current	ADLPC = 0 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	0.61	—	mA	
5	Supply current	Stop, reset, module off		I_{DDA}	—	0.01	0.8	μA	
6	ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low power (ADLPC = 1)			1.25	2	3.3		
7	Sample time	Single/first continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	6	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	10	—		
8	Sample time	Subsequent continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	4	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	8	—		

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
12	Integral non-linearity	12-bit mode	T	INL	—	–1.5 to 2.25	±2.75	LSB[2]	
		10-bit mode	T		—	±0.5	±1.0		
		8-bit mode	T		—	±0.3	±0.5		
13	Zero-scale error	12-bit mode	T	E_{ZS}	—	±1	–1.25 to 1	LSB[2]	V_{ADIN} = V_{SSA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
14	Full-scale error	12-bit mode	T	E_{FS}	—	±1.0	–3.5 to 2.25	LSB[2]	V_{ADIN} = V_{DDA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
15	Quantization error	12-bit mode	D	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode			—	—	±0.5		
		8-bit mode			—	—	±0.5		
16	Input leakage error	12-bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode			—	±0.2	±4		
		8-bit mode			—	±0.1	±1.2		
17	Temp sensor slope	–40 °C– 25 °C	D	m	—	1.646	—	mV/°C	
		25 °C– 125 °C			—	1.769	—		
18	Temp sensor voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes.

4 Based on input pad leakage current. Refer to pad electricals.

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