Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ll64clh

Freescale Semiconductor
Data Sheet Addendum

MC9S08LL64AD
Rev. 1, 08/2012

MC9S08LL64 Data Sheet Addendum

by: Automotive and Industrial Solutions Group

This document describes corrections to the *MC9S08LL64 Series Data Sheet*, order number MC9S08LL64. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MC9S08LL64 Series Data Sheet* is Revision 7.

Table of Contents

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC9S08LL64AD
Rev. 1
08/2012

1 Devices in the MC9S08LL64 Series

Table 1 summarizes the feature set available in the MC9S08LL64 series of MCUs.

Table 1. MC9S08LL64 Series Features by MCU and Package

Feature	MC9S08LL64		MC9S08LL36	
Package	**80-pin LQFP**	**64-pin LQFP**	**80-pin LQFP**	**64-pin LQFP**
FLASH	64 KB (32,768 and 32,768 Arrays)		36 KB (24,576 and 12,288 Arrays)	
RAM	4000		4000	
ACMP	yes		yes	
ADC	10-ch	8-ch	10-ch	8-ch
IIC	yes		yes	
IRQ	yes		yes	
KBI	8		8	
SCI1	yes		yes	
SCI2	yes		yes	
SPI	yes		yes	
TPM1	2-ch		2-ch	
TPM2	2-ch		2-ch	
TOD	yes		yes	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO1	yes	no	yes	no
VREFO2	no	yes	no	yes
I/O pins[1]	39	37	39	37

[1] The 39 I/O pins include two output-only pins and 18 LCD GPIO.

The block diagram in Figure 1 shows the structure of the MC9S08LL64 series MCU.

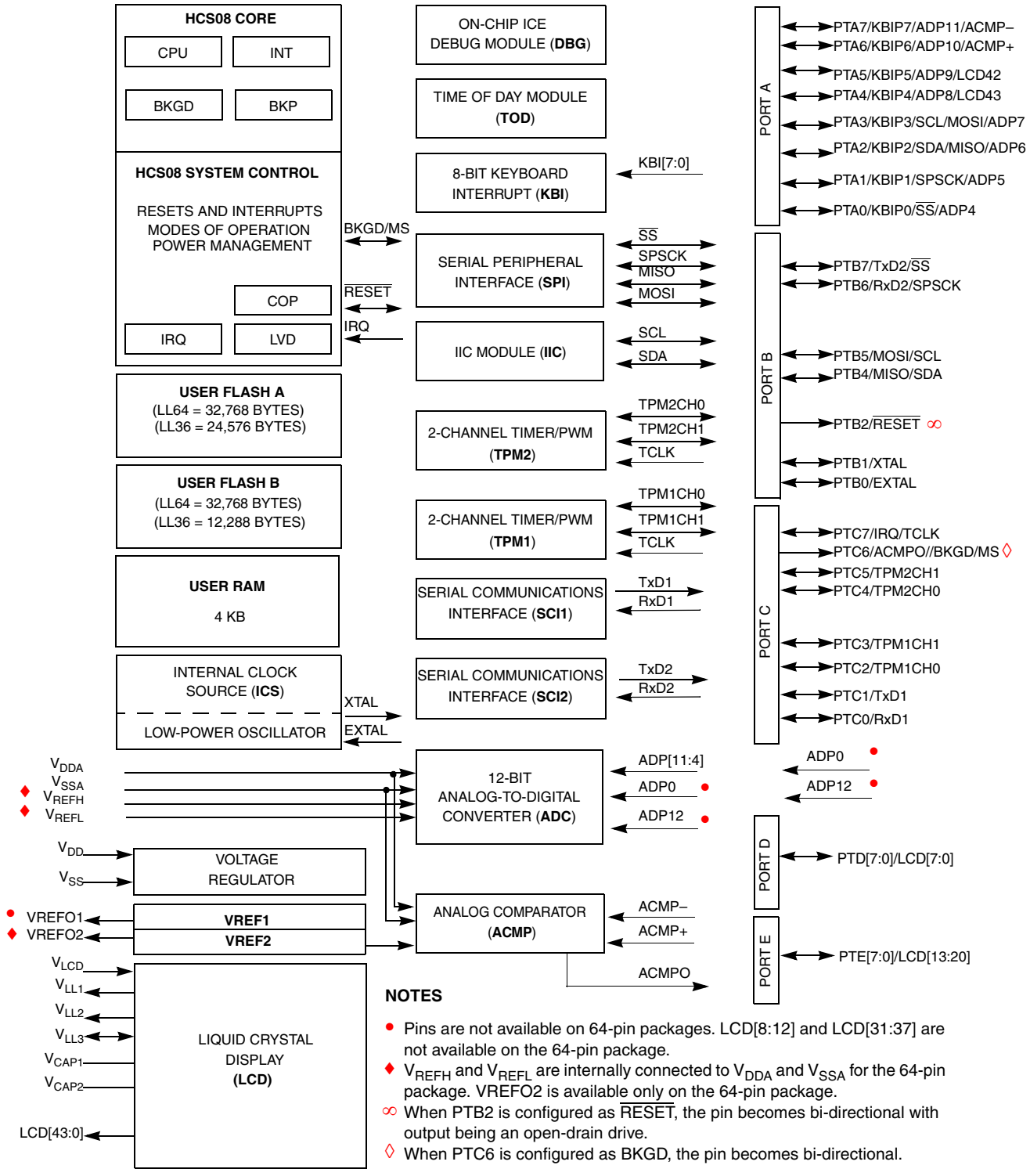


Figure 1. MC9S08LL64 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the This section shows the pin assignments for the MC9S08LL64 series devices.

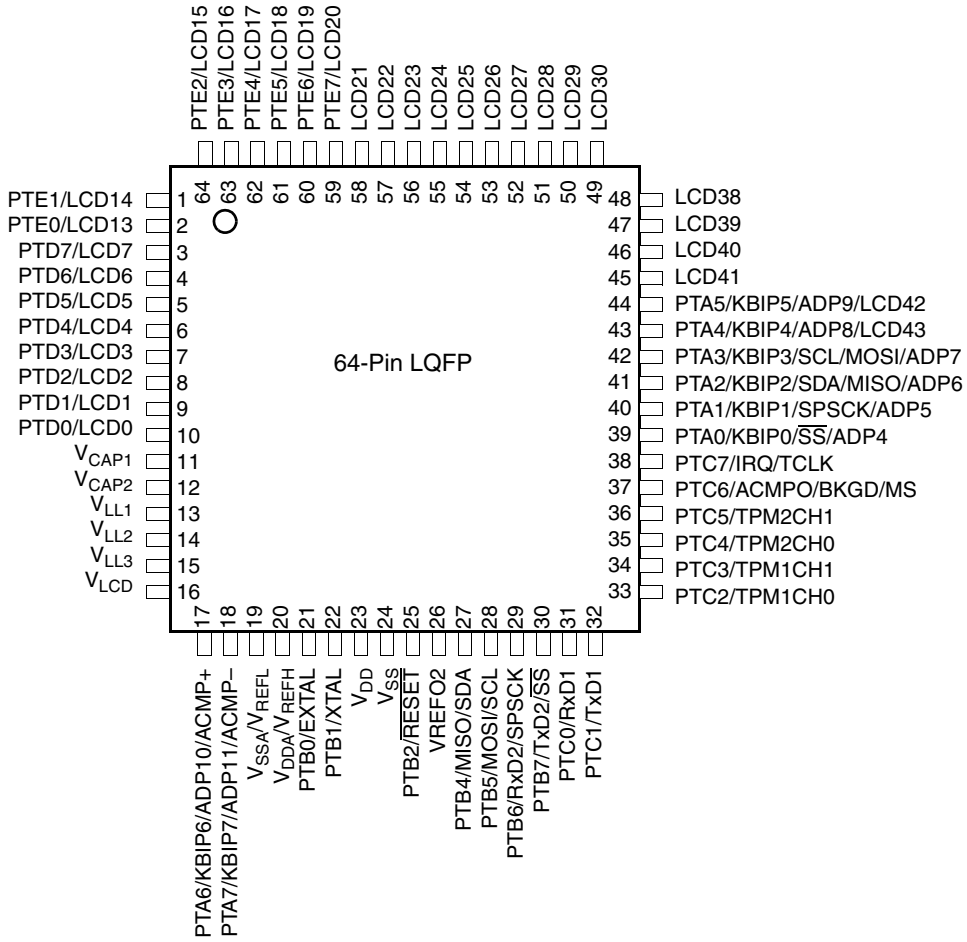


Figure 2. 64-Pin LQFP

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current — all input only pins except for LCD only pins (LCD 8-12, 21-41)	$\lvert I_{In} \rvert$	V_{In} = V_{DD}	—	0.025	1	µA
				V_{In} = V_{SS}	—	0.025	1	µA
		Input leakage current — LCD only pins (LCD 8-12, 21-41)		V_{In} = V_{DD}	—	100	150	µA
				V_{In} = V_{SS}	—	0.025	1	µA
12	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	µA
13	P	Total leakage current[3] — Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	3	µA
14	P	Pullup, Pulldown resistors — all non-LCD pins when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors — LCD/GPIO pins when enabled	R_{PU}, R_{PD}		35	—	77	kΩ
16	D	DC injection current[4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current[4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
18	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
19	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	2.0	V
20	D	POR re-arm time	t_{POR}		10	—	—	µs
21	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
22	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
23	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
24	P	Bandgap Voltage Reference[8]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 All I/O pins except for LCD pins in Open Drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

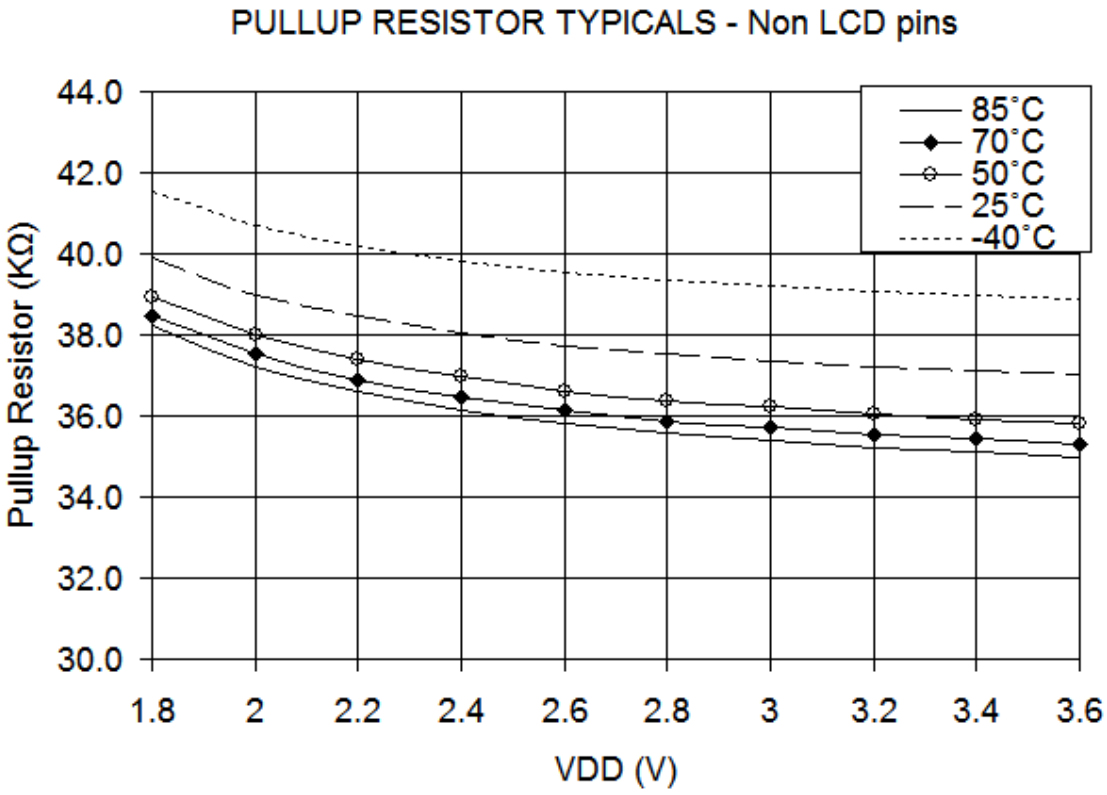


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

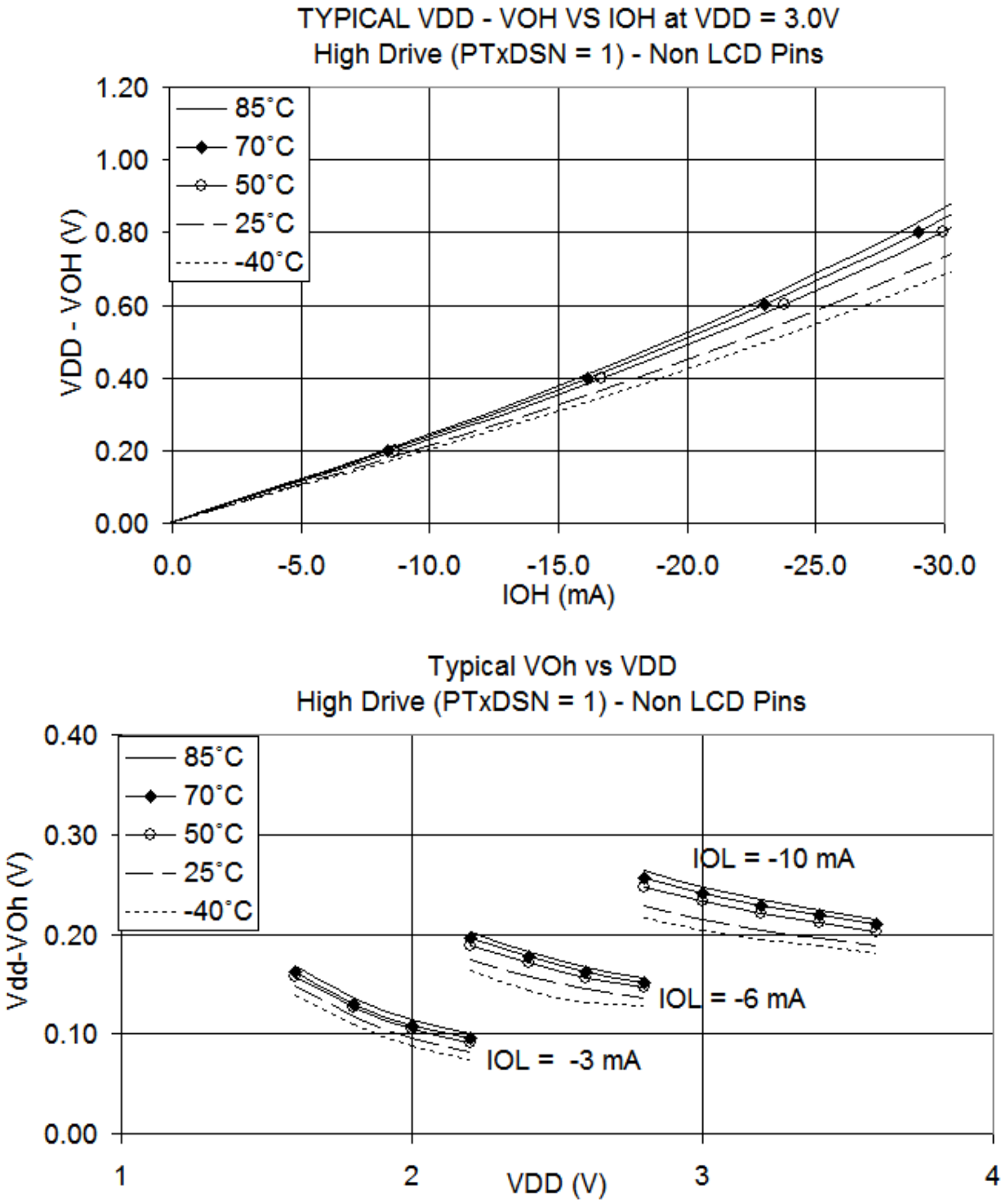


Figure 8. Typical High-Side (Source) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

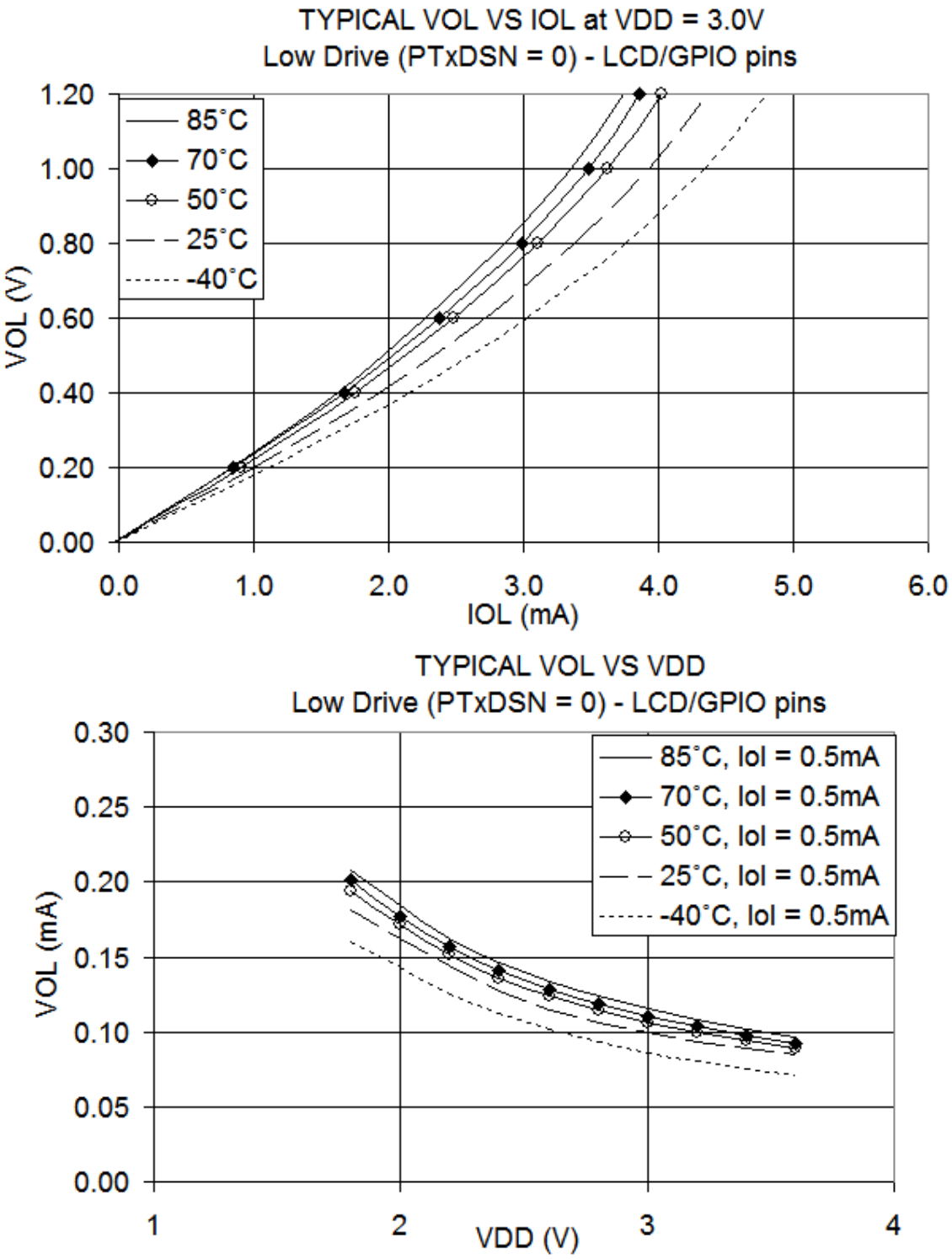


Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	T	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	13.75	17.9	mA	–40 to 85
	T			10 MHz		7	—		
	T			1 MHz		2	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	8.9	—	mA	–40 to 85
	T			10 MHz		5.5	—		
	T			1 MHz		0.9	—		
3	T	Run supply current LPS=0, all modules on	RI_{DD}	16 kHz FBILP	3	185	—	µA	–-40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	25	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	4.57	6	mA	–40 to 85
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.4	1.3	µA	–40 to 25
	C					4	6		70
	P					8.5	13		85
	C				2	0.35	1		–40 to 25
	C					3.9	5		70
	C					7.7	10		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.65	1.8	µA	–40 to 25
	C					5.7	8		70
	P					12.2	20		85
	C				2	0.6	1.5		–40 to 25
	C					5	6.8		70
	C					11.5	14		85

[1] Typical values are measured at 25 °C. Characterized, not tested

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				–40	25	70	85	
1	T	LPO		100	100	150	175	nA
2	T	EREFSTEN	RANGE = HGO = 0	750	750	800	850	nA
3	T	IREFSTEN[1]		63	70	77	81	µA
4	T	TOD	Does not include clock source current	50	50	75	100	nA
5	T	LVD[1]	LVDSE = 1	110	110	112	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	12	12	20	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	95	101	120	µA
8	T	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, No LCD glass connected.	1	1	6	13	µA
9	T	LCD	LCD configured for 1/8 duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, no LCD glass connected.	0.2	0.24	0.5	0.65	µA

1 Not available in stop2 mode.

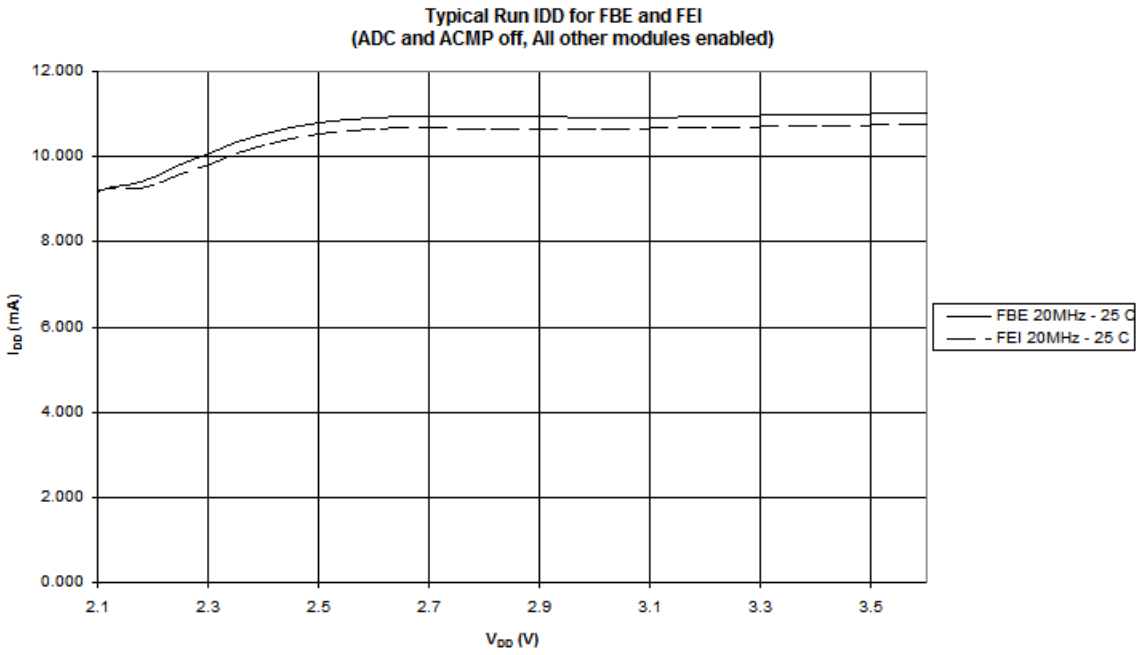


Figure 13. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ADC and ACMP off, All Other Modules Enabled)

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	± 0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

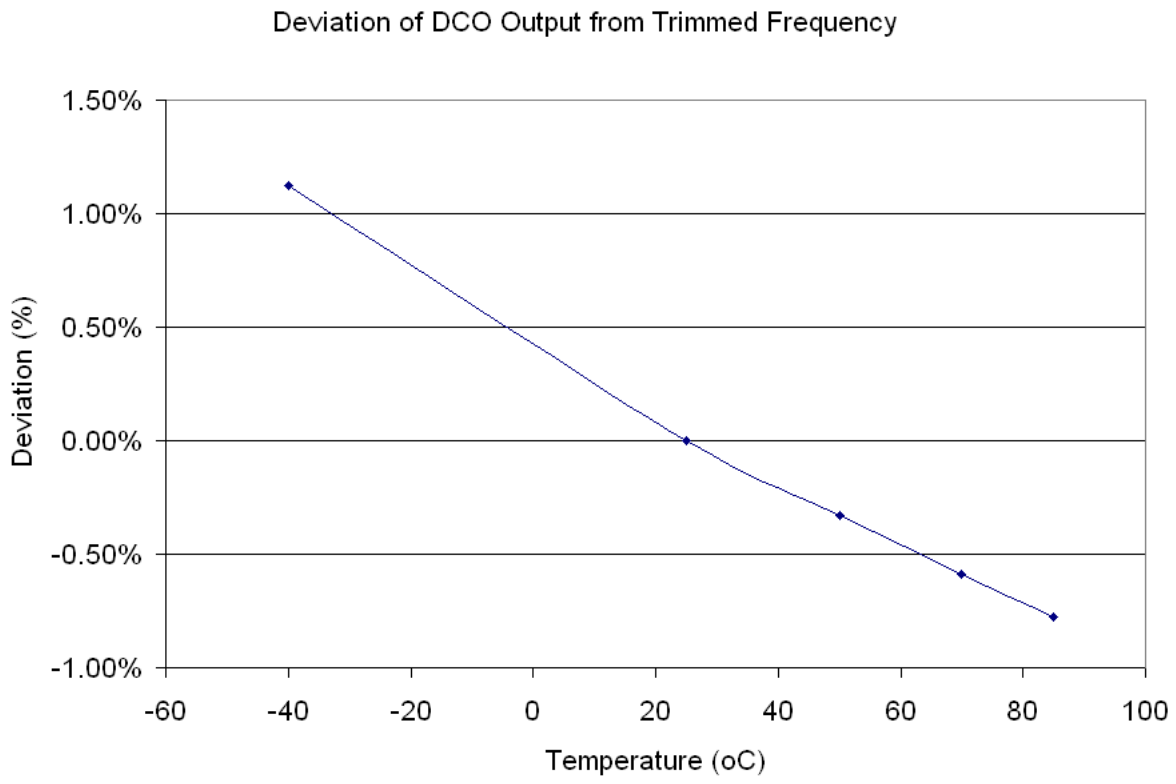


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \leq 2.1V$ $V_{DD} > 2.1V$	f_{Bus}	 dc dc	 — —	 10 20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

6 Except for LCD pins in open drain mode.

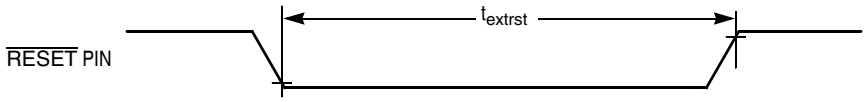


Figure 17. Reset Timing

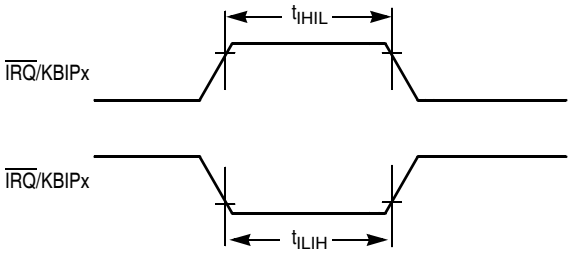


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

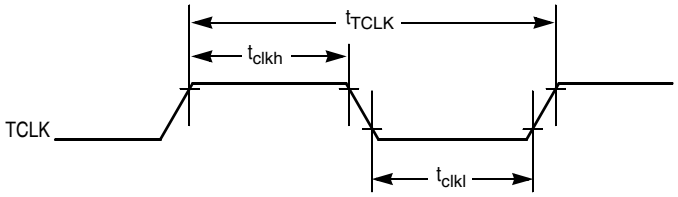
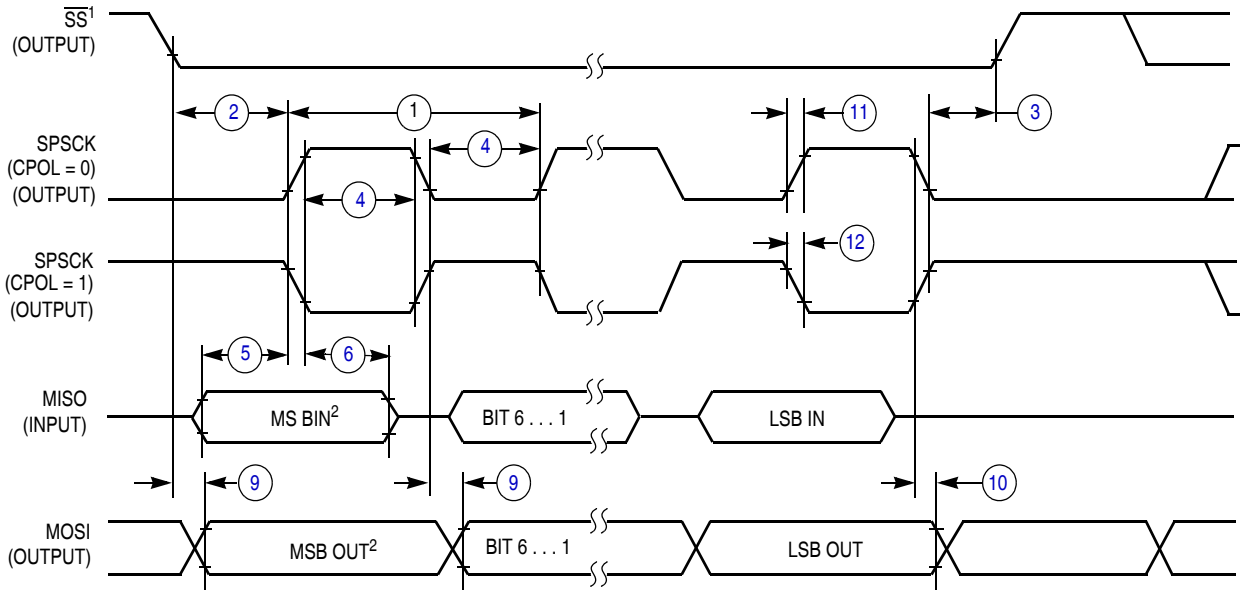


Figure 19. Timer External Clock

Table 15. SPI Timing (continued)

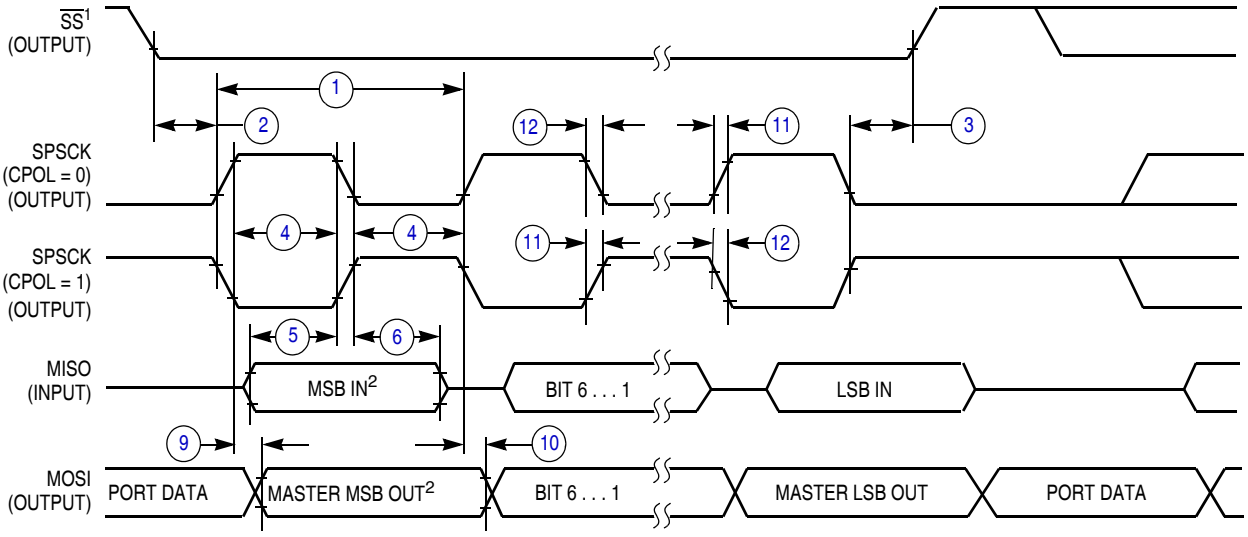
No.	C	Function	Symbol	Min	Max	Unit
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 t_{cyc} – 25 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 t_{cyc} – 25 25	 ns ns



NOTES:

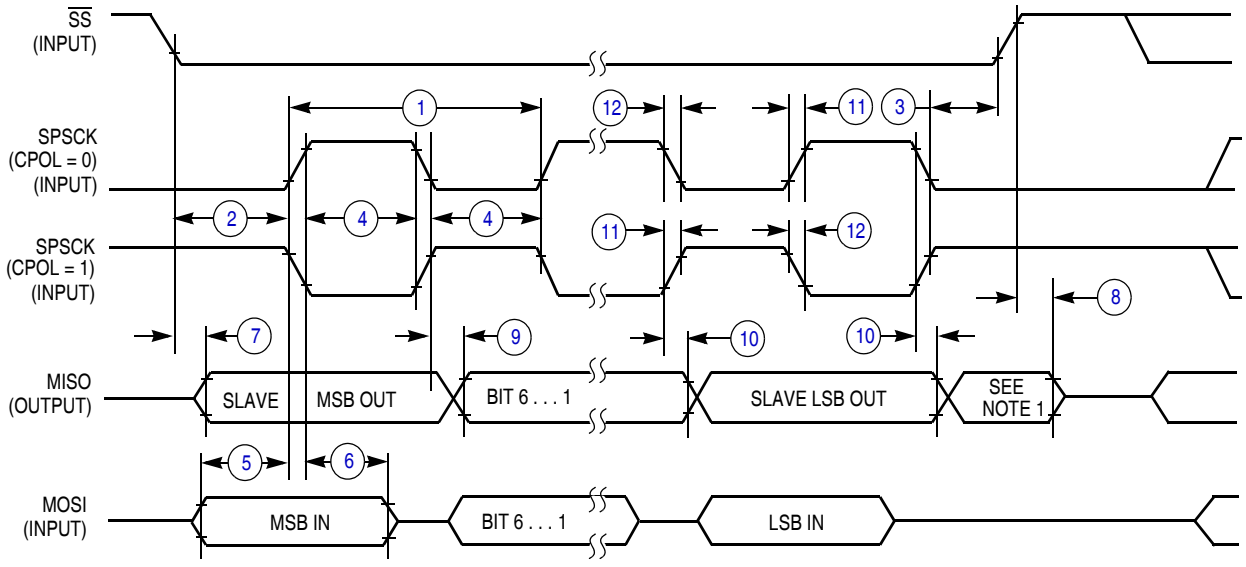
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)



NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 0)

Table 17. 12-Bit ADC Operating Conditions (continued)

No.	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
2	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV
3	Reference voltage high	—	V_{REFH}	1.8	V_{DDA}	V_{DDA}	V
4	Reference voltage low	—	V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V
5	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
6	Input capacitance	8/10/12-bit modes	C_{ADIN}	—	4	5	pF
7	Input resistance	—	R_{ADIN}	—	5	7	kΩ

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

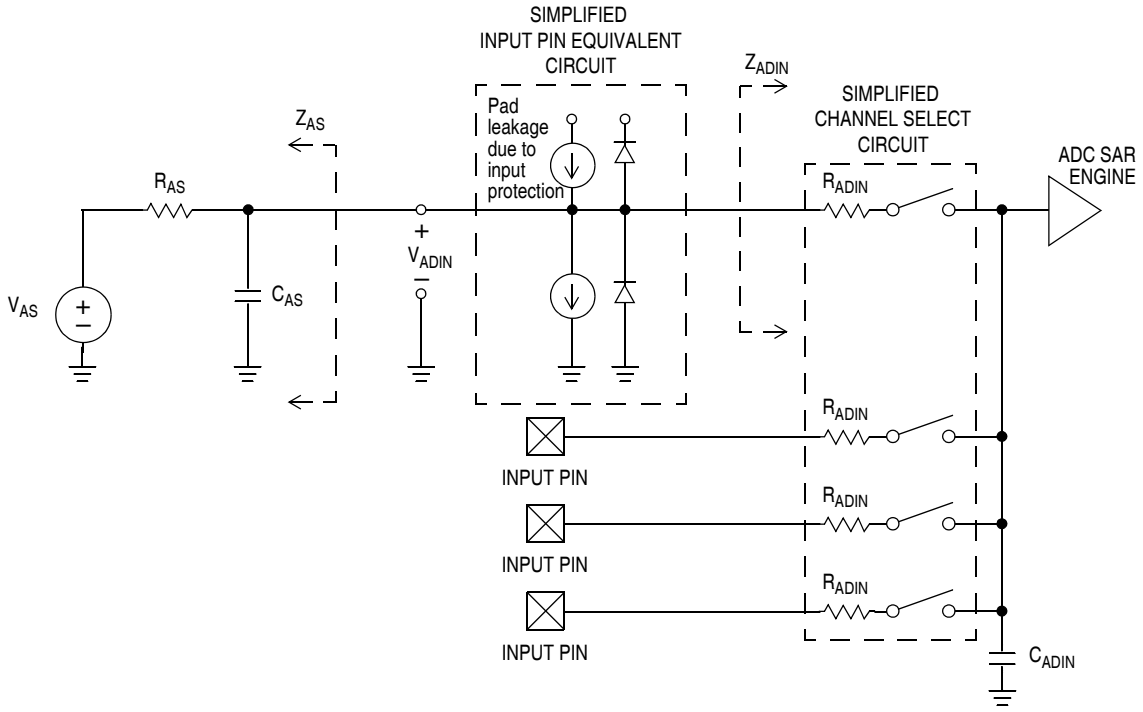


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply current	ADLPC = 1 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	200	—	μA	
2	Supply current	ADLPC = 1 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	280	—	μA	
3	Supply current	ADLPC = 0 ADHSC = 0 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	370	—	μA	
4	Supply current	ADLPC = 0 ADHSC = 1 ADLSMP = 0 ADCO = 1	T	I_{DDA}	—	0.61	—	mA	
5	Supply current	Stop, reset, module off		I_{DDA}	—	0.01	0.8	μA	
6	ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low power (ADLPC = 1)			1.25	2	3.3		
7	Sample time	Single/first continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	6	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	10	—		
8	Sample time	Subsequent continuous ADLSMP = 0							
		ADHSC = 0 ADLSMP = 0 ADLSTS = XX	C	ts	—	4	—	ADCK	
		ADHSC = 1 ADLSMP = 0 ADLSTS = XX	C	ts	—	8	—		

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
12	Integral non-linearity	12-bit mode	T	INL	—	–1.5 to 2.25	±2.75	LSB[2]	
		10-bit mode	T		—	±0.5	±1.0		
		8-bit mode	T		—	±0.3	±0.5		
13	Zero-scale error	12-bit mode	T	E_{ZS}	—	±1	–1.25 to 1	LSB[2]	V_{ADIN} = V_{SSA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
14	Full-scale error	12-bit mode	T	E_{FS}	—	±1.0	–3.5 to 2.25	LSB[2]	V_{ADIN} = V_{DDA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
15	Quantization error	12-bit mode	D	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode			—	—	±0.5		
		8-bit mode			—	—	±0.5		
16	Input leakage error	12-bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode			—	±0.2	±4		
		8-bit mode			—	±0.1	±1.2		
17	Temp sensor slope	–40 °C– 25 °C	D	m	—	1.646	—	mV/°C	
		25 °C– 125 °C			—	1.769	—		
18	Temp sensor voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes.

4 Based on input pad leakage current. Refer to pad electricals.