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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ll64clk

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MC9S08LL64AD
Rev. 1
08/2012

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
7	3	PTD7	LCD7			
8	4	PTD6	LCD6			
9	5	PTD5	LCD5			
10	6	PTD4	LCD4			
11	7	PTD3	LCD3			
12	8	PTD2	LCD2			
13	9	PTD1	LCD1			
14	10	PTD0	LCD0			
15	11	V_{CAP1}				
16	12	V_{CAP2}				
17	13	V_{LL1}				
18	14	V_{LL2}				
19	15	V_{LL3}				
20	16	V_{LCD}				
21	17	PTA6	KBIP6	ADP10	ACMP+	
22	18	PTA7	KBIP7	ADP11	ACMP–	
23	19	V_{SSA}				
24		V_{REFL}				
25		ADP0				
26		ADP12				
27		VREFO1				
28	20	V_{REFH}				
29		V_{DDA}				
30	21	PTB0		EXTAL		
31	22	PTB1		XTAL		
32	23	V_{DD}				
33	24	V_{SS}				
34	25	PTB2	$\overline{\text{RESET}}$			
	26	VREFO2				
35	27	PTB4	MISO	SDA		
36	28	PTB5	MOSI	SCL		
37	29	PTB6	RxD2	SPSCK		
38	30	PTB7	TxD2	$\overline{\text{SS}}$		
39	31	PTC0	RxD1			
40	32	PTC1	TxD1			
41	33	PTC2	TPM1CH0			
42	34	PTC3	TPM1CH1			
43	35	PTC4	TPM2CH0			

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current — all input only pins except for LCD only pins (LCD 8-12, 21-41)	$\lvert I_{In} \rvert$	V_{In} = V_{DD}	—	0.025	1	µA
				V_{In} = V_{SS}	—	0.025	1	µA
		Input leakage current — LCD only pins (LCD 8-12, 21-41)		V_{In} = V_{DD}	—	100	150	µA
				V_{In} = V_{SS}	—	0.025	1	µA
12	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	µA
13	P	Total leakage current[3] — Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	3	µA
14	P	Pullup, Pulldown resistors — all non-LCD pins when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors — LCD/GPIO pins when enabled	R_{PU}, R_{PD}		35	—	77	kΩ
16	D	DC injection current[4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current[4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
18	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
19	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	2.0	V
20	D	POR re-arm time	t_{POR}		10	—	—	µs
21	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
22	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
23	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
24	P	Bandgap Voltage Reference[8]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 All I/O pins except for LCD pins in Open Drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

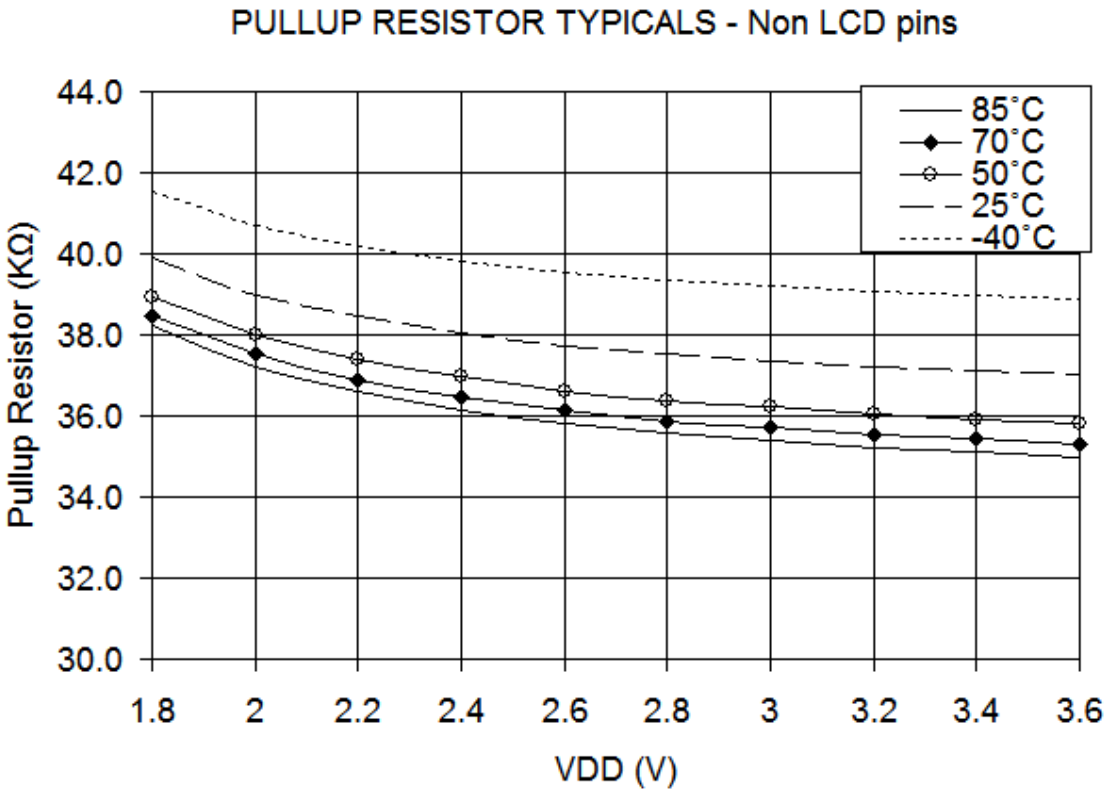


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

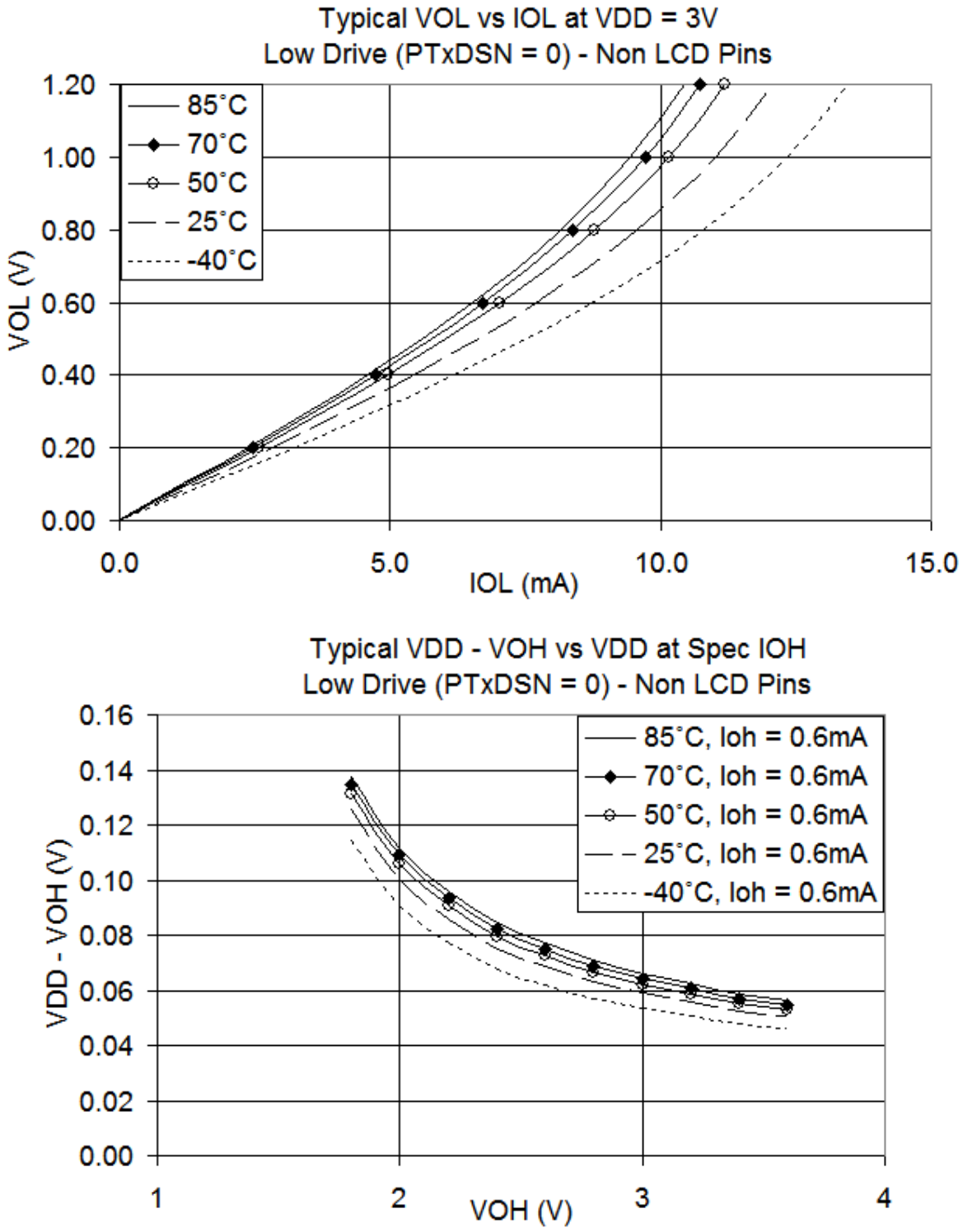


Figure 7. Typical High-Side (Source) Characteristics (Non LCD Pins)— Low Drive (PTxDSn = 0)

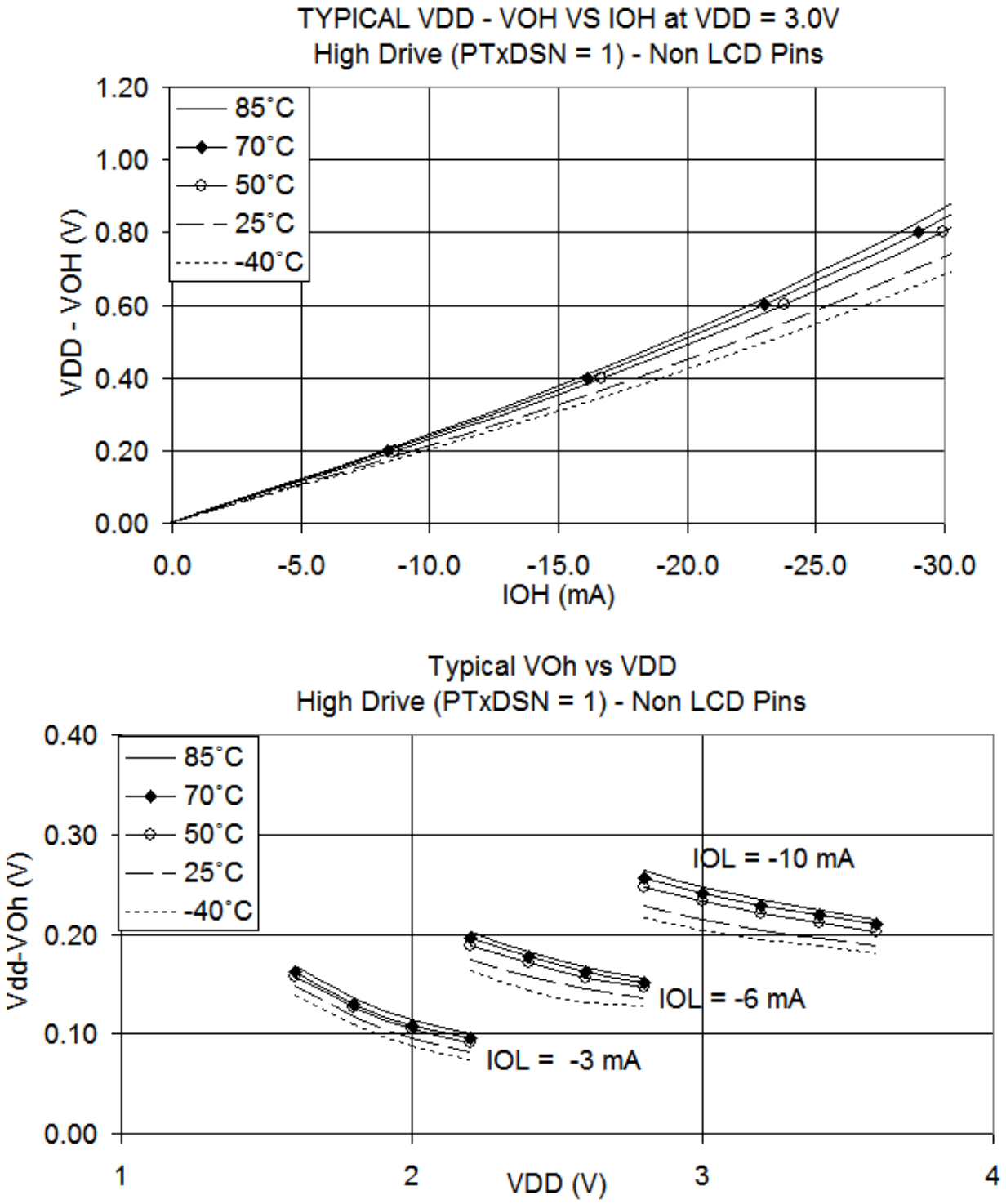


Figure 8. Typical High-Side (Source) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

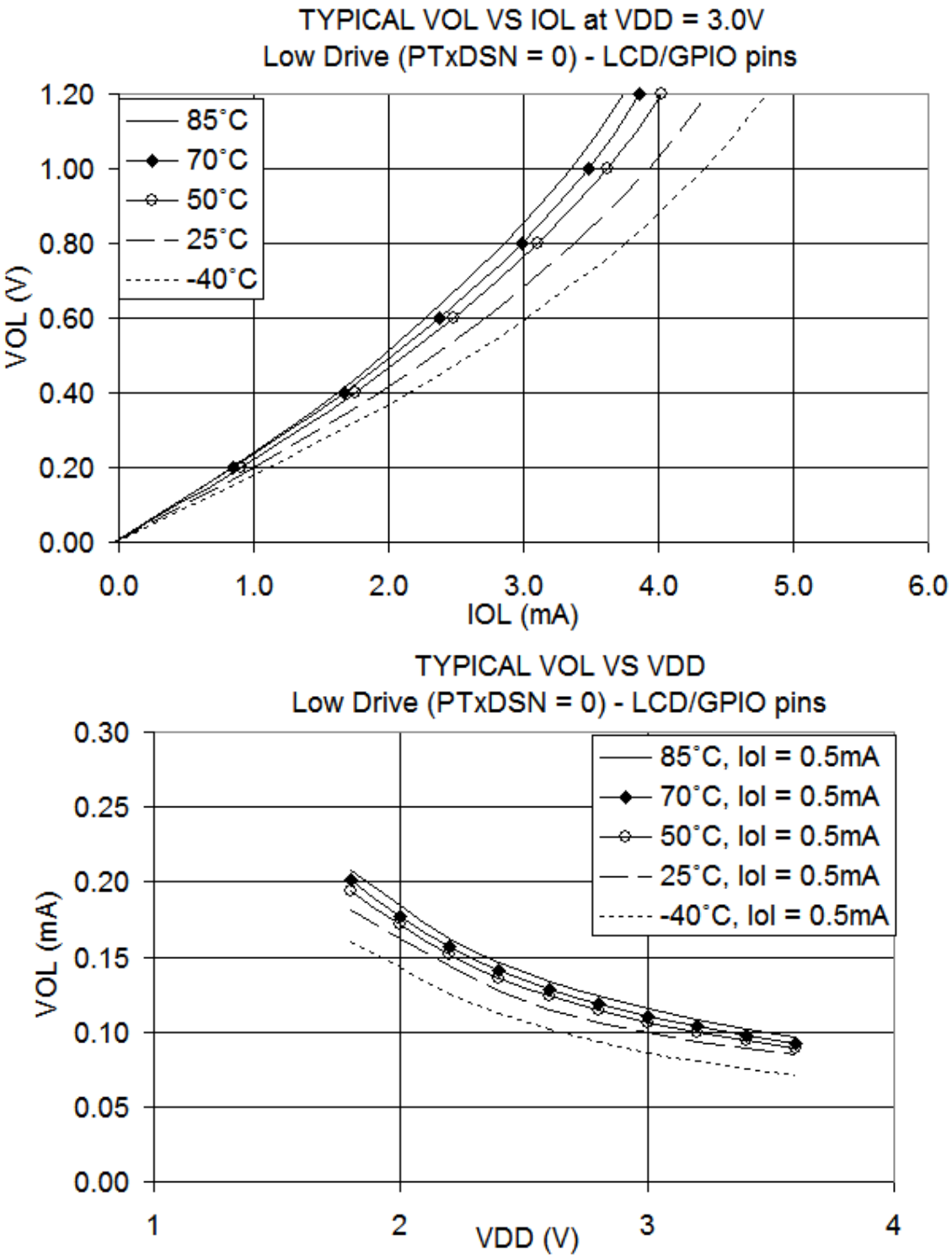


Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

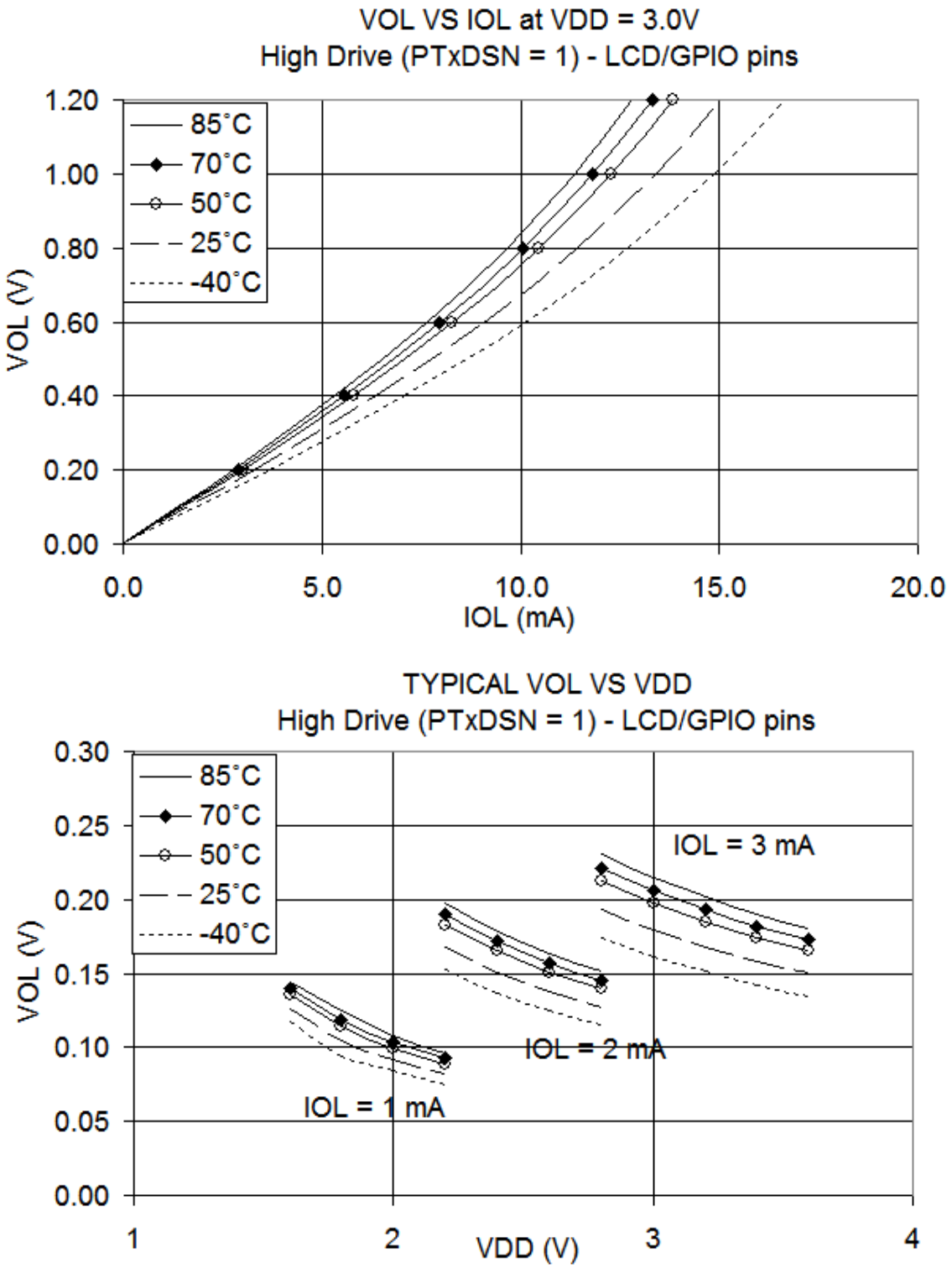


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

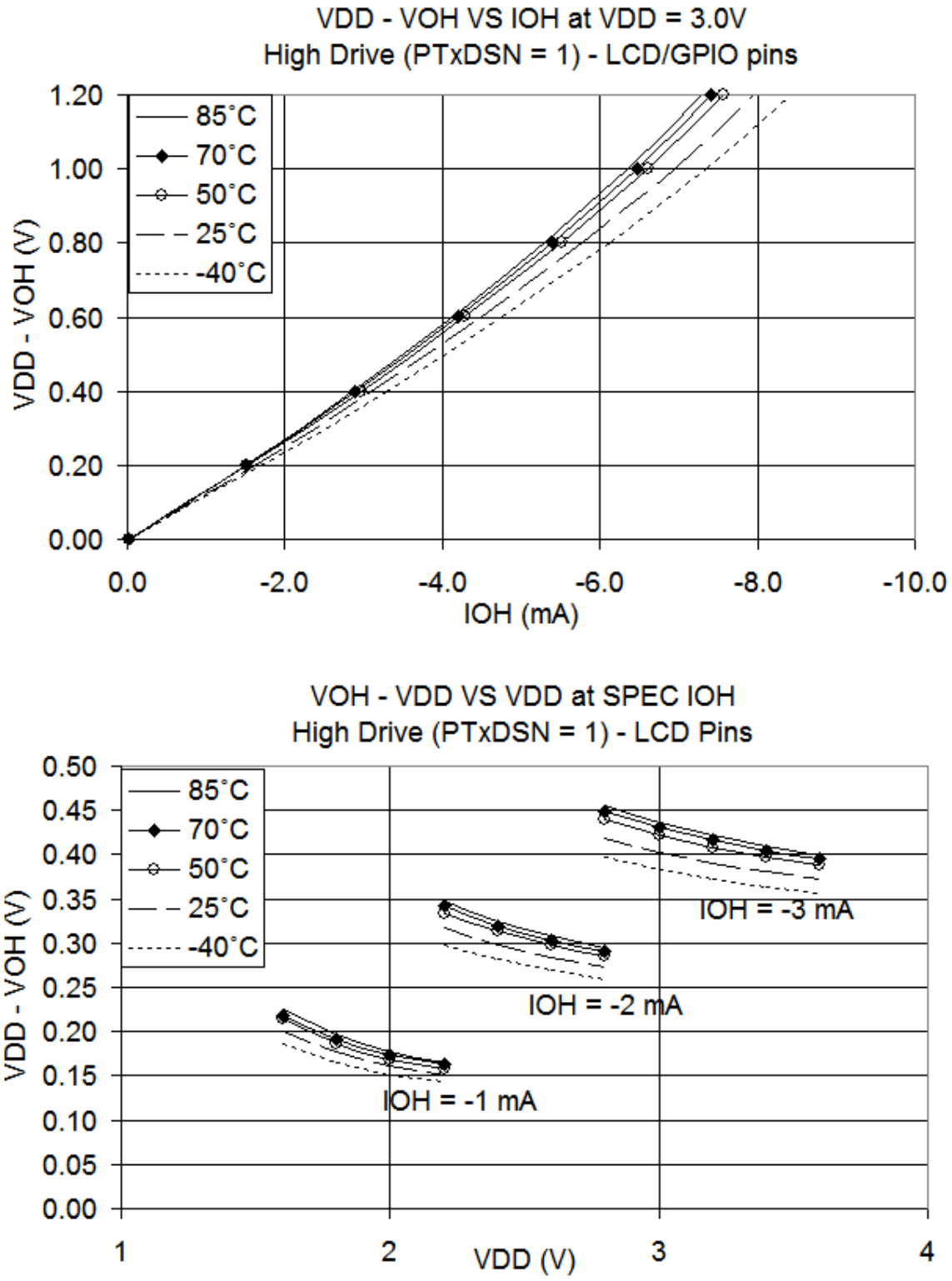


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	T	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	13.75	17.9	mA	–40 to 85
	T			10 MHz		7	—		
	T			1 MHz		2	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	8.9	—	mA	–40 to 85
	T			10 MHz		5.5	—		
	T			1 MHz		0.9	—		
3	T	Run supply current LPS=0, all modules on	RI_{DD}	16 kHz FBILP	3	185	—	µA	–-40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	25	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	4.57	6	mA	–40 to 85
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.4	1.3	µA	–40 to 25
	C					4	6		70
	P					8.5	13		85
	C				2	0.35	1		–40 to 25
	C					3.9	5		70
	C					7.7	10		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.65	1.8	µA	–40 to 25
	C					5.7	8		70
	P					12.2	20		85
	C				2	0.6	1.5		–40 to 25
	C					5	6.8		70
	C					11.5	14		85

[1] Typical values are measured at 25 °C. Characterized, not tested

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

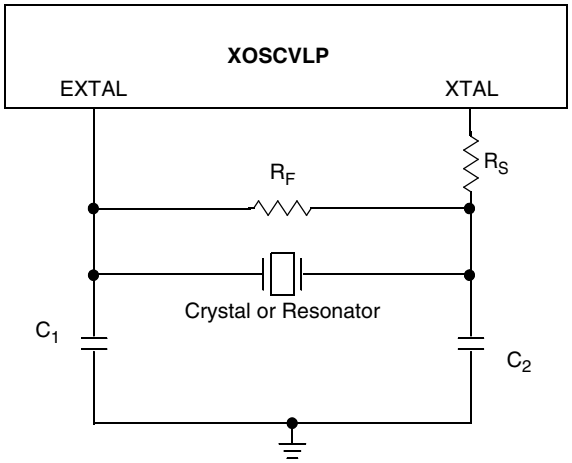


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

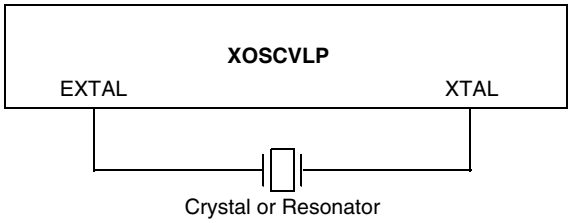


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed		f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — user-trimmed		f_{int_t}	31.25	—	39.06	kHz
3	P	Average internal reference frequency — factory-trimmed		f_{int_t}	—	32.7	—	kHz
4	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
5	P	DCO output frequency range — untrimmed	Low range (DFR = 00)	f_{dco_ut}	12.8	16.8	21.33	MHz
	C		Mid range (DFR = 01)		25.6	33.6	42.67	
6	P	DCO output frequency range — trimmed	Low range (DFR = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	±0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	± 0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

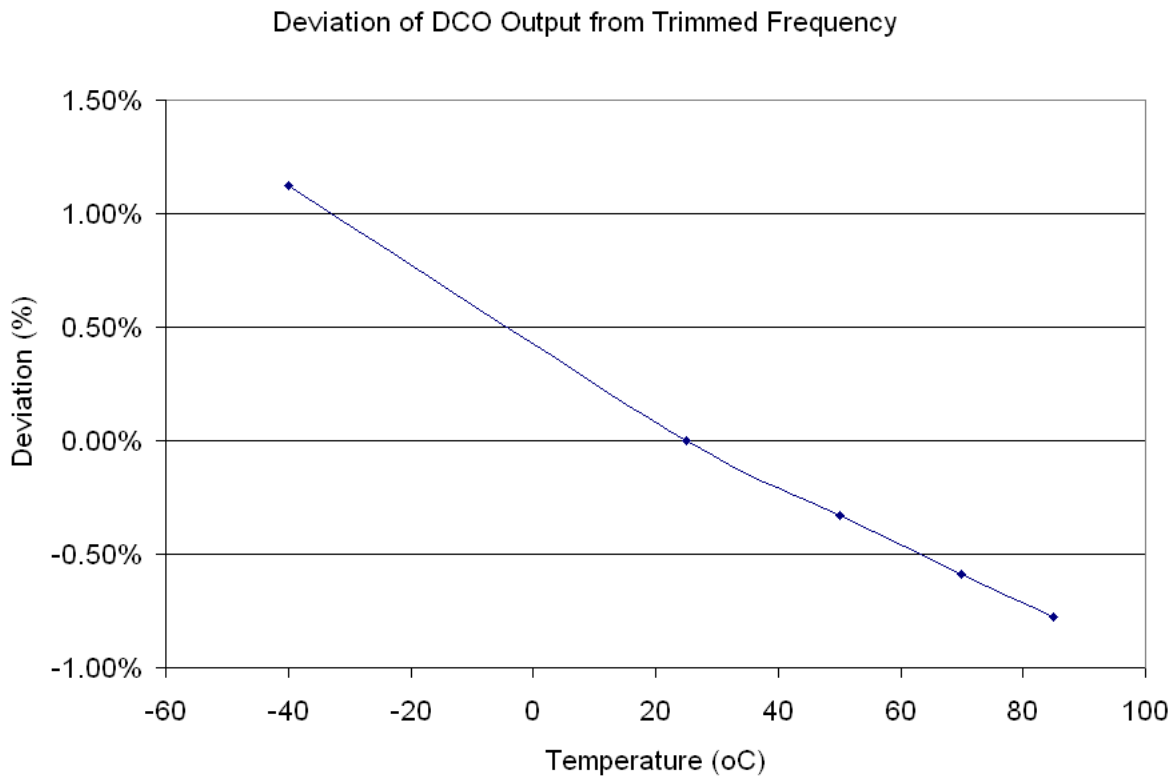


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

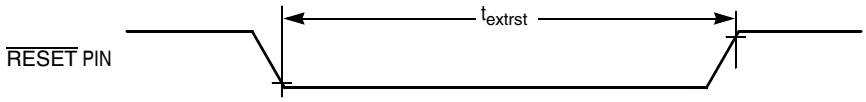


Figure 17. Reset Timing

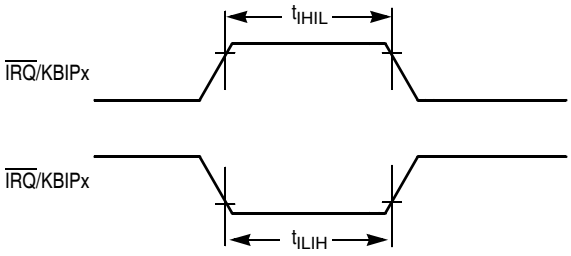


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

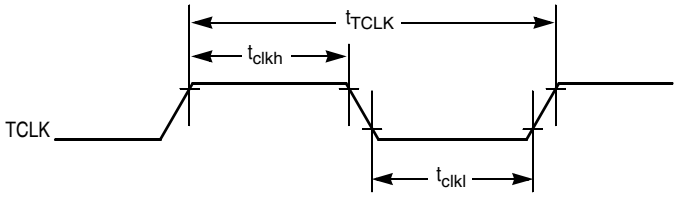
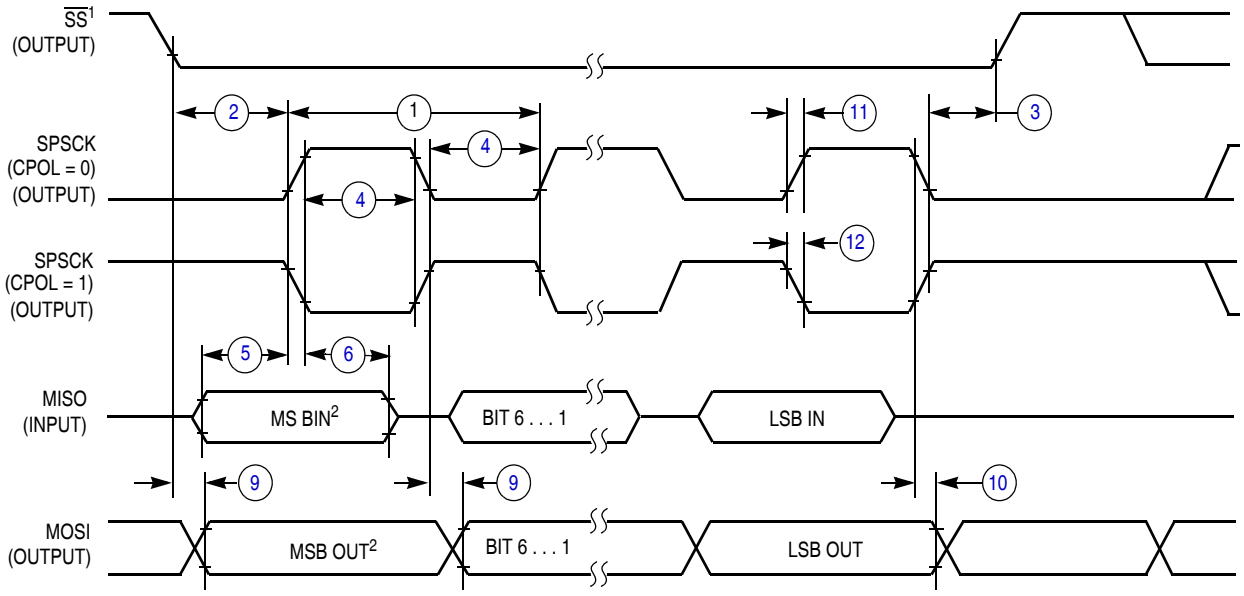


Figure 19. Timer External Clock

Table 15. SPI Timing (continued)

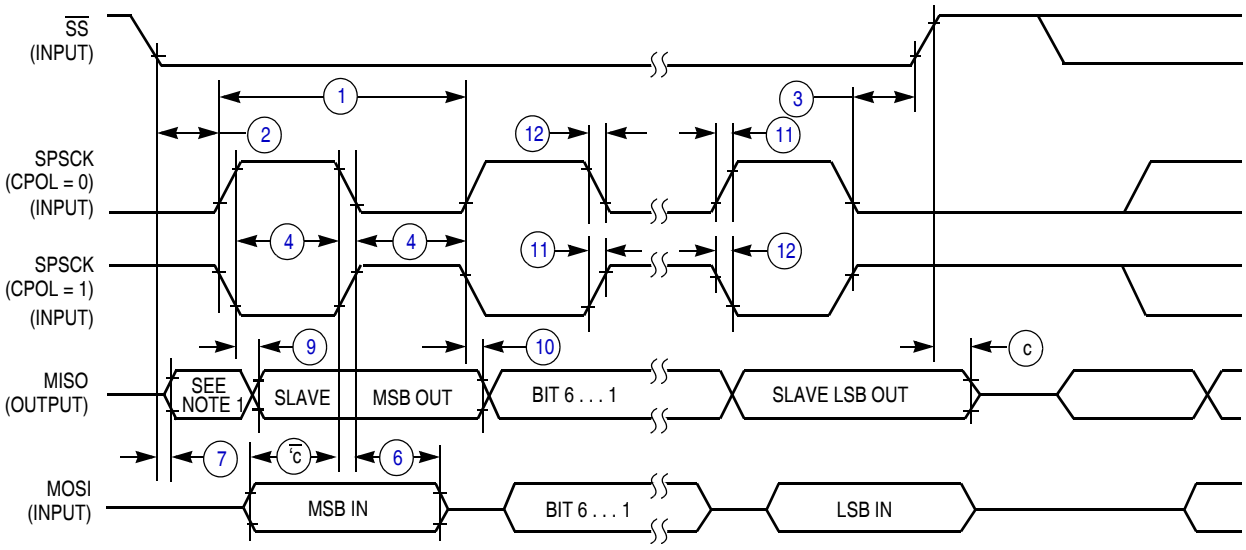
No.	C	Function	Symbol	Min	Max	Unit
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 t_{cyc} – 25 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 t_{cyc} – 25 25	 ns ns



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

No	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.8	—	3.6	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	P	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
6	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
7	C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 12-Bit ADC Operating Conditions

No.	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V
		Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
9	Sample time	Subsequent Continuous or Single/First Continuous ADLSMP = 1							
		ADHSC = 0 ADLSMP = 1 ADLSTS = 00	C	ts	—	24	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 01	C	ts	—	16	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 10	C	ts	—	10	—		
		ADHSC = 0 ADLSMP = 1 ADLSTS = 11	C	ts	—	6	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 00	C	ts	—	28	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 01	C	ts	—	20	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 10	C	ts	—	14	—		
		ADHSC = 1 ADLSMP = 1 ADLSTS = 11	C	ts	—	10	—		
10	Total unadjusted error	12-bit mode $3.6 > V_{DDA} > 2.7V$	T	E_{TUE}	—	–2.5 to 3.25	±4	LSB[2]	Includes quantization
		12-bit mode, $2.7 > V_{DDA} > 1.8V$	T			±3.25	–5.5 to 6.5		
		10-bit mode	T		—	±1	±2.5		
		8-bit mode	T		—	±0.5	±1.0		
11	Differential non-linearity	12-bit mode	T	DNL	—	–1 to 1.75	–1.5 to 2.5	LSB[2]	
		10-bit mode[3]	T		—	±0.5	±1.0		
		8-bit mode[3]	T		—	±0.3	±0.5		

Table 18. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
12	Integral non-linearity	12-bit mode	T	INL	—	–1.5 to 2.25	±2.75	LSB[2]	
		10-bit mode	T		—	±0.5	±1.0		
		8-bit mode	T		—	±0.3	±0.5		
13	Zero-scale error	12-bit mode	T	E_{ZS}	—	±1	–1.25 to 1	LSB[2]	V_{ADIN} = V_{SSA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
14	Full-scale error	12-bit mode	T	E_{FS}	—	±1.0	–3.5 to 2.25	LSB[2]	V_{ADIN} = V_{DDA}
		10-bit mode	T		—	±0.5	±1		
		8-bit mode	T		—	±0.5	±0.5		
15	Quantization error	12-bit mode	D	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode			—	—	±0.5		
		8-bit mode			—	—	±0.5		
16	Input leakage error	12-bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode			—	±0.2	±4		
		8-bit mode			—	±0.1	±1.2		
17	Temp sensor slope	–40 °C– 25 °C	D	m	—	1.646	—	mV/°C	
		25 °C– 125 °C			—	1.769	—		
18	Temp sensor voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes.

4 Based on input pad leakage current. Refer to pad electricals.

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