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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 20 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | 20 |
| Number of Macrocells | 320 |
| Number of Gates | 6000 |
| Number of I/O | 60 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm9320li84-20 |

## ...and More Features

- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

**Table 2. MAX 9000 Package Options & I/O Counts** *Note (1)*

| Device | 84-Pin PLCC | 208-Pin RQFP | 240-Pin RQFP | 280-Pin PGA | 304-Pin RQFP | 356-Pin BGA |
|---|---|---|---|---|---|---|
| EPM9320 | 60 *(2)* | 132 | – | 168 | – | 168 |
| EPM9320A | 60 *(2)* | 132 | – | – | – | 168 |
| EPM9400 | 59 *(2)* | 139 | 159 | – | – | – |
| EPM9480 | – | 146 | 175 | – | – | – |
| EPM9560 | – | 153 | 191 | 216 | 216 | 216 |
| EPM9560A | – | 153 | 191 | – | – | 216 |

***Notes:***

(1) MAX 9000 device package types include plastic J-lead chip carrier (PLCC), power quad flat pack (RQFP), ceramic pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.

## General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the ***PCI Local Bus Specification, Revision 2.2***. Table 3 shows the speed grades available for MAX 9000 devices.

**Table 3. MAX 9000 Speed Grade Availability**

| Device | Speed Grade | | |
|---|---|---|---|
| | -10 | -15 | -20 |
| EPM9320 | | ✓ | ✓ |
| EPM9320A | ✓ | | |
| EPM9400 | | ✓ | ✓ |
| EPM9480 | | ✓ | ✓ |
| EPM9560 | | ✓ | ✓ |
| EPM9560A | ✓ | | |

Table 4 shows the performance of MAX 9000 devices for typical functions.

**Table 4. MAX 9000 Performance** *Note (1)*

| Application | Macrocells Used | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -10 | -15 | -20 | |
| 16-bit loadable counter | 16 | 144 | 118 | 100 | MHz |
| 16-bit up/down counter | 16 | 144 | 118 | 100 | MHz |
| 16-bit prescaled counter | 16 | 144 | 118 | 100 | MHz |
| 16-bit address decode | 1 | 5.6 (10) | 7.9 (15) | 10 (20) | ns |
| 16-to-1 multiplexer | 1 | 7.7 (12.1) | 10.9 (18) | 16 (26) | ns |

***Note:***

(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 devices offer the MultiVolt feature, which allows output drivers to be set for either 3.3-V or 5.0-V operation in mixed-voltage systems.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

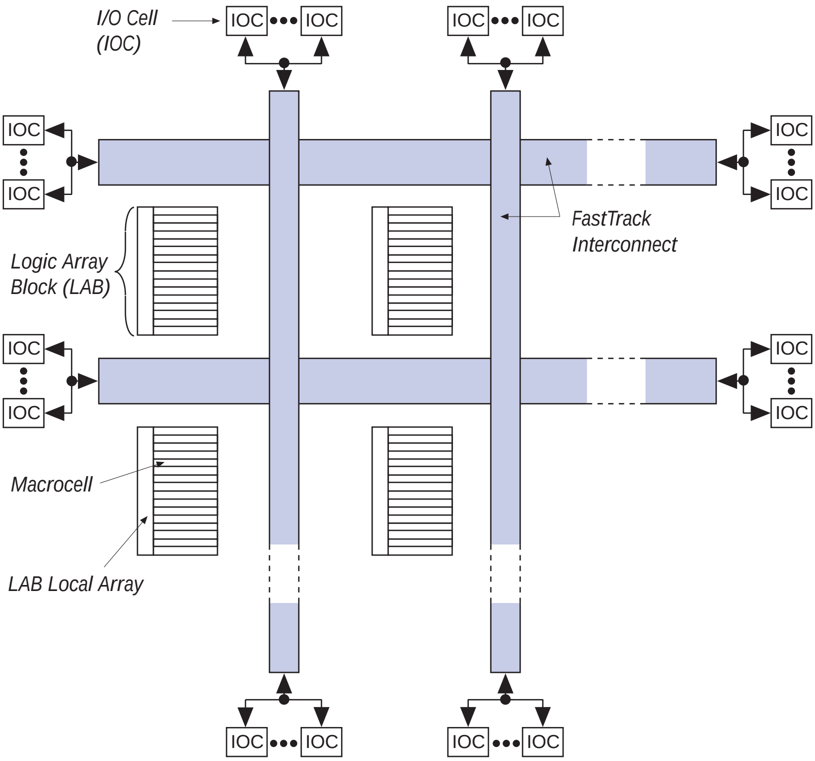
## Functional Description

MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

***Figure 1. MAX 9000 Device Block Diagram***




## Logic Array Blocks

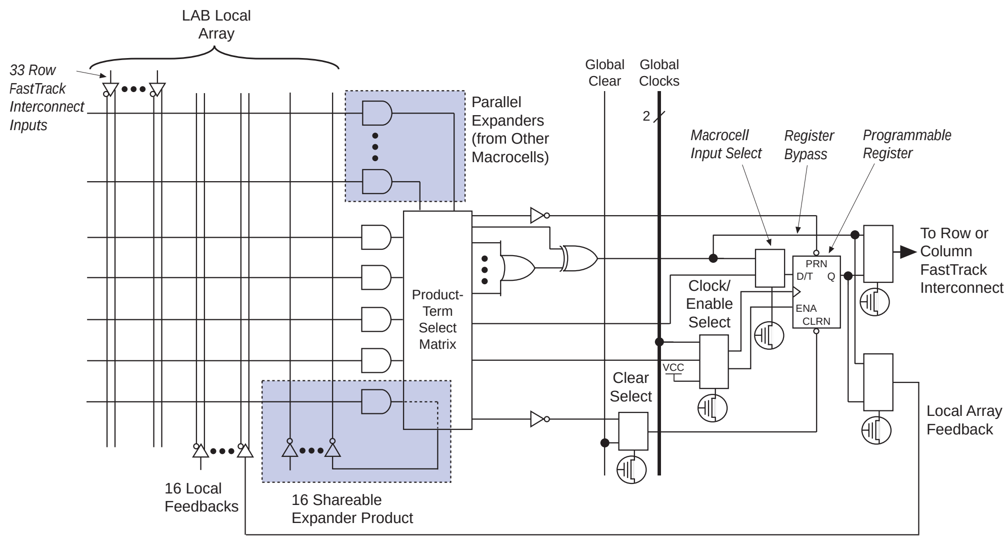
The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2 on page 7. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

## Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

*Figure 3. MAX 9000 Macrocell & Local Array*




Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay ($t_{OD}$) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis. The slew rate control affects both rising and falling edges of the output signals.

*Table 6. Peripheral Bus Sources*

| Peripheral Control Signal | Source | | | |
|---|---|---|---|---|
| | EPM9320 EPM9320A | EPM9400 | EPM9480 | EPM9560 EPM9560A |
| OE0/ENA0 | Row C | Row E | Row F | Row G |
| OE1/ENA1 | Row B | Row E | Row F | Row F |
| OE2/ENA2 | Row A | Row E | Row E | Row E |
| OE3/ENA3 | Row B | Row B | Row B | Row B |
| OE4/ENA4 | Row A | Row A | Row A | Row A |
| OE5 | Row D | Row D | Row D | Row D |
| OE6 | Row C | Row C | Row C | Row C |
| OE7/CLR1 | Row B/GOE | Row B/GOE | Row B/GOE | Row B/GOE |
| CLR0/ENA5 | Row A/GCLR | Row A/GCLR | Row A/GCLR | Row A/GCLR |
| CLK0 | GCLK1 | GCLK1 | GCLK1 | GCLK1 |
| CLK1 | GCLK2 | GCLK2 | GCLK2 | GCLK2 |
| CLK2 | Row D | Row D | Row D | Row D |
| CLK3 | Row C | Row C | Row C | Row C |

## Output Configuration

The MAX 9000 device architecture supports the MultiVolt I/O interface feature, which allows MAX 9000 devices to interface with systems of differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$.

## In-System Programmability (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an “F” suffix in the ordering code.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 9000 device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 9000 Device*

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
$f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The programming times described in Tables 7 through 9 are associated with the worst-case method using the ISP algorithm.

**Table 7. MAX 9000 $t_{PULSE}$ & $Cycle_{TCK}$ Values**

| Device | Programming | | Stand-Alone Verification | |
|---|---|---|---|---|
| | $t_{PPULSE}$ (s) | $Cycle_{PTCK}$ | $t_{VPULSE}$ (s) | $Cycle_{VTCK}$ |
| EPM9320<br>EPM9320A | 11.79 | 2,966,000 | 0.15 | 1,806,000 |
| EPM9400 | 12.00 | 3,365,000 | 0.15 | 2,090,000 |
| EPM9480 | 12.21 | 3,764,000 | 0.15 | 2,374,000 |
| EPM9560<br>EPM9560A | 12.42 | 4,164,000 | 0.15 | 2,658,000 |

Tables 8 and 9 show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 8. MAX 9000 In-System Programming Times for Different Test Clock Frequencies**

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM9320<br>EPM9320A | 12.09 | 12.38 | 13.27 | 14.76 | 17.72 | 26.62 | 41.45 | 71.11 | s |
| EPM9400 | 12.34 | 12.67 | 13.68 | 15.37 | 18.73 | 28.83 | 45.65 | 79.30 | s |
| EPM9480 | 12.59 | 12.96 | 14.09 | 15.98 | 19.74 | 31.03 | 49.85 | 87.49 | s |
| EPM9560<br>EPM9560A | 12.84 | 13.26 | 14.50 | 16.59 | 20.75 | 33.24 | 54.06 | 95.70 | s |

**Table 9. MAX 9000 Stand-Alone Verification Times for Different Test Clock Frequencies**

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM9320<br>EPM9320A | 0.33 | 0.52 | 1.06 | 1.96 | 3.77 | 9.18 | 18.21 | 36.27 | s |
| EPM9400 | 0.36 | 0.57 | 1.20 | 2.24 | 4.33 | 10.60 | 21.05 | 41.95 | s |
| EPM9480 | 0.39 | 0.63 | 1.34 | 2.53 | 4.90 | 12.02 | 23.89 | 47.63 | s |
| EPM9560<br>EPM9560A | 0.42 | 0.69 | 1.48 | 2.81 | 5.47 | 13.44 | 26.73 | 53.31 | s |

*Figure 11. MAX 9000 JTAG Waveforms*

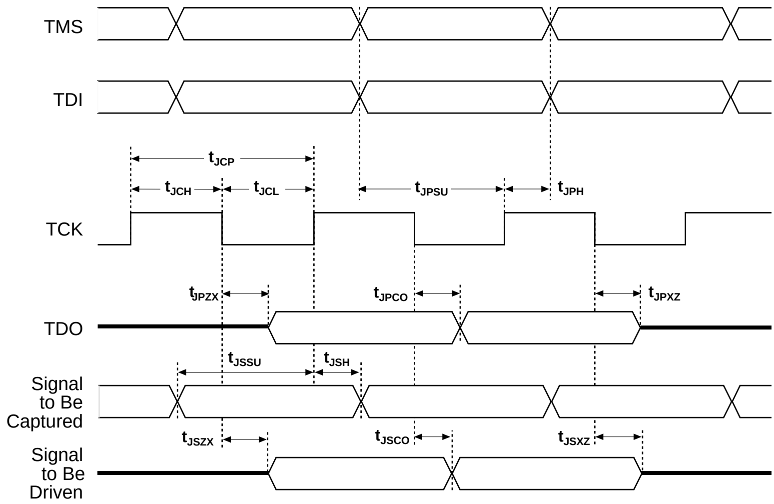



Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

***Table 13. JTAG Timing Parameters & Values for MAX 9000 Devices***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. Because most logic applications require only a small fraction of all gates to operate at maximum frequency, this feature allows total power dissipation to be reduced by 50% or more.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ($t_{LPA}$) for the LAB local array delay ($t_{LOCAL}$).

## Design Security

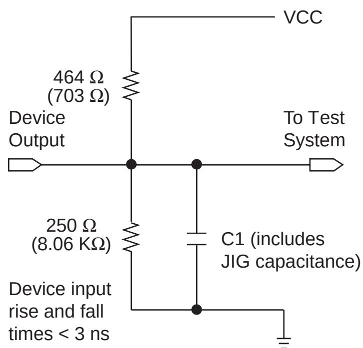
All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

## Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

**Figure 12. MAX 9000 AC Test Conditions**

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V outputs. Numbers without parentheses are for 5.0-V devices or outputs.*



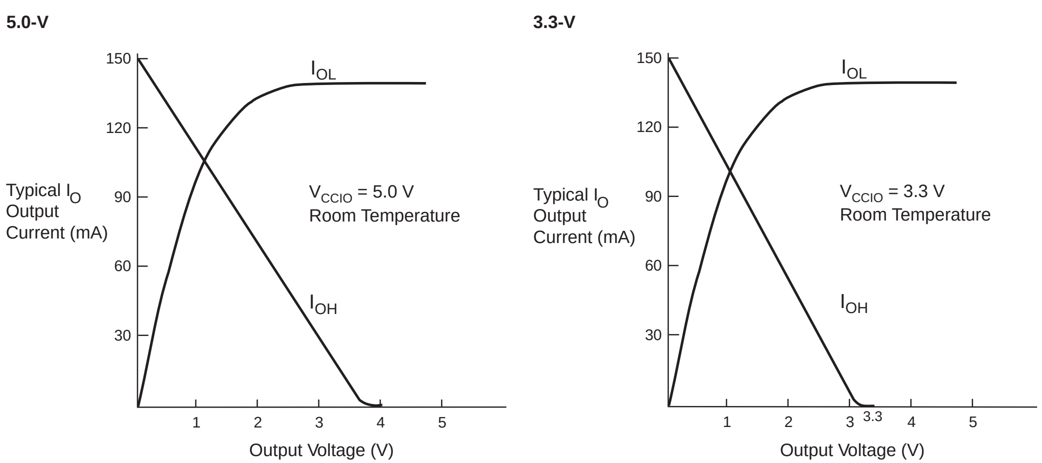
| *Table 20. MAX 9000A Device Typical $I_{CC}$ Supply Current Values* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **EPM9320A** | **EPM9560A** | **Unit** |
| $I_{CC1}$ | $I_{CC}$ supply current (low-power mode, standby, typical) | $V_I$ = ground, no load *(11)* | 99 | 174 | mA |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input on I/O pins is –0.5 V and on the four dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) $V_{CC}$ must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.
(6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 15 on page 27.
(7) During in-system programming, the minimum $V_{IH}$ of the JTAG TCK pin is 3.6 V. The minimum $V_{IH}$ of this pin during JTAG testing remains at 2.0 V. To attain this 3.6-V $V_{IH}$ during programming, the ByteBlaster and ByteBlasterMV download cables must have a 5.0-V $V_{CC}$.
(8) This parameter is measured with 50% of the outputs each sinking 12 mA. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current; the $I_{OL}$ parameter refers to the low-level TTL or CMOS output current.
(9) JTAG pin input leakage is typically –60 µA.
(10) Capacitance is sample-tested only and is measured at 25° C.
(11) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. $I_{CC}$ is measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V $V_{CCIO}$.

***Figure 13. Output Drive Characteristics of MAX 9000 Devices*** *Note (1)*




***Note:***

(1) Output drive characteristics include the JTAG TDO pin.

## Timing Model

The continuous, high-performance FastTrack Interconnect ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

The MAX 9000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell, IOC, and interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the internal timing characteristics tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, see *Application Note 77 (Understanding MAX 9000 Timing)*.

Tables 21 through 24 show timing for MAX 9000 devices.

*Table 21. MAX 9000 External Timing Characteristics* *Note (1)*

| Symbol | Parameter | Conditions | | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | -10 | | -15 | | -20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Row I/O pin input to row I/O pin output | C1 = 35 pF *(2)* | | | 10.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | Column I/O pin input to column I/O pin output | C1 = 35 pF *(2)* | EPM9320A | | 10.8 | | | | | ns |
| | | | EPM9320 | | | | 16.0 | | 23.0 | ns |
| | | | EPM9400 | | | | 16.2 | | 23.2 | ns |
| | | | EPM9480 | | | | 16.4 | | 23.4 | ns |
| | | | EPM9560A | | 11.4 | | | | | ns |
| | | | EPM9560 | | | | 16.6 | | 23.6 | ns |
| $t_{FSU}$ | Global clock setup time for I/O cell | | | 3.0 | | 5.0 | | 6.0 | | ns |
| $t_{FH}$ | Global clock hold time for I/O cell | | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FCO}$ | Global clock to I/O cell output delay | C1 = 35 pF | | 1.0 *(3)* | 4.8 | 1.0 *(3)* | 7.0 | 1.0 *(3)* | 8.5 | ns |
| $t_{CNT}$ | Minimum internal global clock period | *(4)* | | | 6.9 | | 8.5 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | | 144.9 | | 117.6 | | 100.0 | | MHz |

***Figure 15. $I_{CC}$ vs. Frequency for MAX 9000 Devices (Part 1 of 2)***

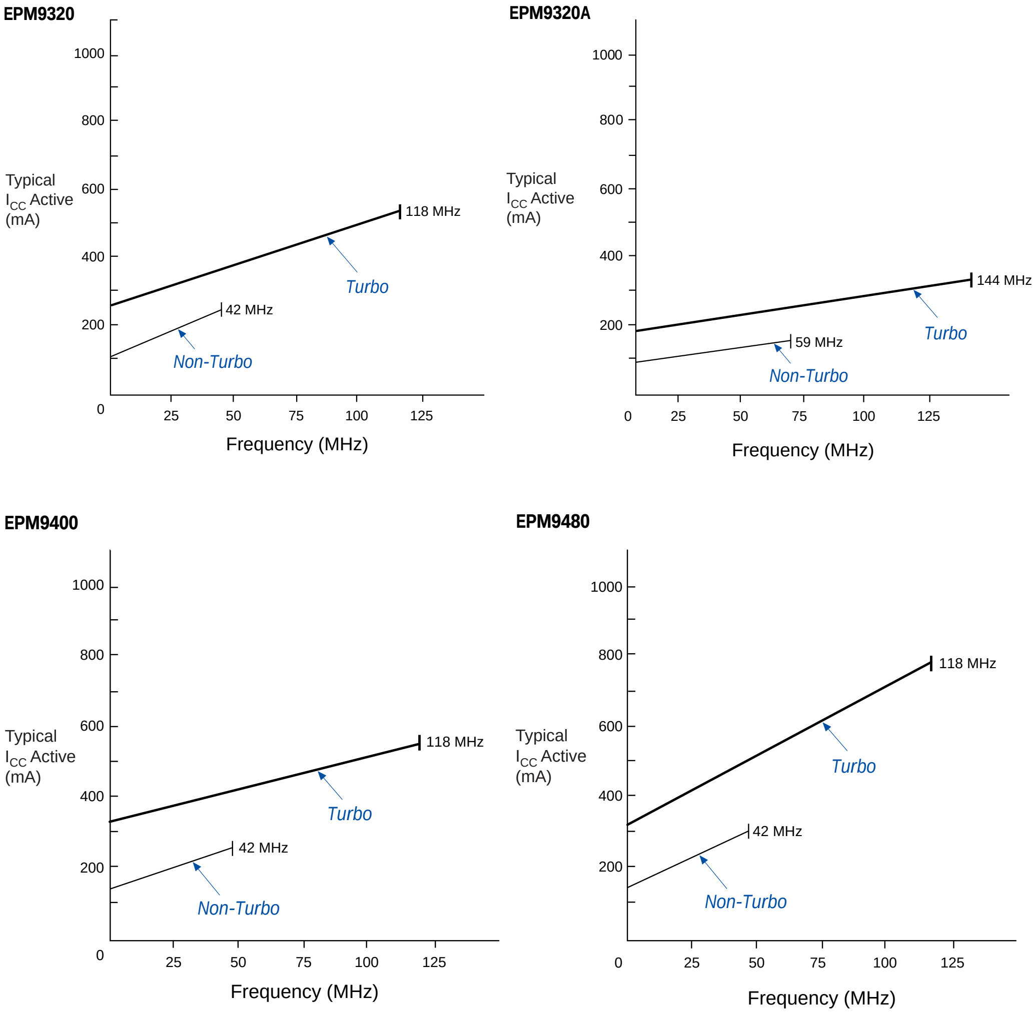
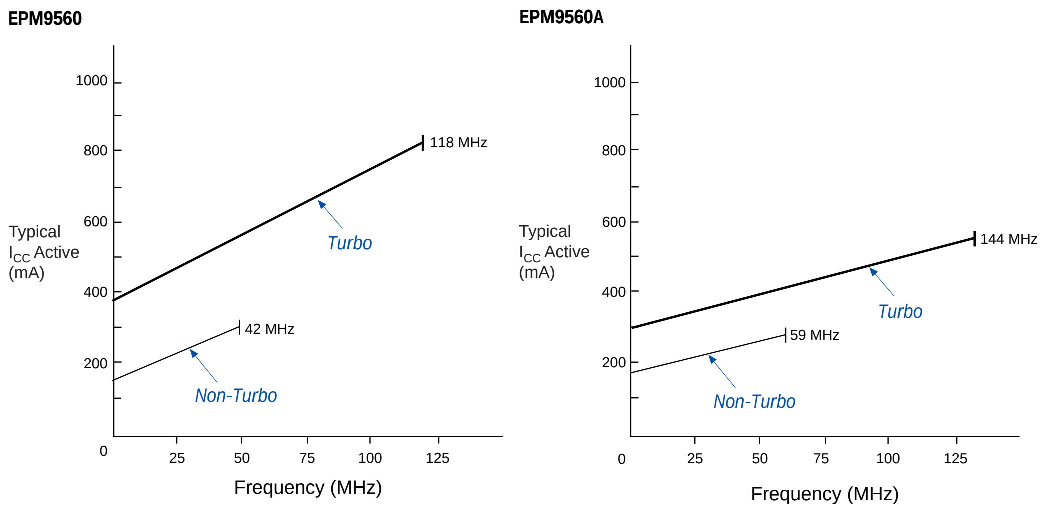


*Figure 15. $I_{CC}$ vs. Frequency for MAX 9000 Devices (Part 2 of 2)*




## Device Pin-Outs

Tables 26 through 29 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

*Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2) Note (1)*

| Pin Name | 84-Pin PLCC (2) | 208-Pin RQFP | 280-Pin PGA (3) | 356-Pin BGA |
|---|---|---|---|---|
| DIN1 (GCLK1) | 1 | 182 | V10 | AD13 |
| DIN2 (GCLK2) | 84 | 183 | U10 | AF14 |
| DIN3 (GCLR) | 13 | 153 | V17 | AD1 |
| DIN4 (GOE) | 72 | 4 | W2 | AC24 |
| TCK | 43 | 78 | A9 | A18 |
| TMS | 55 | 49 | D6 | E23 |
| TDI | 42 | 79 | C11 | A13 |
| TDO | 30 | 108 | A18 | D3 |

**Table 28. EPM9480 Dedicated Pin-Outs** *Note (1)*

| Pin Name | 208-Pin RQFP | 240-Pin RQFP |
|---|---|---|
| DIN1 (GCLK1) | 182 | 210 |
| DIN2 (GCLK2) | 183 | 211 |
| DIN3 (GCLR) | 153 | 187 |
| DIN4 (GOE) | 4 | 234 |
| TCK | 78 | 91 |
| TMS | 49 | 68 |
| TDI | 79 | 92 |
| TDO | 108 | 114 |
| GND | 14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206 | 5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229 |
| VCCINT (5.0 V only) | 10, 19, 30, 45, 112, 128, 139, 148 | 4, 24, 44, 64, 117, 137, 157, 177 |
| VCCIO (3.3 or 5.0 V) | 5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195 | 15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235 |
| No Connect (N.C.) | 6, 7, 8, 9, 109, 149, 150, 151 | 1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240 |
| VPP *(2)* | 48 | 67 |
| Total User I/O Pins *(3)* | 146 | 175 |

***Notes:***

(1) All pins not listed are user I/O pins.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.