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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 20 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | 20 |
| Number of Macrocells | 320 |
| Number of Gates | 6000 |
| Number of I/O | 132 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-BFQFP Exposed Pad |
| Supplier Device Package | 208-RQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm9320ri208-20 |

## ...and More Features

- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

***Table 2. MAX 9000 Package Options & I/O Counts*** *Note (1)*

| Device | 84-Pin PLCC | 208-Pin RQFP | 240-Pin RQFP | 280-Pin PGA | 304-Pin RQFP | 356-Pin BGA |
|---|---|---|---|---|---|---|
| EPM9320 | 60 *(2)* | 132 | – | 168 | – | 168 |
| EPM9320A | 60 *(2)* | 132 | – | – | – | 168 |
| EPM9400 | 59 *(2)* | 139 | 159 | – | – | – |
| EPM9480 | – | 146 | 175 | – | – | – |
| EPM9560 | – | 153 | 191 | 216 | 216 | 216 |
| EPM9560A | – | 153 | 191 | – | – | 216 |

***Notes:***

(1) MAX 9000 device package types include plastic J-lead chip carrier (PLCC), power quad flat pack (RQFP), ceramic pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 devices offer the MultiVolt feature, which allows output drivers to be set for either 3.3-V or 5.0-V operation in mixed-voltage systems.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins (`DIN1` and `DIN2`).

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (`DIN3`). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

## Expander Product Terms

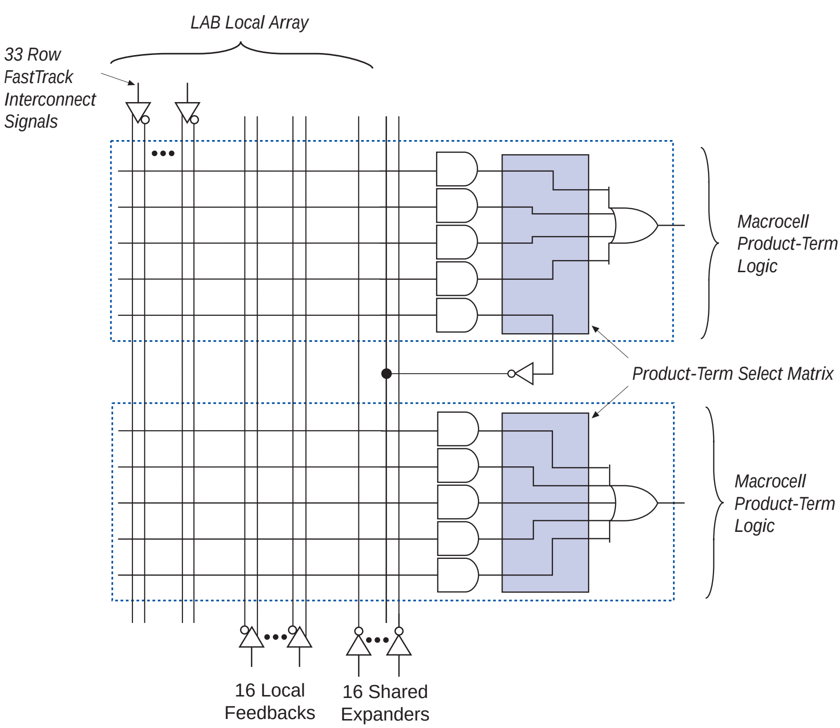
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

**Figure 4. MAX 9000 Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in the LAB.*

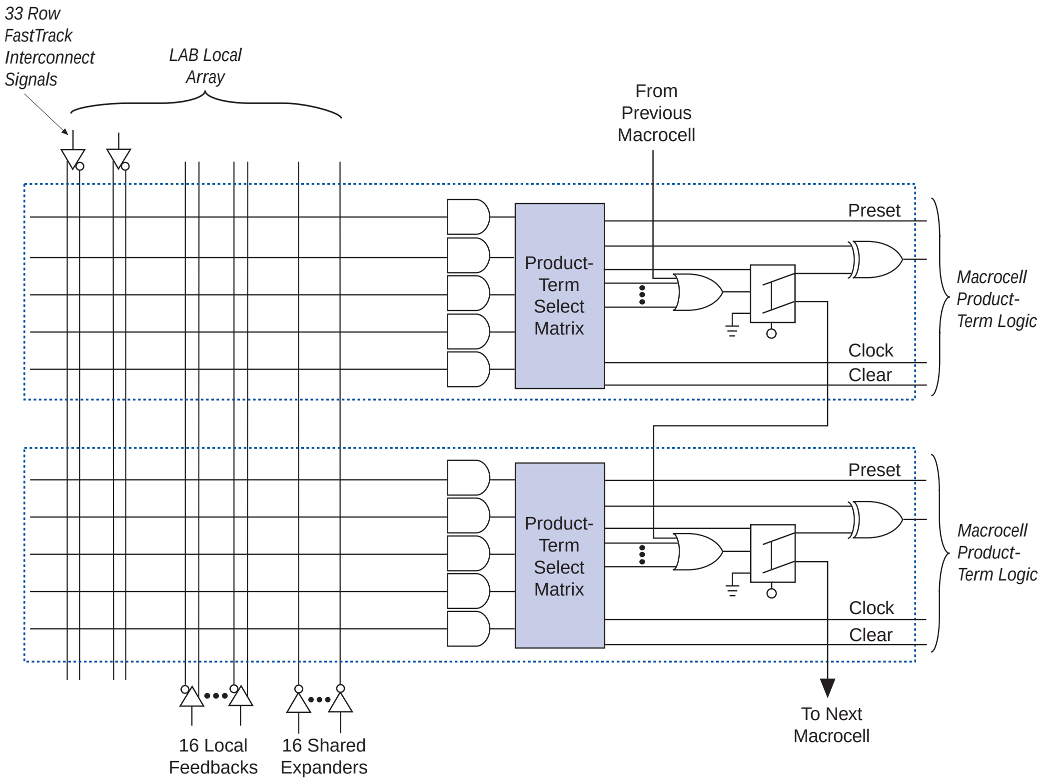


*Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

**Figure 5. MAX 9000 Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

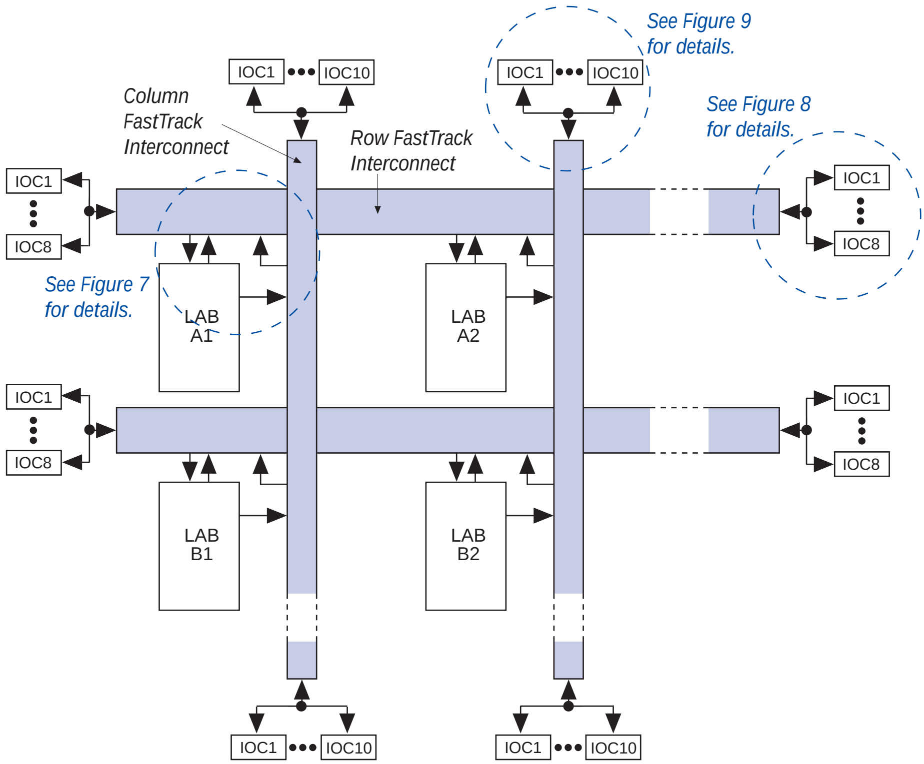
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

## FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

**Figure 6. MAX 9000 Device Interconnect Resources**

*Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.*




The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

**Table 5. MAX 9000 Rows & Columns**

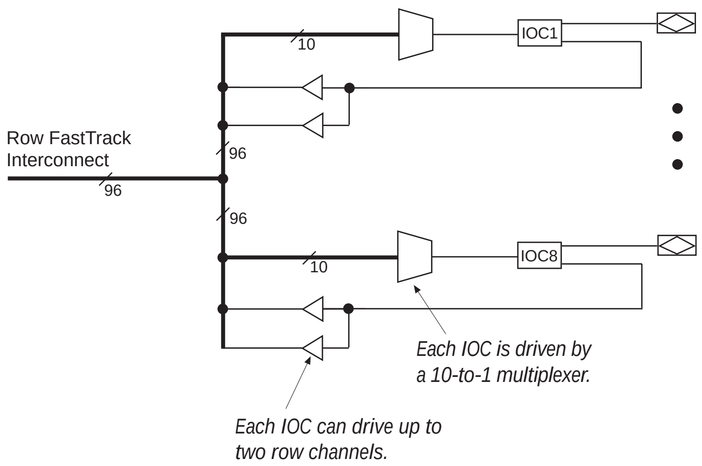
| Devices | Rows | Columns |
|---|---|---|
| EPM9320, EPM9320A | 4 | 5 |
| EPM9400 | 5 | 5 |
| EPM9480 | 6 | 5 |
| EPM9560, EPM9560A | 7 | 5 |

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

### *Row-to-I/O Cell Connections*

Figure 8 illustrates the connections between row interconnect channels and IOCs. An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

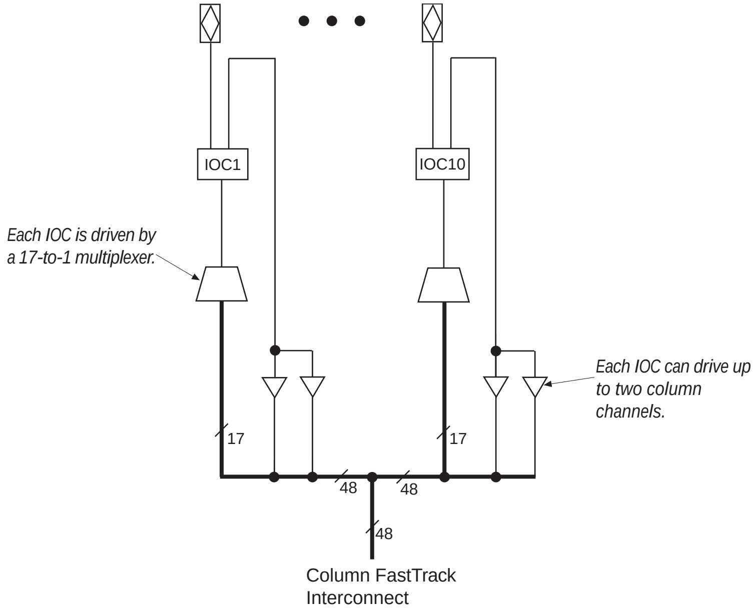
***Figure 8. MAX 9000 Row-to-IOC Connections***




### *Column-to-I/O Cell Connections*

Each end of a column channel has up to 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

*Figure 9. MAX 9000 Column-to-IOC Connections*




## Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect (see Figure 2 on page 7).

## I/O Cells

Figure 10 shows the IOC block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$.

## In-System Programmability (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an “F” suffix in the ordering code.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 9000 Device*

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
$f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

***Figure 11. MAX 9000 JTAG Waveforms***

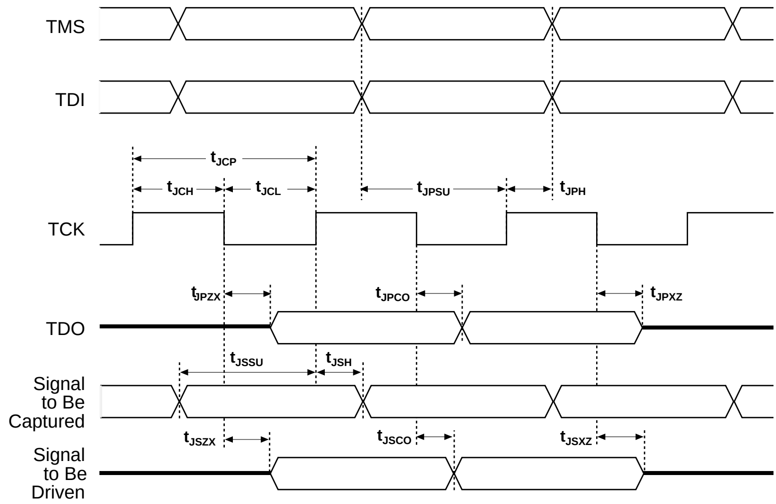



Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

***Table 13. JTAG Timing Parameters & Values for MAX 9000 Devices***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Operating Conditions

Tables 14 through 20 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 9000 devices.

*Table 14. MAX 9000 Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP packages, under bias | | 135 | ° C |

*Table 15. MAX 9000 Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

## Timing Model

The continuous, high-performance FastTrack Interconnect ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

The MAX 9000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell, IOC, and interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the internal timing characteristics tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, see *Application Note 77 (Understanding MAX 9000 Timing)*.

Tables 21 through 24 show timing for MAX 9000 devices.

*Table 21. MAX 9000 External Timing Characteristics* *Note (1)*

| Symbol | Parameter | Conditions | | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | -10 | | -15 | | -20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Row I/O pin input to row I/O pin output | C1 = 35 pF *(2)* | | | 10.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | Column I/O pin input to column I/O pin output | C1 = 35 pF *(2)* | EPM9320A | | 10.8 | | | | | ns |
| | | | EPM9320 | | | | 16.0 | | 23.0 | ns |
| | | | EPM9400 | | | | 16.2 | | 23.2 | ns |
| | | | EPM9480 | | | | 16.4 | | 23.4 | ns |
| | | | EPM9560A | | 11.4 | | | | | ns |
| | | | EPM9560 | | | | 16.6 | | 23.6 | ns |
| $t_{FSU}$ | Global clock setup time for I/O cell | | | 3.0 | | 5.0 | | 6.0 | | ns |
| $t_{FH}$ | Global clock hold time for I/O cell | | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FCO}$ | Global clock to I/O cell output delay | C1 = 35 pF | | 1.0 *(3)* | 4.8 | 1.0 *(3)* | 7.0 | 1.0 *(3)* | 8.5 | ns |
| $t_{CNT}$ | Minimum internal global clock period | *(4)* | | | 6.9 | | 8.5 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | | 144.9 | | 117.6 | | 100.0 | | MHz |

*Table 24. Interconnect Delays*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -10 | | -15 | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{LOCAL}$ | LAB local array delay | | | 0.5 | | 0.5 | | 0.5 | ns |
| $t_{ROW}$ | FastTrack row delay | *(6)* | | 0.9 | | 1.4 | | 2.0 | ns |
| $t_{COL}$ | FastTrack column delay | *(6)* | | 0.9 | | 1.7 | | 3.0 | ns |
| $t_{DIN\_D}$ | Dedicated input data delay | | | 4.0 | | 4.5 | | 5.0 | ns |
| $t_{DIN\_CLK}$ | Dedicated input clock delay | | | 2.7 | | 3.5 | | 4.0 | ns |
| $t_{DIN\_CLR}$ | Dedicated input clear delay | | | 4.5 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_IOC}$ | Dedicated input I/O register clock delay | | | 2.5 | | 3.5 | | 4.5 | ns |
| $t_{DIN\_IO}$ | Dedicated input I/O register control delay | | | 5.5 | | 6.0 | | 6.5 | ns |

***Notes to tables:***

(1) These values are specified under the MAX 9000 device recommended operating conditions, shown in Table 15 on page 27.

(2) See *Application Note 77 (Understanding MAX 9000 Timing)* for more information on test conditions for $\mathbf{t_{PD1}}$ and $\mathbf{t_{PD2}}$ delays.

(3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.

(5) The $t_{LPA}$ parameter must be added to the $t_{LOCAL}$ parameter for macrocells running in low-power mode.

(6) The $t_{ROW}$, $t_{COL}$, and $t_{IOC}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

## Power Consumption

The supply power (P) versus frequency ($\mathbf{f_{MAX}}$) for MAX 9000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCINT}$ value depends on the switching frequency and the application logic.

The $I_{CCINT}$ value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are shown below:

$MC_{TON}$ = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
$MC_{DEV}$ = Number of macrocells in the device
$MC_{USED}$ = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 25

***Table 25. MAX 9000 $I_{CC}$ Equation Constants***

| Device | Constant A | Constant B | Constant C |
|---|---|---|---|
| EPM9320 | 0.81 | 0.33 | 0.056 |
| EPM9320A | 0.56 | 0.31 | 0.024 |
| EPM9400 | 0.60 | 0.33 | 0.053 |
| EPM9480 | 0.68 | 0.29 | 0.064 |
| EPM9560 | 0.68 | 0.26 | 0.052 |
| EPM9560A | 0.56 | 0.31 | 0.024 |

This calculation provides an $I_{CC}$ estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual $I_{CC}$ values should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 15 shows typical supply current versus frequency for MAX 9000 devices.

***Figure 15. $I_{CC}$ vs. Frequency for MAX 9000 Devices (Part 1 of 2)***

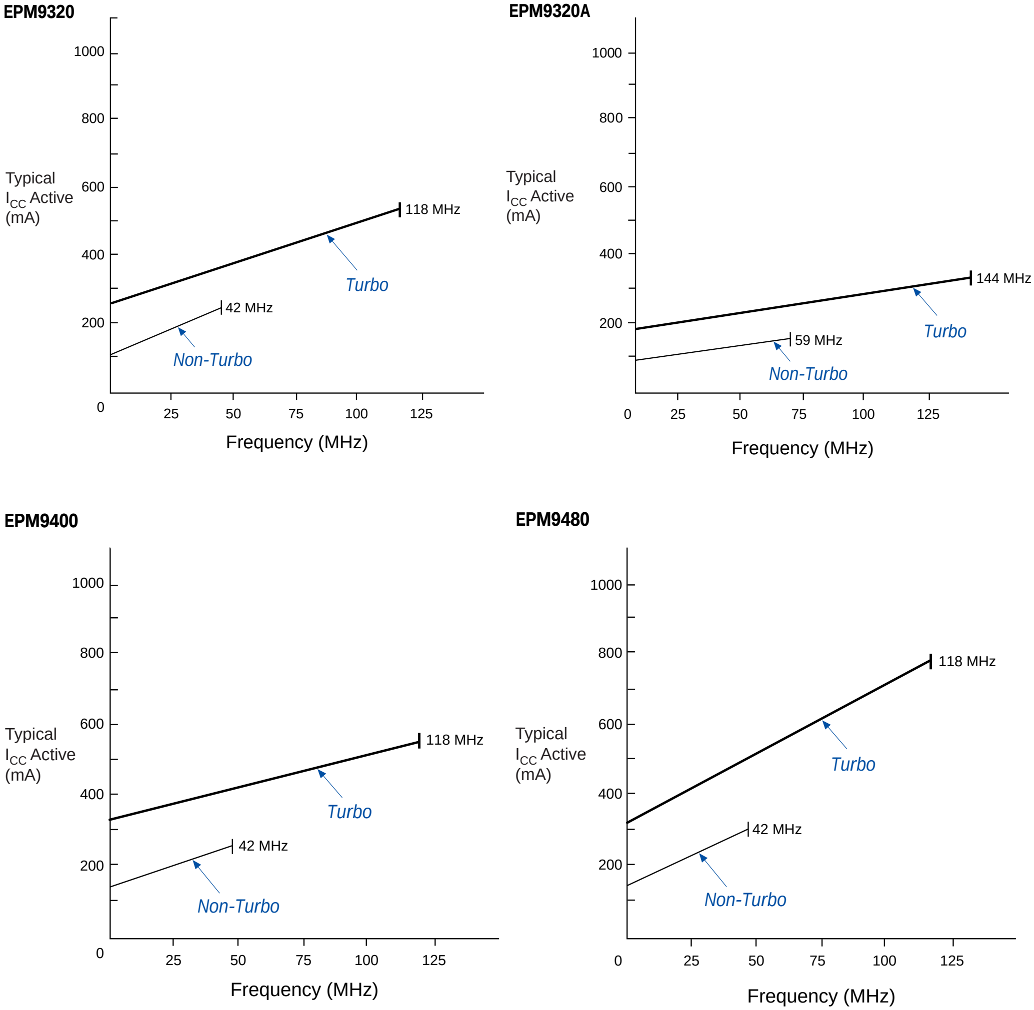
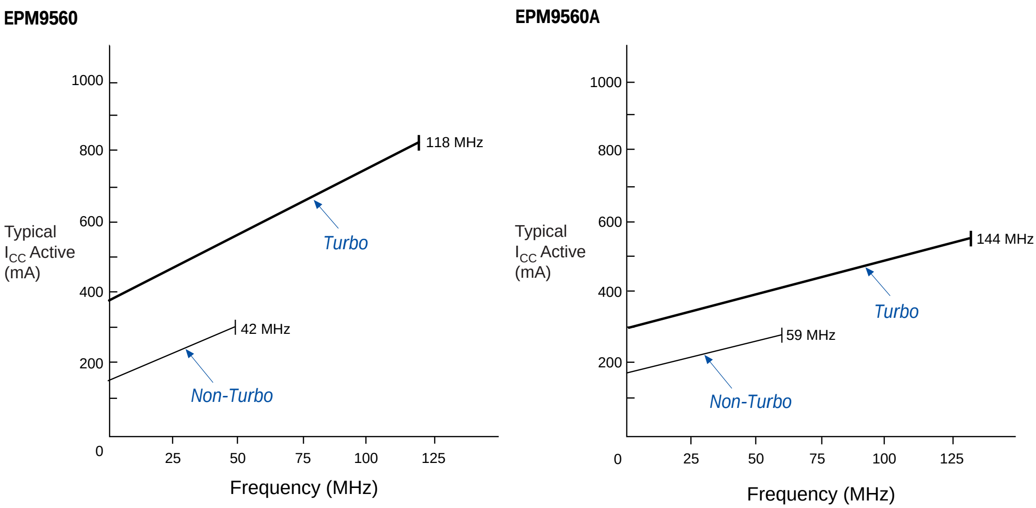


***Figure 15. $I_{CC}$ vs. Frequency for MAX 9000 Devices (Part 2 of 2)***




## Device Pin-Outs

Tables 26 through 29 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

***Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2)*** *Note (1)*

| Pin Name | 84-Pin PLCC *(2)* | 208-Pin RQFP | 280-Pin PGA *(3)* | 356-Pin BGA |
|---|---|---|---|---|
| DIN1 (GCLK1) | 1 | 182 | V10 | AD13 |
| DIN2 (GCLK2) | 84 | 183 | U10 | AF14 |
| DIN3 (GCLR) | 13 | 153 | V17 | AD1 |
| DIN4 (GOE) | 72 | 4 | W2 | AC24 |
| TCK | 43 | 78 | A9 | A18 |
| TMS | 55 | 49 | D6 | E23 |
| TDI | 42 | 79 | C11 | A13 |
| TDO | 30 | 108 | A18 | D3 |

*Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) Note (1)*

| Pin Name | 208-Pin RQFP | 240-Pin RQFP | 280-Pin PGA *(2)* | 304-Pin RQFP *(2)* | 356-Pin BGA |
|---|---|---|---|---|---|
| No Connect (N.C.) | 109 | – | B6, W1 | 1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304 | B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23 |
| VPP *(3)* | 48 | 67 | C4 | 75 | E25 |
| Total User I/O Pins *(4)* | 153 | 191 | 216 | 216 | 216 |

***Notes:***

(1) All pins not listed are user I/O pins.
(2) EPM9560A devices are not offered in this package.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.