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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 20 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 25 |
| Number of Macrocells | 400 |
| Number of Gates | 8000 |
| Number of I/O | 139 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-BFQFP Exposed Pad |
| Supplier Device Package | 208-RQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm9400rc208-20 |

## ...and More Features

- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

**Table 2. MAX 9000 Package Options & I/O Counts** *Note (1)*

| Device | 84-Pin PLCC | 208-Pin RQFP | 240-Pin RQFP | 280-Pin PGA | 304-Pin RQFP | 356-Pin BGA |
|---|---|---|---|---|---|---|
| EPM9320 | 60 *(2)* | 132 | – | 168 | – | 168 |
| EPM9320A | 60 *(2)* | 132 | – | – | – | 168 |
| EPM9400 | 59 *(2)* | 139 | 159 | – | – | – |
| EPM9480 | – | 146 | 175 | – | – | – |
| EPM9560 | – | 153 | 191 | 216 | 216 | 216 |
| EPM9560A | – | 153 | 191 | – | – | 216 |

***Notes:***

(1) MAX 9000 device package types include plastic J-lead chip carrier (PLCC), power quad flat pack (RQFP), ceramic pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

## Functional Description

MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

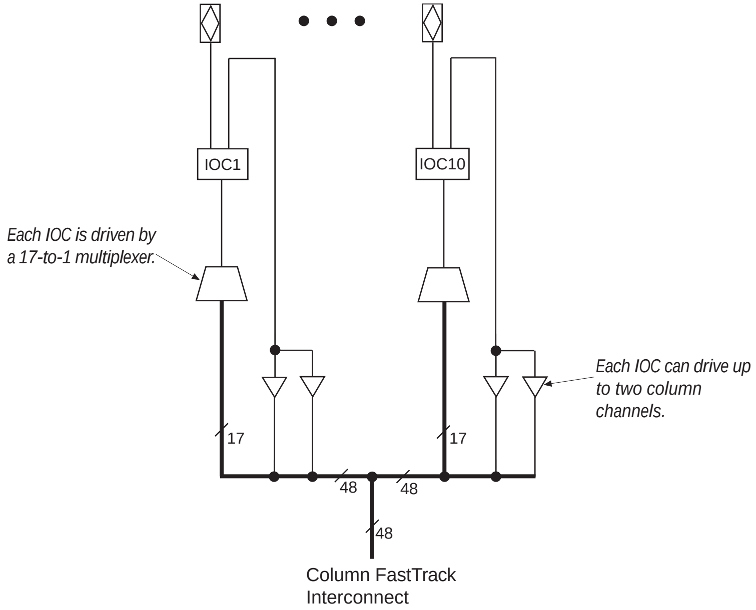
The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

## FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

*Figure 9. MAX 9000 Column-to-IOC Connections*



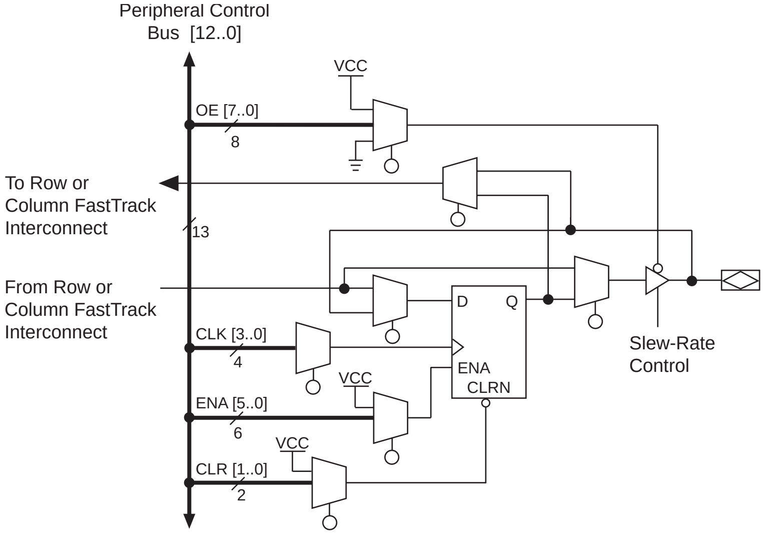

## Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect (see Figure 2 on page 7).

## I/O Cells

Figure 10 shows the IOC block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

*Figure 10. MAX 9000 IOC*




I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 on page 18 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay ($t_{OD}$) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis. The slew rate control affects both rising and falling edges of the output signals.

*Table 6. Peripheral Bus Sources*

| Peripheral Control Signal | Source | | | |
|---|---|---|---|---|
| | EPM9320 EPM9320A | EPM9400 | EPM9480 | EPM9560 EPM9560A |
| OE0/ENA0 | Row C | Row E | Row F | Row G |
| OE1/ENA1 | Row B | Row E | Row F | Row F |
| OE2/ENA2 | Row A | Row E | Row E | Row E |
| OE3/ENA3 | Row B | Row B | Row B | Row B |
| OE4/ENA4 | Row A | Row A | Row A | Row A |
| OE5 | Row D | Row D | Row D | Row D |
| OE6 | Row C | Row C | Row C | Row C |
| OE7/CLR1 | Row B/GOE | Row B/GOE | Row B/GOE | Row B/GOE |
| CLR0/ENA5 | Row A/GCLR | Row A/GCLR | Row A/GCLR | Row A/GCLR |
| CLK0 | GCLK1 | GCLK1 | GCLK1 | GCLK1 |
| CLK1 | GCLK2 | GCLK2 | GCLK2 | GCLK2 |
| CLK2 | Row D | Row D | Row D | Row D |
| CLK3 | Row C | Row C | Row C | Row C |

## Output Configuration

The MAX 9000 device architecture supports the MultiVolt I/O interface feature, which allows MAX 9000 devices to interface with systems of differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 9000 device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 9000 Device*

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:
- $t_{PROG}$ = Programming time
- $t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
- $Cycle_{PTCK}$ = Number of TCK cycles to program a device
- $f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:
- $t_{VER}$ = Verify time
- $t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
- $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

***Figure 11. MAX 9000 JTAG Waveforms***

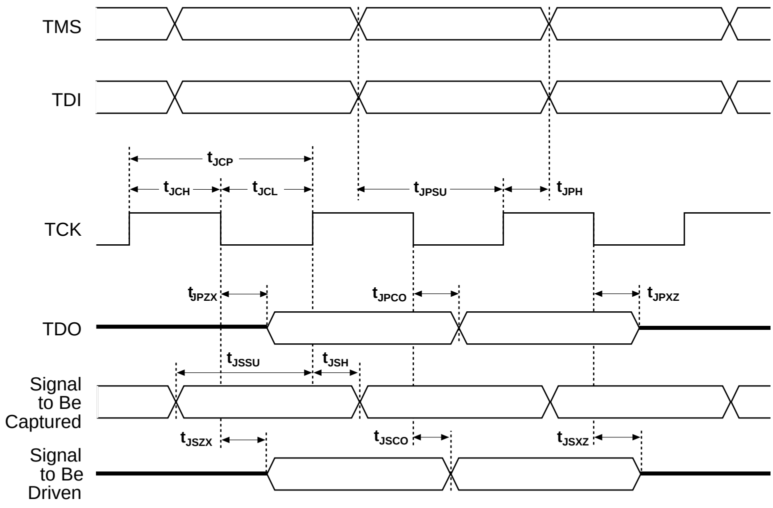



Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

***Table 13. JTAG Timing Parameters & Values for MAX 9000 Devices***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. Because most logic applications require only a small fraction of all gates to operate at maximum frequency, this feature allows total power dissipation to be reduced by 50% or more.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ($t_{LPA}$) for the LAB local array delay ($t_{LOCAL}$).

## Design Security

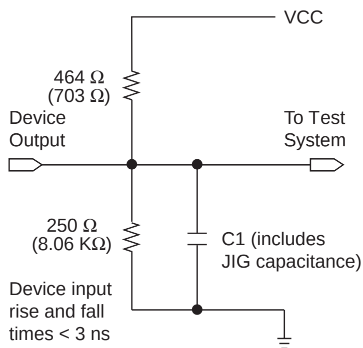
All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

## Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

***Figure 12. MAX 9000 AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V outputs. Numbers without parentheses are for 5.0-V devices or outputs.*



## Operating Conditions

Tables 14 through 20 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 9000 devices.

**Table 14. MAX 9000 Device Absolute Maximum Ratings** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP packages, under bias | | 135 | ° C |

**Table 15. MAX 9000 Device Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCISP}$ | Supply voltage during in-system programming | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 20. MAX 9000A Device Typical $I_{CC}$ Supply Current Values*

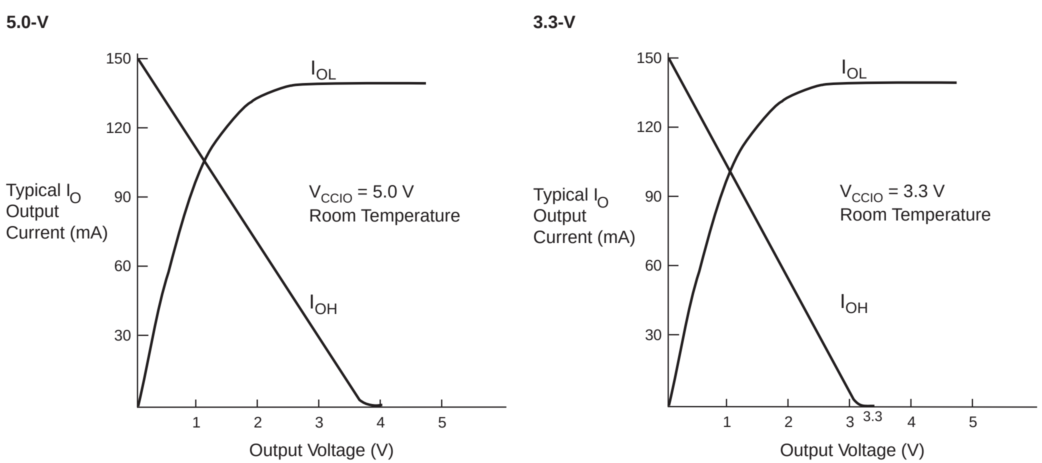
| Symbol | Parameter | Conditions | EPM9320A | EPM9560A | Unit |
|---|---|---|---|---|---|
| $I_{CC1}$ | $I_{CC}$ supply current (low-power mode, standby, typical) | $V_I$ = ground, no load *(11)* | 99 | 174 | mA |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input on I/O pins is –0.5 V and on the four dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) $V_{CC}$ must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.
(6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 15 on page 27.
(7) During in-system programming, the minimum $V_{IH}$ of the JTAG TCK pin is 3.6 V. The minimum $V_{IH}$ of this pin during JTAG testing remains at 2.0 V. To attain this 3.6-V $V_{IH}$ during programming, the ByteBlaster and ByteBlasterMV download cables must have a 5.0-V $V_{CC}$.
(8) This parameter is measured with 50% of the outputs each sinking 12 mA. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current; the $I_{OL}$ parameter refers to the low-level TTL or CMOS output current.
(9) JTAG pin input leakage is typically –60 µA.
(10) Capacitance is sample-tested only and is measured at 25° C.
(11) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. $I_{CC}$ is measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V $V_{CCIO}$.

*Figure 13. Output Drive Characteristics of MAX 9000 Devices* *Note (1)*




***Note:***

(1) Output drive characteristics include the JTAG TDO pin.

Tables 21 through 24 show timing for MAX 9000 devices.

***Table 21. MAX 9000 External Timing Characteristics*** *Note (1)*

| Symbol | Parameter | Conditions | | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | -10 | | -15 | | -20 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Row I/O pin input to row I/O pin output | C1 = 35 pF *(2)* | | | 10.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | Column I/O pin input to column I/O pin output | C1 = 35 pF *(2)* | EPM9320A | | 10.8 | | | | | ns |
| | | | EPM9320 | | | | 16.0 | | 23.0 | ns |
| | | | EPM9400 | | | | 16.2 | | 23.2 | ns |
| | | | EPM9480 | | | | 16.4 | | 23.4 | ns |
| | | | EPM9560A | | 11.4 | | | | | ns |
| | | | EPM9560 | | | | 16.6 | | 23.6 | ns |
| $t_{FSU}$ | Global clock setup time for I/O cell | | | 3.0 | | 5.0 | | 6.0 | | ns |
| $t_{FH}$ | Global clock hold time for I/O cell | | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FCO}$ | Global clock to I/O cell output delay | C1 = 35 pF | | 1.0 *(3)* | 4.8 | 1.0 *(3)* | 7.0 | 1.0 *(3)* | 8.5 | ns |
| $t_{CNT}$ | Minimum internal global clock period | *(4)* | | | 6.9 | | 8.5 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | | 144.9 | | 117.6 | | 100.0 | | MHz |

*Table 24. Interconnect Delays*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -10 | | -15 | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{LOCAL}$ | LAB local array delay | | | 0.5 | | 0.5 | | 0.5 | ns |
| $t_{ROW}$ | FastTrack row delay | (6) | | 0.9 | | 1.4 | | 2.0 | ns |
| $t_{COL}$ | FastTrack column delay | (6) | | 0.9 | | 1.7 | | 3.0 | ns |
| $t_{DIN\_D}$ | Dedicated input data delay | | | 4.0 | | 4.5 | | 5.0 | ns |
| $t_{DIN\_CLK}$ | Dedicated input clock delay | | | 2.7 | | 3.5 | | 4.0 | ns |
| $t_{DIN\_CLR}$ | Dedicated input clear delay | | | 4.5 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_IOC}$ | Dedicated input I/O register clock delay | | | 2.5 | | 3.5 | | 4.5 | ns |
| $t_{DIN\_IO}$ | Dedicated input I/O register control delay | | | 5.5 | | 6.0 | | 6.5 | ns |

***Notes to tables:***

(1) These values are specified under the MAX 9000 device recommended operating conditions, shown in Table 15 on page 27.

(2) See *Application Note 77 (Understanding MAX 9000 Timing)* for more information on test conditions for $\mathbf{t_{PD1}}$ and $\mathbf{t_{PD2}}$ delays.

(3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.

(5) The $t_{LPA}$ parameter must be added to the $t_{LOCAL}$ parameter for macrocells running in low-power mode.

(6) The $t_{ROW}$, $t_{COL}$, and $t_{IOC}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

## Power Consumption

The supply power (P) versus frequency ($\mathbf{f_{MAX}}$) for MAX 9000 devices can be calculated with the following equation:

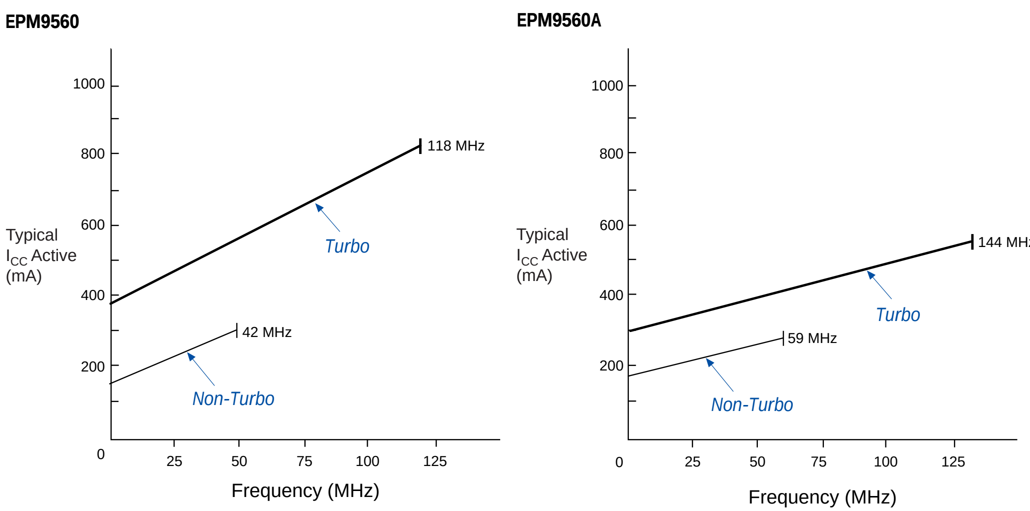
$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCINT}$ value depends on the switching frequency and the application logic.

The $I_{CCINT}$ value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

*Figure 15. $I_{CC}$ vs. Frequency for MAX 9000 Devices (Part 2 of 2)*




## Device Pin-Outs

Tables 26 through 29 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

**Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2)** Note (1)

| Pin Name | 84-Pin PLCC (2) | 208-Pin RQFP | 280-Pin PGA (3) | 356-Pin BGA |
|---|---|---|---|---|
| DIN1 (GCLK1) | 1 | 182 | V10 | AD13 |
| DIN2 (GCLK2) | 84 | 183 | U10 | AF14 |
| DIN3 (GCLR) | 13 | 153 | V17 | AD1 |
| DIN4 (GOE) | 72 | 4 | W2 | AC24 |
| TCK | 43 | 78 | A9 | A18 |
| TMS | 55 | 49 | D6 | E23 |
| TDI | 42 | 79 | C11 | A13 |
| TDO | 30 | 108 | A18 | D3 |

*Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 2 of 2)* *Note (1)*

| Pin Name | 84-Pin PLCC *(2)* | 208-Pin RQFP | 280-Pin PGA *(3)* | 356-Pin BGA |
|---|---|---|---|---|
| GND | 6, 18, 24, 25, 48, 61, 67, 70 | 14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206 | D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16 | A9, A22, A25, A26, B25, B26, D2, E1, E26, F2, G1, G25, G26, H2, J1, J25, J26, K2, L26, M26, N1, N25, P26, R2, T1, U2, U26, V1, V25, W25, Y26, AA2, AB1, AB26, AC26, AE1, AF1, AF2, AF4, AF7, AF20 |
| VCCINT (5.0 V only) | 14, 21, 28, 57, 64, 71 | 10, 19, 30, 45, 112, 128, 139, 148 | D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14 | D26, F1, H1, K26, N26, P1, U1, W26, AE26, AF25, AF26 |
| VCCIO (3.3 or 5.0 V) | 15, 37, 60, 79 | 5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195 | D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15 | A1, A2, A21, B1, B10, B24, D1, H26, K1, M25, R1, V26, AA1, AC25, AF5, AF8, AF19 |
| No Connect (N.C.) | 29 | 6, 7, 8, 9, 11, 12, 13, 15, 16, 17, 18, 109, 140, 141, 142, 144, 145, 146, 147, 149, 150, 151 | B6, K19, L2, L4, L18, L19, M1, M2, M3, M4, M16, M17, M18, M19, N1, N2, N3, N4, N16, N17, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1 | B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, R3, R26, T2, T3, T4, T5, T22, T23, T24, T25, T26, U3, U4, U5, U22, U23, U24, U25, V2, V3, V4, V5, V22, V23, V24, W1, W2, W3, W4, W5, W22, W23, W24, Y1, Y2, Y3, Y4, Y5, Y22, Y23, Y24, Y25, AA3, AA4, AA5, AA22, AA23, AA24, AA25, AA26, AB2, AB3, AB4, AB5, AB23, AB24, AB25, AC1, AC2, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23 |
| VPP *(4)* | 56 | 48 | C4 | E25 |
| Total User I/O Pins *(5)* | 60 | 132 | 168 | 168 |

***Notes:***
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.
(3) EPM9320A devices are not offered in this package.
(4) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

***Table 27. EPM9400 Dedicated Pin-Outs*** *Note (1)*

| Pin Name | 84-Pin PLCC *(2)* | 208-Pin RQFP | 240-Pin RQFP |
|---|---|---|---|
| DIN1 (GCLK1) | 2 | 182 | 210 |
| DIN2 (GCLK2) | 1 | 183 | 211 |
| DIN3 (GCLR) | 12 | 153 | 187 |
| DIN4 (GOE) | 74 | 4 | 234 |
| TCK | 43 | 78 | 91 |
| TMS | 54 | 49 | 68 |
| TDI | 42 | 79 | 92 |
| TDO | 31 | 108 | 114 |
| GND | 6, 13, 20, 26, 27, 47, 60, 66, 69, 73 | 14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206 | 5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229 |
| VCCINT (5.0 V only) | 16, 23, 30, 56, 63, 70 | 10, 19, 30, 45, 112, 128, 139, 148 | 4, 24, 44, 64, 117, 137, 157, 177 |
| VCCIO (3.3 or 5.0 V) | 17, 37, 59, 80 | 5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195 | 15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235 |
| No Connect (N.C.) | – | 6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151 | 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240 |
| VPP *(3)* | 55 | 48 | 67 |
| Total User I/O Pins *(4)* | 59 | 139 | 159 |

***Notes:***
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

**Table 28. EPM9480 Dedicated Pin-Outs** *Note (1)*

| Pin Name | 208-Pin RQFP | 240-Pin RQFP |
|---|---|---|
| DIN1 (GCLK1) | 182 | 210 |
| DIN2 (GCLK2) | 183 | 211 |
| DIN3 (GCLR) | 153 | 187 |
| DIN4 (GOE) | 4 | 234 |
| TCK | 78 | 91 |
| TMS | 49 | 68 |
| TDI | 79 | 92 |
| TDO | 108 | 114 |
| GND | 14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206 | 5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229 |
| VCCINT (5.0 V only) | 10, 19, 30, 45, 112, 128, 139, 148 | 4, 24, 44, 64, 117, 137, 157, 177 |
| VCCIO (3.3 or 5.0 V) | 5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195 | 15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235 |
| No Connect (N.C.) | 6, 7, 8, 9, 109, 149, 150, 151 | 1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240 |
| VPP *(2)* | 48 | 67 |
| Total User I/O Pins *(3)* | 146 | 175 |

***Notes:***

(1) All pins not listed are user I/O pins.
(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(3) The user I/O pin count includes dedicated input pins and all I/O pins.

| *Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) Note (1)* | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **208-Pin RQFP** | **240-Pin RQFP** | **280-Pin PGA** *(2)* | **304-Pin RQFP** *(2)* | **356-Pin BGA** |
| No Connect (N.C.) | 109 | – | B6, W1 | 1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304 | B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23 |
| VPP *(3)* | 48 | 67 | C4 | 75 | E25 |
| Total User I/O Pins *(4)* | 153 | 191 | 216 | 216 | 216 |

***Notes:***

(1) All pins not listed are user I/O pins.
(2) EPM9560A devices are not offered in this package.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.