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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	30
Number of Macrocells	480
Number of Gates	10000
Number of I/O	146
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm9480rc208-15">https://www.e-xfl.com/product-detail/intel/epm9480rc208-15</a>

## General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the **PCI Local Bus Specification, Revision 2.2**. Table 3 shows the speed grades available for MAX 9000 devices.

**Table 3. MAX 9000 Speed Grade Availability**

Device	Speed Grade		
	-10	-15	-20
EPM9320		✓	✓
EPM9320A	✓		
EPM9400		✓	✓
EPM9480		✓	✓
EPM9560		✓	✓
EPM9560A	✓		

Table 4 shows the performance of MAX 9000 devices for typical functions.

**Table 4. MAX 9000 Performance** Note (1)

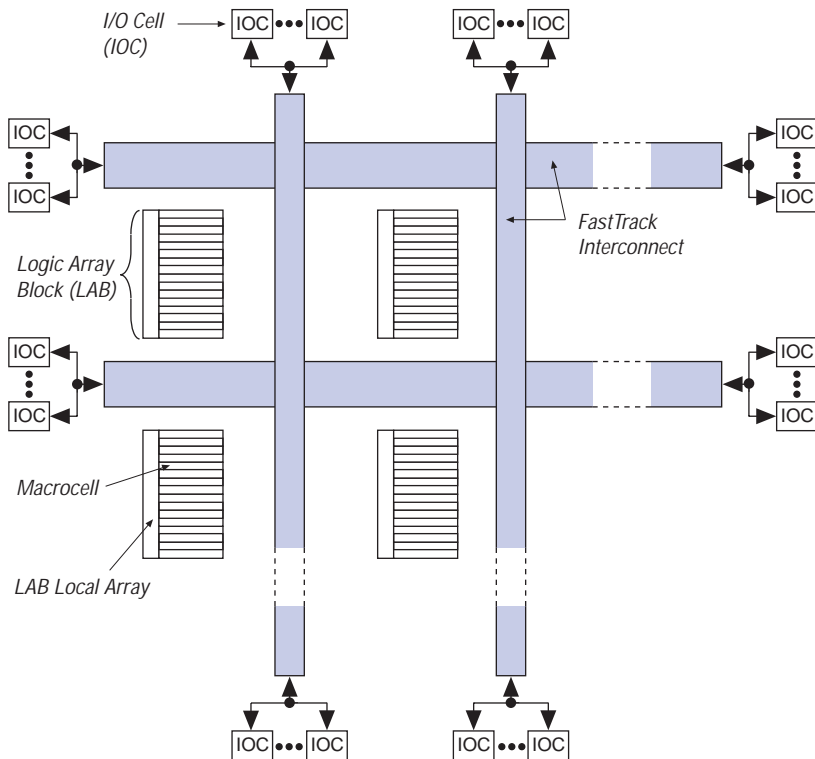
Application	Macrocells Used	Speed Grade			Units
		-10	-15	-20	
16-bit loadable counter	16	144	118	100	MHz
16-bit up/down counter	16	144	118	100	MHz
16-bit prescaled counter	16	144	118	100	MHz
16-bit address decode	1	5.6 (10)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	7.7 (12.1)	10.9 (18)	16 (26)	ns

**Note:**

- (1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

Figure 1. MAX 9000 Device Block Diagram



## Logic Array Blocks

The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in [Figure 2 on page 7](#). Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms (“expanders”) are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins (DIN1 and DIN2).

Each register also supports asynchronous preset and clear functions. As shown in [Figure 3](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

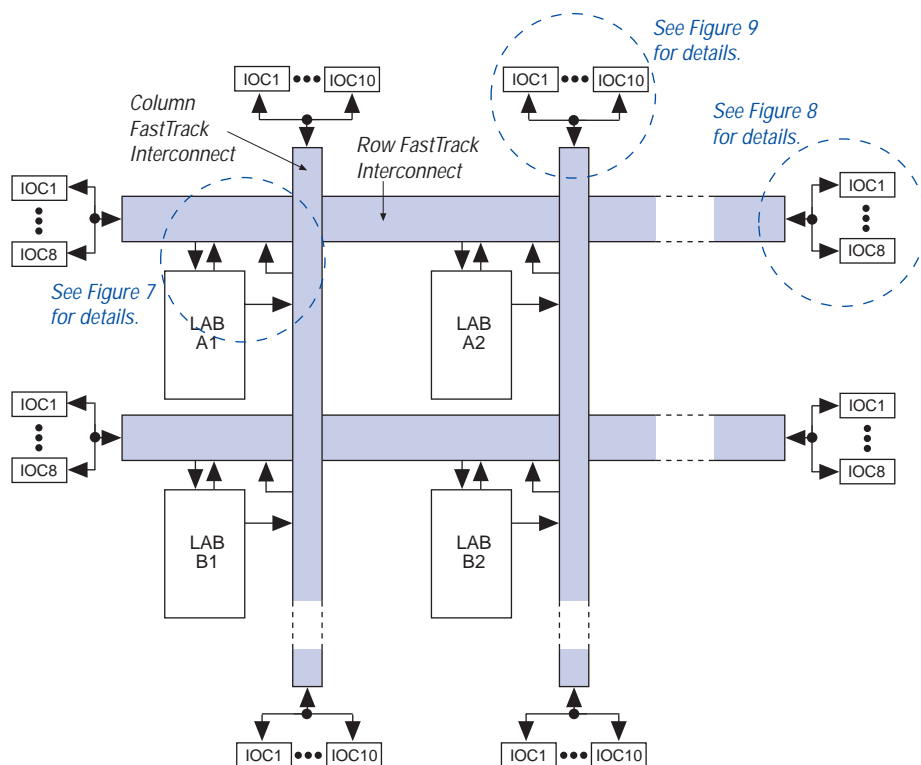
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

### FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. [Figure 6](#) shows the interconnection of four adjacent LABs with row and column interconnects.

**Figure 6. MAX 9000 Device Interconnect Resources**

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

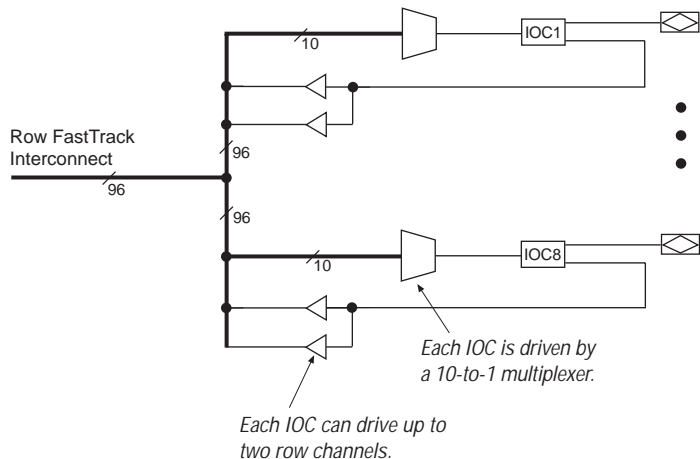
Table 5. MAX 9000 Rows & Columns		
Devices	Rows	Columns
EPM9320, EPM9320A	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560, EPM9560A	7	5

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

#### *Row-to-I/O Cell Connections*

**Figure 8** illustrates the connections between row interconnect channels and IOCs. An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

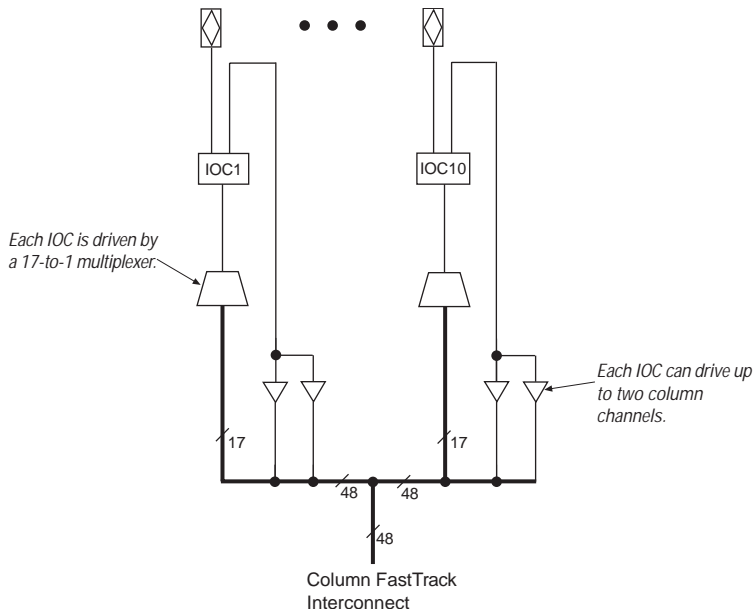
**Figure 8.** MAX 9000 Row-to-IOC Connections



#### *Column-to-I/O Cell Connections*

Each end of a column channel has up to 10 IOCs (see **Figure 9**). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Figure 9. MAX 9000 Column-to-I/O Connections



## Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect (see [Figure 2 on page 7](#)).

## I/O Cells

[Figure 10](#) shows the IOC block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.



The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay ( $t_{OD}$ ) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis. The slew rate control affects both rising and falling edges of the output signals.

*Table 6. Peripheral Bus Sources*

Peripheral Control Signal	Source			
	EPM9320 EPM9320A	EPM9400	EPM9480	EPM9560 EPM9560A
OE0/ENA0	Row C	Row E	Row F	Row G
OE1/ENA1	Row B	Row E	Row F	Row F
OE2/ENA2	Row A	Row E	Row E	Row E
OE3/ENA3	Row B	Row B	Row B	Row B
OE4/ENA4	Row A	Row A	Row A	Row A
OE5	Row D	Row D	Row D	Row D
OE6	Row C	Row C	Row C	Row C
OE7/CLR1	Row B/GOE	Row B/GOE	Row B/GOE	Row B/GOE
CLR0/ENA5	Row A/GCLR	Row A/GCLR	Row A/GCLR	Row A/GCLR
CLK0	GCLK1	GCLK1	GCLK1	GCLK1
CLK1	GCLK2	GCLK2	GCLK2	GCLK2
CLK2	Row D	Row D	Row D	Row D
CLK3	Row C	Row C	Row C	Row C

## Output Configuration

The MAX 9000 device architecture supports the MultiVolt I/O interface feature, which allows MAX 9000 devices to interface with systems of differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCINT}$  pins must always be connected to a 5.0-V power supply. With a 5.0-V  $V_{CCINT}$  level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

## In-System Programmability (ISP)

The  $V_{CCIO}$  pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 9000 device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

The programming times described in [Tables 7 through 9](#) are associated with the worst-case method using the ISP algorithm.

**Table 7. MAX 9000  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PPULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EPM9320 EPM9320A	11.79	2,966,000	0.15	1,806,000
EPM9400	12.00	3,365,000	0.15	2,090,000
EPM9480	12.21	3,764,000	0.15	2,374,000
EPM9560 EPM9560A	12.42	4,164,000	0.15	2,658,000

[Tables 8 and 9](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 8. MAX 9000 In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	12.09	12.38	13.27	14.76	17.72	26.62	41.45	71.11	s
EPM9400	12.34	12.67	13.68	15.37	18.73	28.83	45.65	79.30	s
EPM9480	12.59	12.96	14.09	15.98	19.74	31.03	49.85	87.49	s
EPM9560 EPM9560A	12.84	13.26	14.50	16.59	20.75	33.24	54.06	95.70	s

**Table 9. MAX 9000 Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	0.33	0.52	1.06	1.96	3.77	9.18	18.21	36.27	s
EPM9400	0.36	0.57	1.20	2.24	4.33	10.60	21.05	41.95	s
EPM9480	0.39	0.63	1.34	2.53	4.90	12.02	23.89	47.63	s
EPM9560 EPM9560A	0.42	0.69	1.48	2.81	5.47	13.44	26.73	53.31	s

The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. [Tables 11 and 12](#) show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

**Table 11. MAX 9000 Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

**Table 12. 32-Bit MAX 9000 Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) (2)	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A (3)	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A (3)	0000	1001 0101 0110 0000	00001101110	1

**Notes:**

- (1) The IDCODE's least significant bit (LSB) is always 1.
- (2) The most significant bit (MSB) is on the left.
- (3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

[Figure 11](#) shows the timing requirements for the JTAG signals.

Figure 11. MAX 9000 JTAG Waveforms

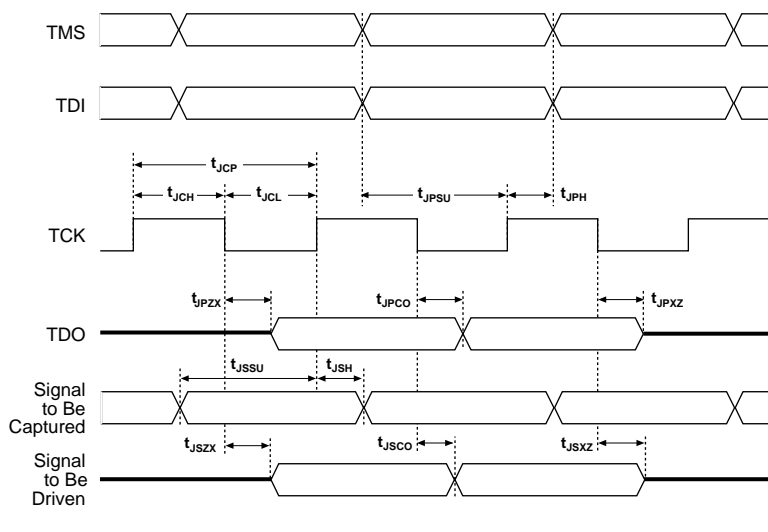


Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

Table 13. JTAG Timing Parameters &amp; Values for MAX 9000 Devices

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns



For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Table 23. IOC Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
$t_{IODR}$	I/O row output data delay			0.2		0.2		1.5	ns
$t_{IDOC}$	I/O column output data delay			0.4		0.2		1.5	ns
$t_{IOC}$	I/O control delay	(6)		0.5		1.0		2.0	ns
$t_{IORD}$	I/O register clock-to-output delay			0.6		1.0		1.5	ns
$t_{IOCOMB}$	I/O combinatorial delay			0.2		1.0		1.5	ns
$t_{IOSU}$	I/O register setup time before clock		2.0		4.0		5.0		ns
$t_{IOH}$	I/O register hold time after clock		1.0		1.0		1.0		ns
$t_{IOCLR}$	I/O register clear delay			1.5		3.0		3.0	ns
$t_{IOFD}$	I/O register feedback delay			0.0		0.0		0.5	ns
$t_{INREG}$	I/O input pad and buffer to I/O register delay			3.5		4.5		5.5	ns
$t_{INCOMB}$	I/O input pad and buffer to row and column delay			1.5		2.0		2.5	ns
$t_{OD1}$	Output buffer and pad delay, Slow slew rate = off, $V_{CCIO} = 5.0$ V	C1 = 35 pF		1.8		2.5		2.5	ns
$t_{OD2}$	Output buffer and pad delay, Slow slew rate = off, $V_{CCIO} = 3.3$ V	C1 = 35 pF		2.3		3.5		3.5	ns
$t_{OD3}$	Output buffer and pad delay, Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	C1 = 35 pF		8.3		10.0		10.5	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		2.5		2.5		2.5	ns
$t_{ZX1}$	Output buffer enable delay, Slow slew rate = off, $V_{CCIO} = 5.0$ V	C1 = 35 pF		2.5		2.5		2.5	ns
$t_{ZX2}$	Output buffer enable delay, Slow slew rate = off, $V_{CCIO} = 3.3$ V	C1 = 35 pF		3.0		3.5		3.5	ns
$t_{ZX3}$	Output buffer enable delay, Slow slew rate = on, $V_{CCIO} = 3.3$ V or 5.0 V	C1 = 35 pF		9.0		10.0		10.5	ns

Table 24. Interconnect Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
$t_{LOCAL}$	LAB local array delay			0.5		0.5		0.5	ns
$t_{ROW}$	FastTrack row delay	(6)		0.9		1.4		2.0	ns
$t_{COL}$	FastTrack column delay	(6)		0.9		1.7		3.0	ns
$t_{DIN\_D}$	Dedicated input data delay			4.0		4.5		5.0	ns
$t_{DIN\_CLK}$	Dedicated input clock delay			2.7		3.5		4.0	ns
$t_{DIN\_CLR}$	Dedicated input clear delay			4.5		5.0		5.5	ns
$t_{DIN\_IOC}$	Dedicated input I/O register clock delay			2.5		3.5		4.5	ns
$t_{DIN\_IO}$	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

**Notes to tables:**

- (1) These values are specified under the MAX 9000 device recommended operating conditions, shown in [Table 15 on page 27](#).
- (2) See [Application Note 77 \(Understanding MAX 9000 Timing\)](#) for more information on test conditions for  $t_{PD1}$  and  $t_{PD2}$  delays.
- (3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.
- (4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
- (5) The  $t_{LPA}$  parameter must be added to the  $t_{LOCAL}$  parameter for macrocells running in low-power mode.
- (6) The  $t_{ROW}$ ,  $t_{COL}$ , and  $t_{IOC}$  delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

## Power Consumption

The supply power (P) versus frequency ( $f_{MAX}$ ) for MAX 9000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#). The  $I_{CCINT}$  value depends on the switching frequency and the application logic.

The  $I_{CCINT}$  value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$



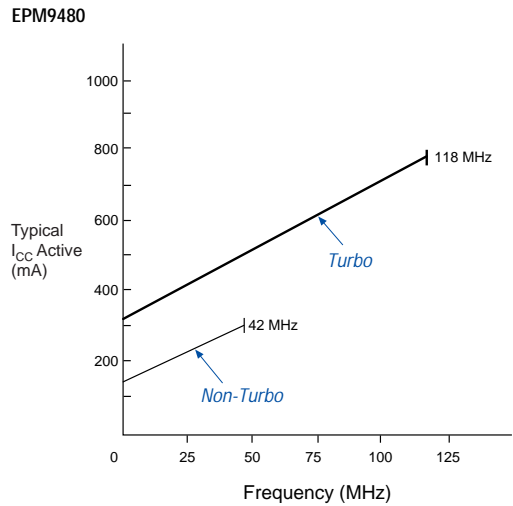
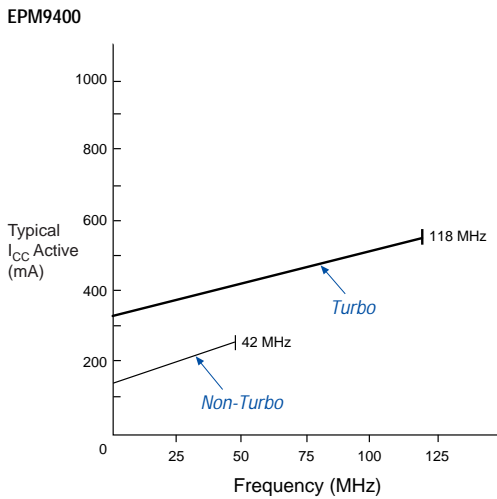
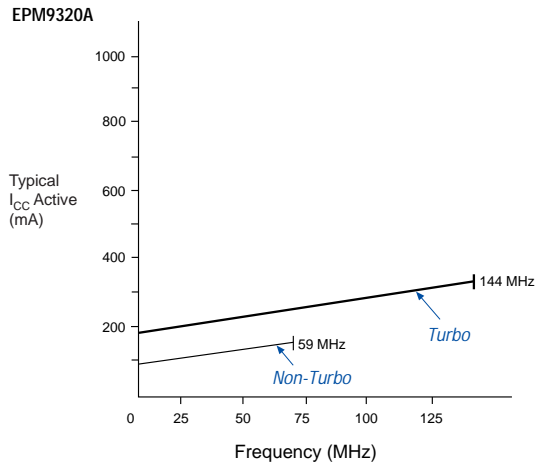
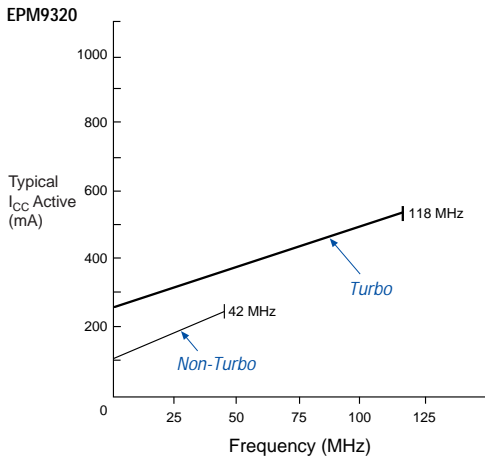
Figure 15.  $I_{CC}$  vs. Frequency for MAX 9000 Devices (Part 1 of 2)

Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA (2)	304-Pin RQFP (2)	356-Pin BGA
DIN1 (GCLK1)	182	210	V10	266	AD13
DIN2 (GCLK2)	183	211	U10	267	AF14
DIN3 (GCLR)	153	187	V17	237	AD1
DIN4 (GOE)	4	234	W2	296	AC24
TCK	78	91	A9	114	A18
TMS	49	68	D6	85	E23
TDI	79	92	C11	115	A13
TDO	108	114	A18	144	D3
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290	A9, A22, A25, A26, B25, B26, D2, E1, E26, F2, G1, G25, G26, H2, J1, J25, J26, K2, L26, M26, N1, N25, P26, R2, T1, U2, U26, V1, V25, W25, Y26, AA2, AB1, AB26, AC26, AE1, AF1, AF2, AF4, AF7, AF20
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217	D26, F1, H1, K26, N26, P1, U1, W26, AE26, AF25, AF26
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279	A1, A2, A21, B1, B10, B24, D1, H26, K1, M25, R1, V26, AA1, AC25, AF5, AF8, AF19

Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA (2)	304-Pin RQFP (2)	356-Pin BGA
No Connect (N.C.)	109	—	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304	B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23
VPP (3)	48	67	C4	75	E25
Total User I/O Pins (4)	153	191	216	216	216

**Notes:**

- (1) All pins not listed are user I/O pins.
- (2) EPM9560A devices are not offered in this package.
- (3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
- (4) The user I/O pin count includes dedicated input pins and all I/O pins.

## Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.5 supersedes information published in previous versions.

### Version 6.5

Version 6.6 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change:

- Added **Tables 7** through **9**.
- Added **“Programming Sequence”** on **page 20** and **“Programming Times”** on **page 20**

### Version 6.4

Version 6.4 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: Updated text on **page 23**.

### Version 6.3

Version 6.3 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: added **Note (7)** to **Table 16**.



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
<http://www.altera.com>  
**Applications Hotline:**  
(800) 800-EPLD  
**Customer Marketing:**  
(408) 544-7104  
**Literature Services:**  
[lit\\_req@altera.com](mailto:lit_req@altera.com)

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