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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	35
Number of Macrocells	560
Number of Gates	12000
Number of I/O	153
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm9560ari208-10

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the ***PCI Local Bus Specification, Revision 2.2***. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-10	-15	-20
EPM9320		✓	✓
EPM9320A	✓		
EPM9400		✓	✓
EPM9480		✓	✓
EPM9560		✓	✓
EPM9560A	✓		

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance *Note (1)*

Application	Macrocells Used	Speed Grade			Units
		-10	-15	-20	
16-bit loadable counter	16	144	118	100	MHz
16-bit up/down counter	16	144	118	100	MHz
16-bit prescaled counter	16	144	118	100	MHz
16-bit address decode	1	5.6 (10)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	7.7 (12.1)	10.9 (18)	16 (26)	ns

Note:

(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

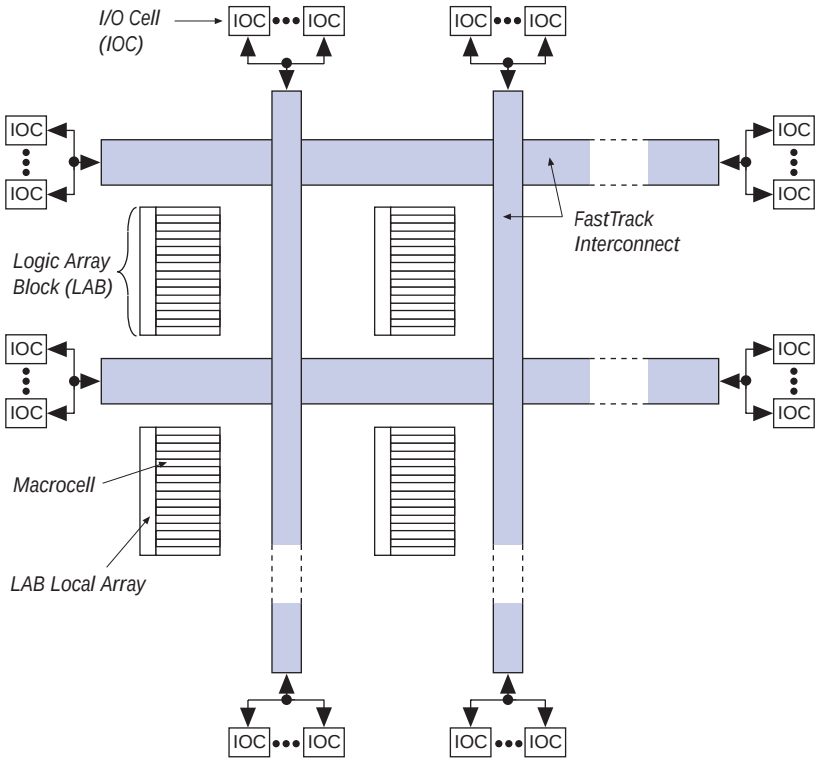
Functional Description

MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram



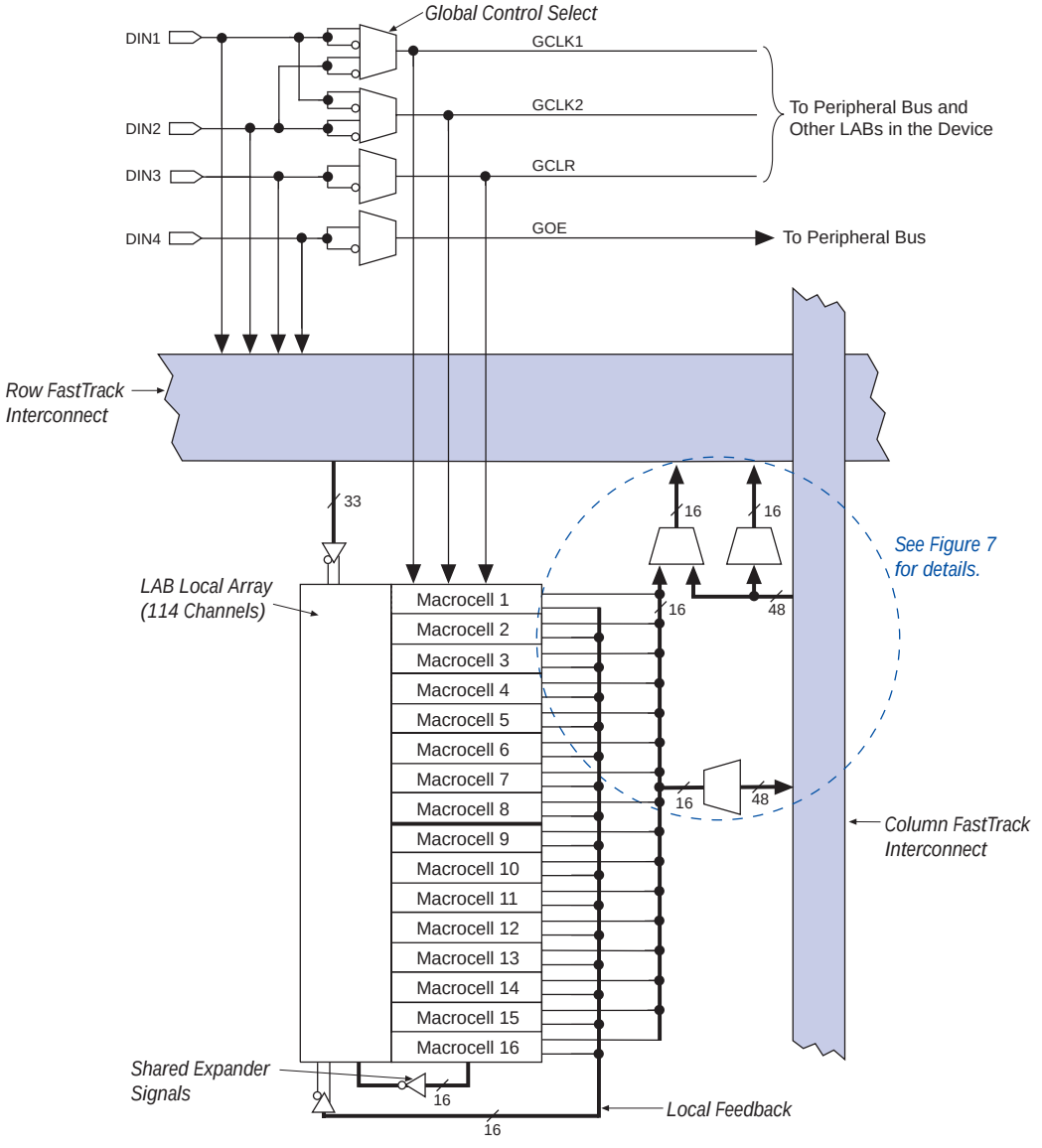
Logic Array Blocks

The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2 on page 7. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

LABs drive the row and column interconnect directly. Each macrocell can drive out of the LAB onto one or both routing resources. Once on the row or column interconnect, signals can traverse to other LABs or to the IOCs.

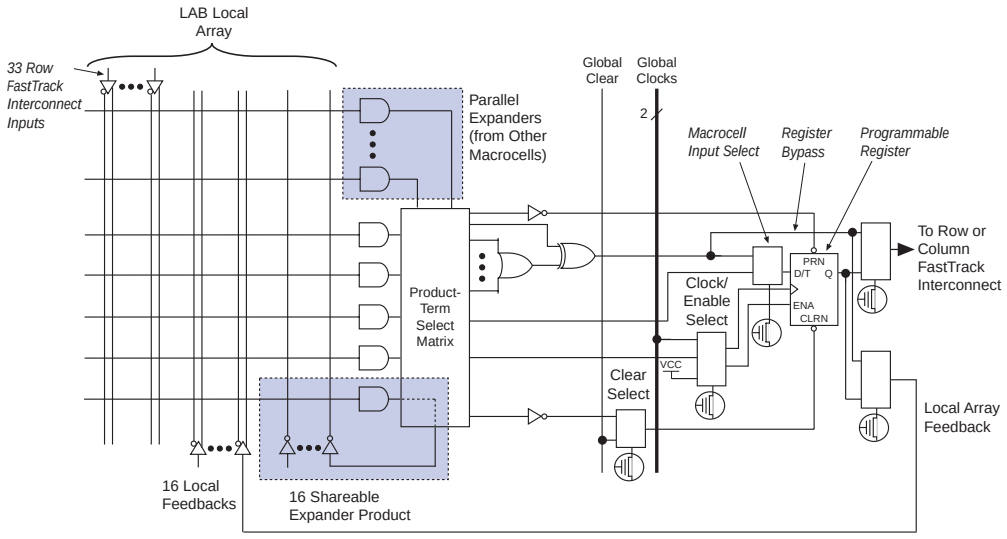
Figure 2. MAX 9000 Logic Array Block



Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

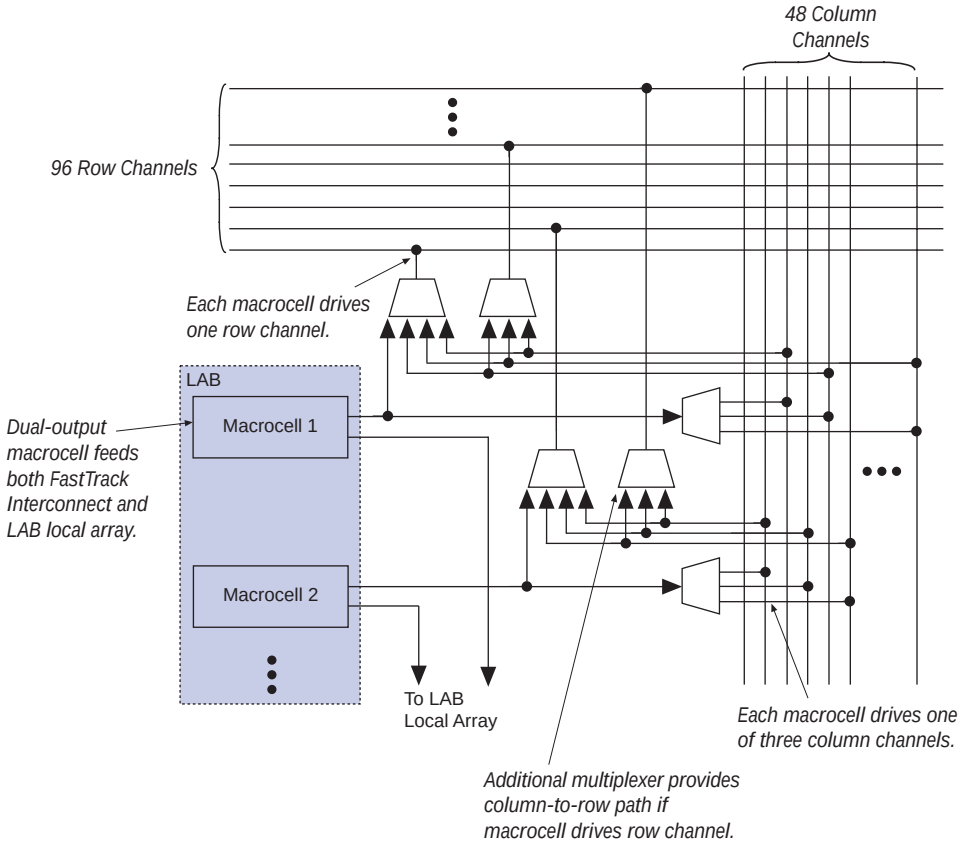
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

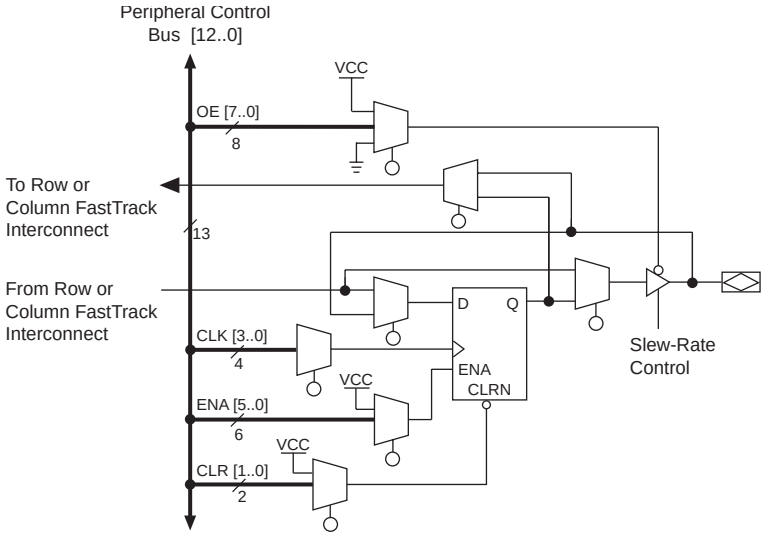
Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I / O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. MAX 9000 LAB Connections to Row & Column Interconnect



Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler optimizes connections to a column channel automatically.

Figure 10. MAX 9000 IOC



I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 on page 18 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 9000 Device

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programming with External Hardware

MAX 9000 devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 9000 device with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers.*

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 9000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 10 describes the JTAG instructions supported by the MAX 9000 family. The pin-out tables starting on page 38 show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 10. MAX 9000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be shifted out of `TDO`. Supported by the EPM9320A, EPM9400, EPM9480, and EPM9560A devices only.
UESCODE	Selects the user electronic signature (UESCODE) register and allows the UESCODE to be shifted out of `TDO` serially. This instruction is supported by MAX 9000A devices only.
ISP Instructions	These instructions are used when programming MAX 9000 devices via the JTAG ports with the BitBlaster or ByteBlasterMV download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format (**.svf**) File via an embedded processor or test equipment.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. Because most logic applications require only a small fraction of all gates to operate at maximum frequency, this feature allows total power dissipation to be reduced by 50% or more.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

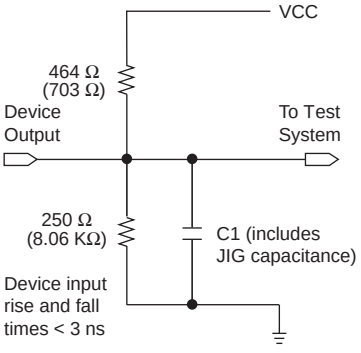
Design Security

All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

Figure 12. MAX 9000 AC Test Conditions



Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V outputs. Numbers without parentheses are for 5.0-V devices or outputs.

Operating Conditions

Tables 14 through 20 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 9000 devices.

Table 14. MAX 9000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
V_{CCISP}	Supply voltage during in-system programming		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Table 15. MAX 9000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during in-system programming		4.75	5.25	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 20. MAX 9000A Device Typical I_{CC} Supply Current Values

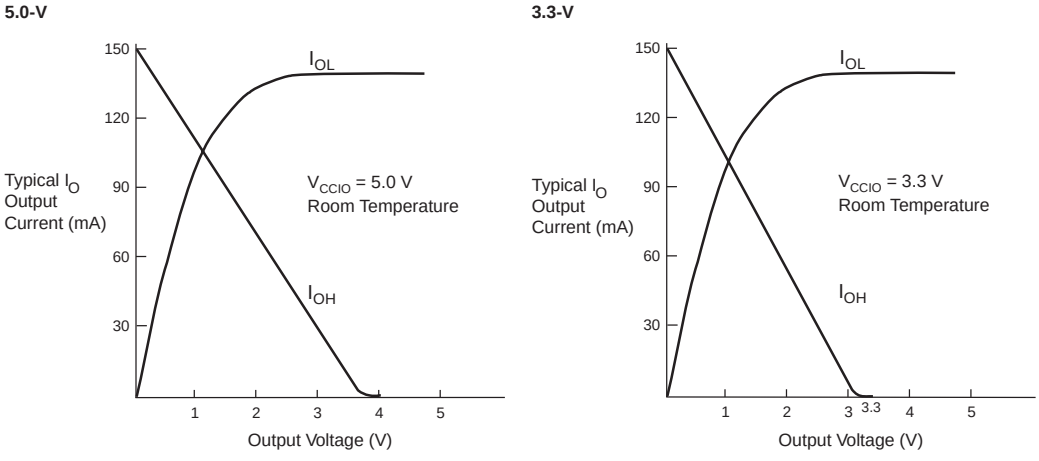
Symbol	Parameter	Conditions	EPM9320A	EPM9560A	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load *(11)*	99	174	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input on I/O pins is –0.5 V and on the four dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 15 on page 27.
(7) During in-system programming, the minimum V_{IH} of the JTAG TCK pin is 3.6 V. The minimum V_{IH} of this pin during JTAG testing remains at 2.0 V. To attain this 3.6-V V_{IH} during programming, the ByteBlaster and ByteBlasterMV download cables must have a 5.0-V V_{CC}.
(8) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to the low-level TTL or CMOS output current.
(9) JTAG pin input leakage is typically –60 µA.
(10) Capacitance is sample-tested only and is measured at 25° C.
(11) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V V_{CCIO}.

Figure 13. Output Drive Characteristics of MAX 9000 Devices *Note (1)*



Note:

(1) Output drive characteristics include the JTAG TDO pin.

Table 23. IOC Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{IODR}	I/O row output data delay			0.2		0.2		1.5	ns
t_{IODC}	I/O column output data delay			0.4		0.2		1.5	ns
t_{IOC}	I/O control delay	*(6)*		0.5		1.0		2.0	ns
t_{IORD}	I/O register clock-to-output delay			0.6		1.0		1.5	ns
t_{IOCOMB}	I/O combinatorial delay			0.2		1.0		1.5	ns
t_{IOSU}	I/O register setup time before clock		2.0		4.0		5.0		ns
t_{IOH}	I/O register hold time after clock		1.0		1.0		1.0		ns
t_{IOCLR}	I/O register clear delay			1.5		3.0		3.0	ns
t_{IOFD}	I/O register feedback delay			0.0		0.0		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay			3.5		4.5		5.5	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay			1.5		2.0		2.5	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		1.8		2.5		2.5	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF		2.3		3.5		3.5	ns
t_{OD3}	Output buffer and pad delay, Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF		8.3		10.0		10.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.5		2.5		2.5	ns
t_{ZX1}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		2.5		2.5		2.5	ns
t_{ZX2}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF		3.0		3.5		3.5	ns
t_{ZX3}	Output buffer enable delay, Slow slew rate = on, V_{CCIO} = 3.3 V or 5.0 V	C1 = 35 pF		9.0		10.0		10.5	ns

Table 24. Interconnect Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LOCAL}	LAB local array delay			0.5		0.5		0.5	ns
t_{ROW}	FastTrack row delay	*(6)*		0.9		1.4		2.0	ns
t_{COL}	FastTrack column delay	*(6)*		0.9		1.7		3.0	ns
t_{DIN_D}	Dedicated input data delay			4.0		4.5		5.0	ns
t_{DIN_CLK}	Dedicated input clock delay			2.7		3.5		4.0	ns
t_{DIN_CLR}	Dedicated input clear delay			4.5		5.0		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register clock delay			2.5		3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

Notes to tables:

(1) These values are specified under the MAX 9000 device recommended operating conditions, shown in Table 15 on page 27.

(2) See *Application Note 77 (Understanding MAX 9000 Timing)* for more information on test conditions for $\mathbf{t_{PD1}}$ and $\mathbf{t_{PD2}}$ delays.

(3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.

(5) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.

(6) The t_{ROW}, t_{COL}, and t_{IOC} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Power Consumption

The supply power (P) versus frequency ($\mathbf{f_{MAX}}$) for MAX 9000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The I_{CCINT} value depends on the switching frequency and the application logic.

The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

Table 28. EPM9480 Dedicated Pin-Outs *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(2)*	48	67
Total User I/O Pins *(3)*	146	175

Notes:

(1) All pins not listed are user I/O pins.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA *(2)*	304-Pin RQFP *(2)*	356-Pin BGA
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304	B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23
VPP *(3)*	48	67	C4	75	E25
Total User I/O Pins *(4)*	153	191	216	216	216

Notes:

(1) All pins not listed are user I/O pins.
(2) EPM9560A devices are not offered in this package.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.5 supersedes information published in previous versions.

Version 6.5

Version 6.6 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change:

- Added Tables 7 through 9.
- Added "Programming Sequence" on page 20 and "Programming Times" on page 20

Version 6.4

Version 6.4 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: Updated text on page 23.

Version 6.3

Version 6.3 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: added Note (7) to Table 16.

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