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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	35
Number of Macrocells	560
Number of Gates	12000
Number of I/O	153
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm9560rc208-20

…and More Features

- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

Table 2. MAX 9000 Package Options & I/O Counts *Note (1)*

Device	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP	356-Pin BGA
EPM9320	60 *(2)*	132	–	168	–	168
EPM9320A	60 *(2)*	132	–	–	–	168
EPM9400	59 *(2)*	139	159	–	–	–
EPM9480	–	146	175	–	–	–
EPM9560	–	153	191	216	216	216
EPM9560A	–	153	191	–	–	216

Notes:

(1) MAX 9000 device package types include plastic J-lead chip carrier (PLCC), power quad flat pack (RQFP), ceramic pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the ***PCI Local Bus Specification, Revision 2.2***. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-10	-15	-20
EPM9320		✓	✓
EPM9320A	✓		
EPM9400		✓	✓
EPM9480		✓	✓
EPM9560		✓	✓
EPM9560A	✓		

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance *Note (1)*

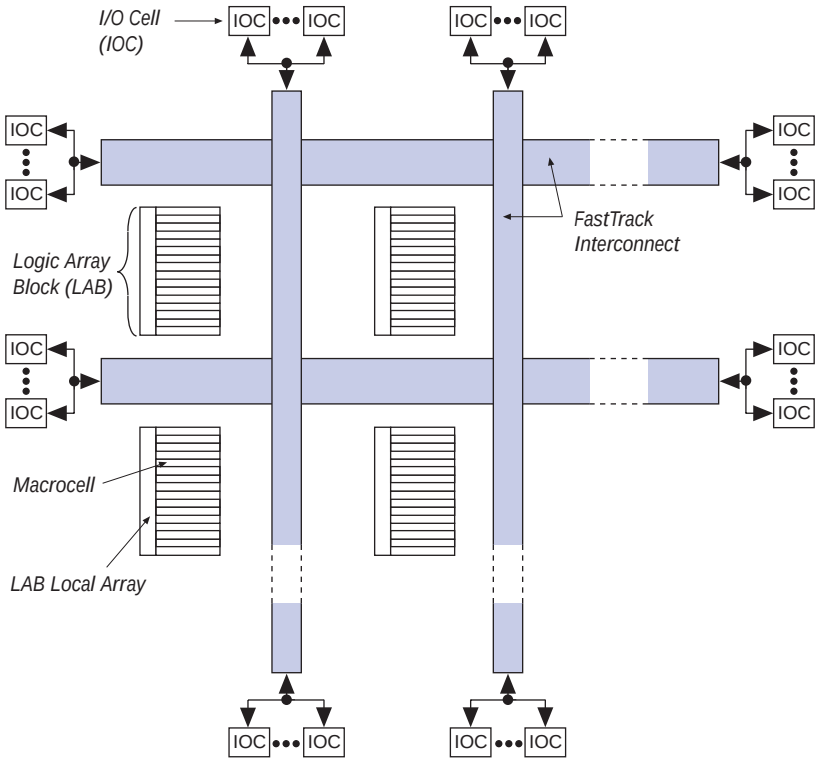
Application	Macrocells Used	Speed Grade			Units
		-10	-15	-20	
16-bit loadable counter	16	144	118	100	MHz
16-bit up/down counter	16	144	118	100	MHz
16-bit prescaled counter	16	144	118	100	MHz
16-bit address decode	1	5.6 (10)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	7.7 (12.1)	10.9 (18)	16 (26)	ns

Note:

(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

Figure 1. MAX 9000 Device Block Diagram



Logic Array Blocks

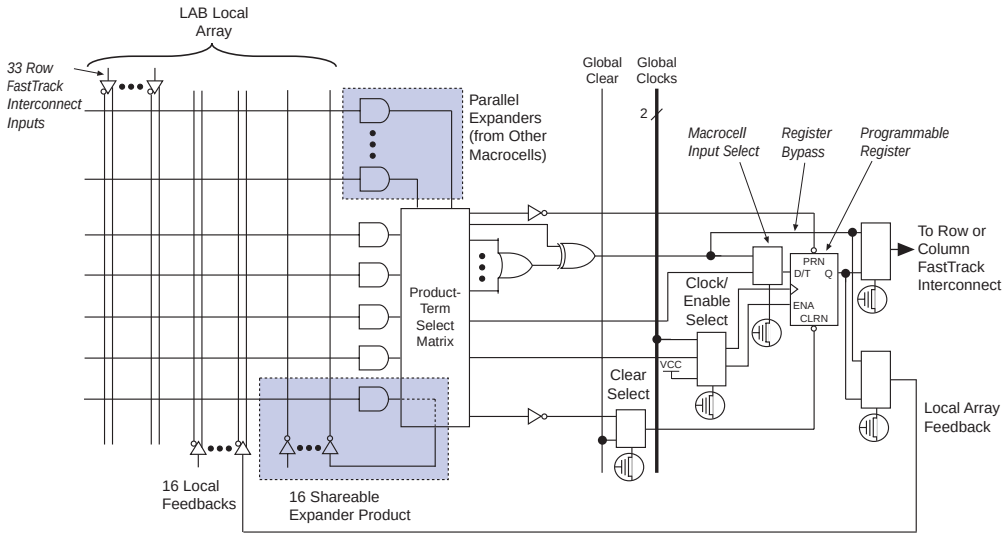
The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2 on page 7. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins (DIN1 and DIN2).

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. MAX 9000 Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.

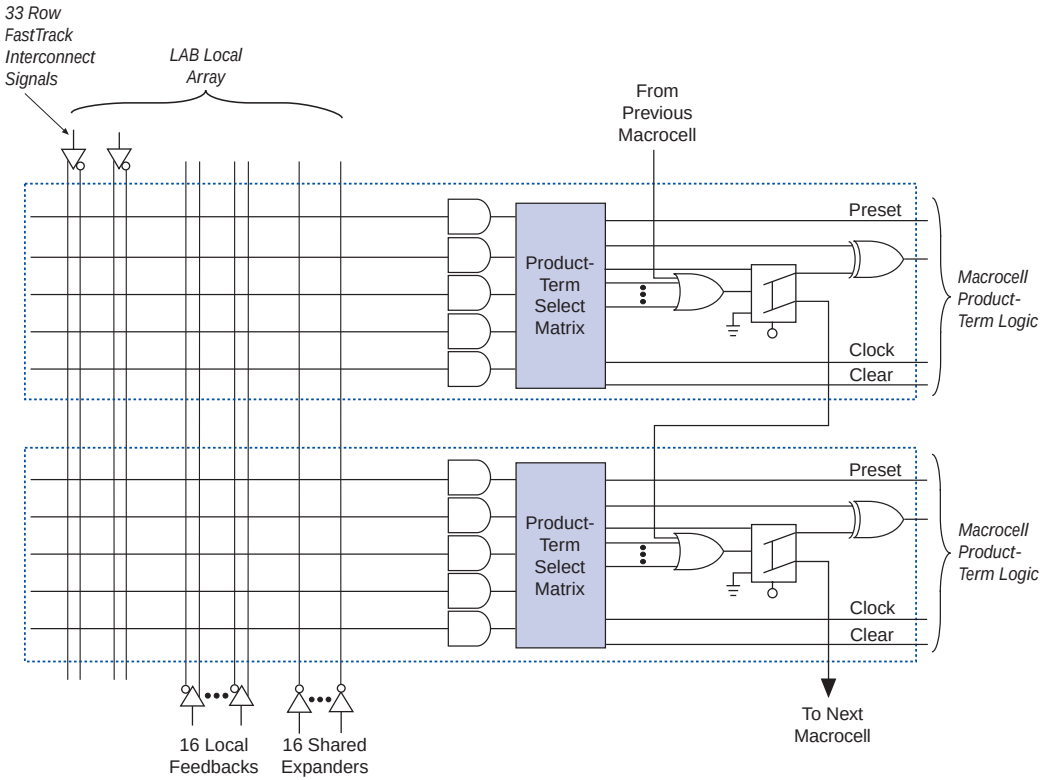
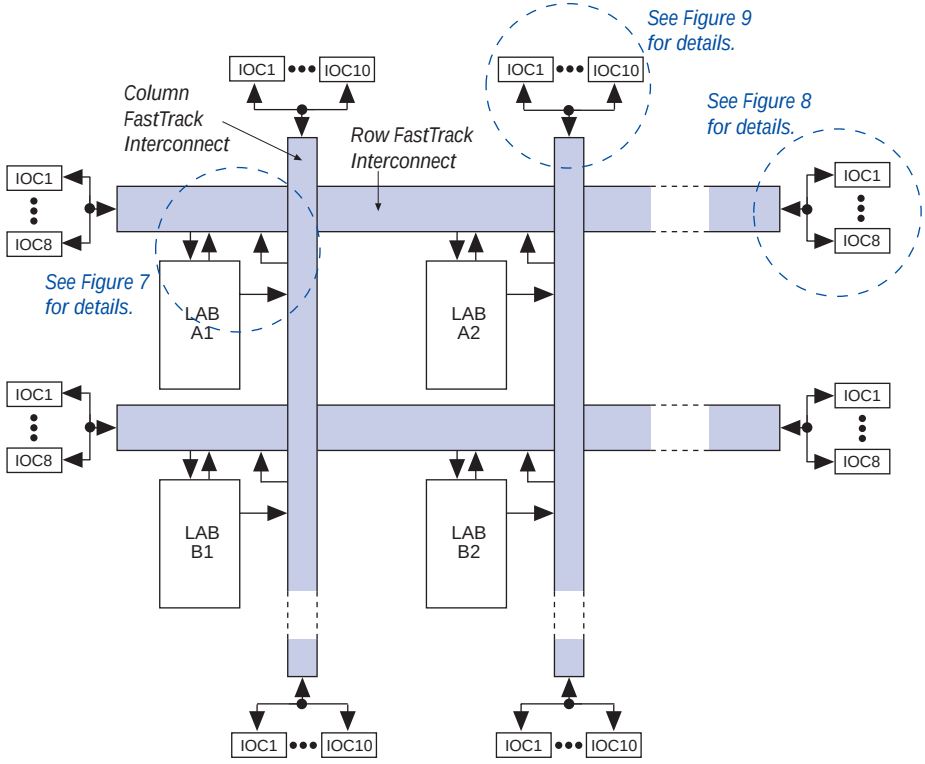


Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

Table 5. MAX 9000 Rows & Columns

Devices	Rows	Columns
EPM9320, EPM9320A	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560, EPM9560A	7	5

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 9000 Device

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The programming times described in Tables 7 through 9 are associated with the worst-case method using the ISP algorithm.

Table 7. MAX 9000 t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM9320 EPM9320A	11.79	2,966,000	0.15	1,806,000
EPM9400	12.00	3,365,000	0.15	2,090,000
EPM9480	12.21	3,764,000	0.15	2,374,000
EPM9560 EPM9560A	12.42	4,164,000	0.15	2,658,000

Tables 8 and 9 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 8. MAX 9000 In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	12.09	12.38	13.27	14.76	17.72	26.62	41.45	71.11	s
EPM9400	12.34	12.67	13.68	15.37	18.73	28.83	45.65	79.30	s
EPM9480	12.59	12.96	14.09	15.98	19.74	31.03	49.85	87.49	s
EPM9560 EPM9560A	12.84	13.26	14.50	16.59	20.75	33.24	54.06	95.70	s

Table 9. MAX 9000 Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	0.33	0.52	1.06	1.96	3.77	9.18	18.21	36.27	s
EPM9400	0.36	0.57	1.20	2.24	4.33	10.60	21.05	41.95	s
EPM9480	0.39	0.63	1.34	2.53	4.90	12.02	23.89	47.63	s
EPM9560 EPM9560A	0.42	0.69	1.48	2.81	5.47	13.44	26.73	53.31	s

The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. Tables 11 and 12 show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

Table 11. MAX 9000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

Table 12. 32-Bit MAX 9000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) *(2)*	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A *(3)*	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A *(3)*	0000	1001 0101 0110 0000	00001101110	1

Notes:

(1) The IDCODE's least significant bit (LSB) is always 1.
(2) The most significant bit (MSB) is on the left.
(3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

Figure 11 shows the timing requirements for the JTAG signals.

Operating Conditions

Tables 14 through 20 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 9000 devices.

Table 14. MAX 9000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
V_{CCISP}	Supply voltage during in-system programming		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Table 15. MAX 9000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during in-system programming		4.75	5.25	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 16. MAX 9000 Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*(7)*	2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(8)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(8)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(8)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(8)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(8)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*		0.2	V
I_I	I/O pin leakage current of dedicated input pins	V_I = –0.5 to 5.5 V *(9)*	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_I = –0.5 to 5.5 V	–40	40	µA

Table 17. MAX 9000 Device Capacitance: EPM9320, EPM9400, EPM9480 & EPM9560 Devices *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		17	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF

Table 18. MAX 9000A Device Capacitance: EPM9320A & EPM9560A Devices *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		16	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF

Table 19. MAX 9000 Device Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load *(11)*	106	132	140	146	mA

Timing Model

The continuous, high-performance FastTrack Interconnect ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

The MAX 9000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell, IOC, and interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the internal timing characteristics tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, see *Application Note 77 (Understanding MAX 9000 Timing)*.

Tables 21 through 24 show timing for MAX 9000 devices.

Table 21. MAX 9000 External Timing Characteristics *Note (1)*

Symbol	Parameter	Conditions		Speed Grade						Unit
				-10		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{PD1}	Row I/O pin input to row I/O pin output	C1 = 35 pF *(2)*			10.0		15.0		20.0	ns
t_{PD2}	Column I/O pin input to column I/O pin output	C1 = 35 pF *(2)*	EPM9320A		10.8					ns
			EPM9320				16.0		23.0	ns
			EPM9400				16.2		23.2	ns
			EPM9480				16.4		23.4	ns
			EPM9560A		11.4					ns
			EPM9560				16.6		23.6	ns
t_{FSU}	Global clock setup time for I/O cell			3.0		5.0		6.0		ns
t_{FH}	Global clock hold time for I/O cell			0.0		0.0		0.0		ns
t_{FCO}	Global clock to I/O cell output delay	C1 = 35 pF		1.0 *(3)*	4.8	1.0 *(3)*	7.0	1.0 *(3)*	8.5	ns
t_{CNT}	Minimum internal global clock period	*(4)*			6.9		8.5		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*		144.9		117.6		100.0		MHz

Notes:
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.
(3) EPM9320A devices are not offered in this package.
(4) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 27. EPM9400 Dedicated Pin-Outs *Note (1)*

Pin Name	84-Pin PLCC *(2)*	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(3)*	55	48	67
Total User I/O Pins *(4)*	59	139	159

Notes:
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 28. EPM9480 Dedicated Pin-Outs *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(2)*	48	67
Total User I/O Pins *(3)*	146	175

Notes:

(1) All pins not listed are user I/O pins.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA *(2)*	304-Pin RQFP *(2)*	356-Pin BGA
DIN1 (GCLK1)	182	210	V10	266	AD13
DIN2 (GCLK2)	183	211	U10	267	AF14
DIN3 (GCLR)	153	187	V17	237	AD1
DIN4 (GOE)	4	234	W2	296	AC24
TCK	78	91	A9	114	A18
TMS	49	68	D6	85	E23
TDI	79	92	C11	115	A13
TDO	108	114	A18	144	D3
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290	A9, A22, A25, A26, B25, B26, D2, E1, E26, F2, G1, G25, G26, H2, J1, J25, J26, K2, L26, M26, N1, N25, P26, R2, T1, U2, U26, V1, V25, W25, Y26, AA2, AB1, AB26, AC26, AE1, AF1, AF2, AF4, AF7, AF20
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217	D26, F1, H1, K26, N26, P1, U1, W26, AE26, AF25, AF26
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279	A1, A2, A21, B1, B10, B24, D1, H26, K1, M25, R1, V26, AA1, AC25, AF5, AF8, AF19

Table 29. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA *(2)*	304-Pin RQFP *(2)*	356-Pin BGA
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304	B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23
VPP *(3)*	48	67	C4	75	E25
Total User I/O Pins *(4)*	153	191	216	216	216

Notes:

(1) All pins not listed are user I/O pins.
(2) EPM9560A devices are not offered in this package.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.5 supersedes information published in previous versions.

Version 6.5

Version 6.6 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change:

- Added Tables 7 through 9.
- Added "Programming Sequence" on page 20 and "Programming Times" on page 20

Version 6.4

Version 6.4 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: Updated text on page 23.

Version 6.3

Version 6.3 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: added Note (7) to Table 16.

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