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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	35
Number of Macrocells	560
Number of Gates	12000
Number of I/O	191
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm9560rc240-15

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2.0.0 and 3.0.0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

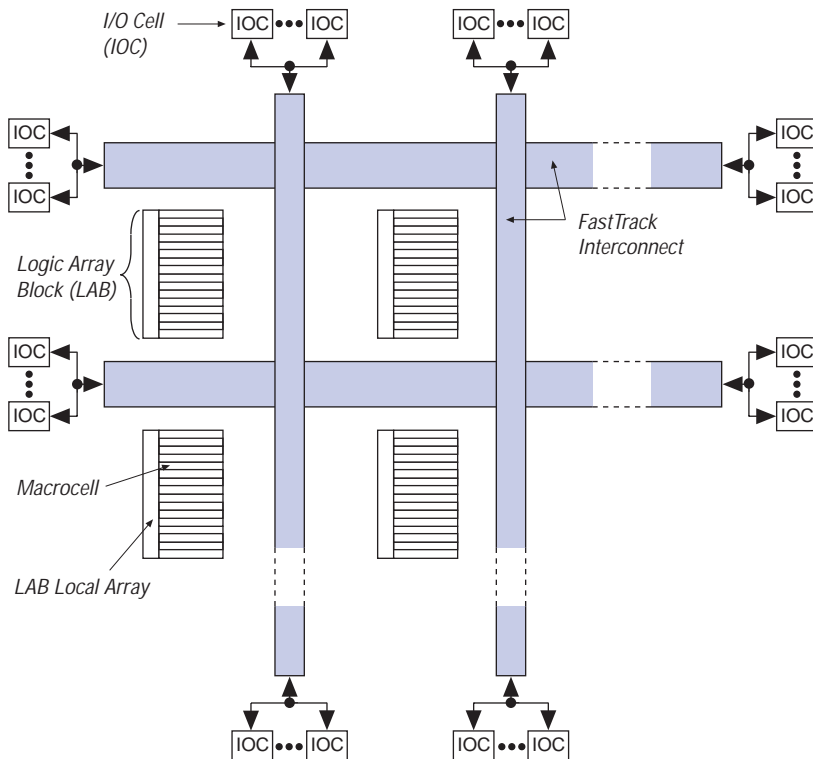
Functional Description

MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram



Logic Array Blocks

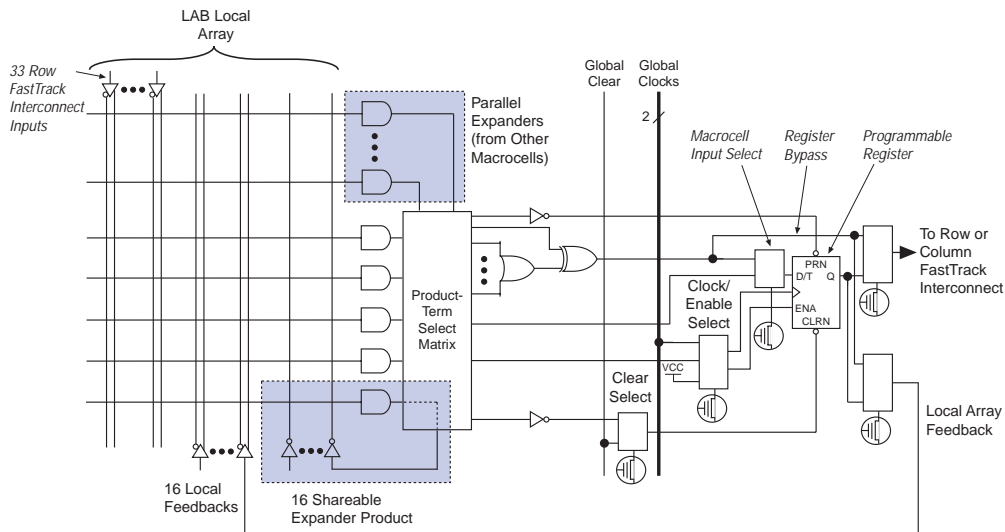
The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in [Figure 2 on page 7](#). Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms (“expanders”) are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See [Figure 3](#).

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins (DIN1 and DIN2).

Each register also supports asynchronous preset and clear functions. As shown in [Figure 3](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Expander Product Terms

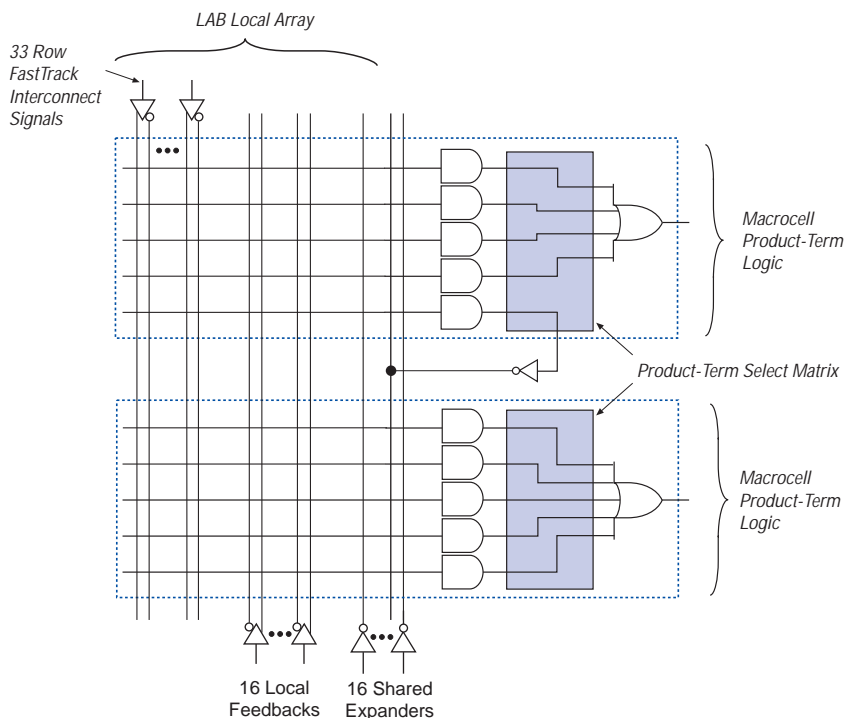
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. MAX 9000 Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.



The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

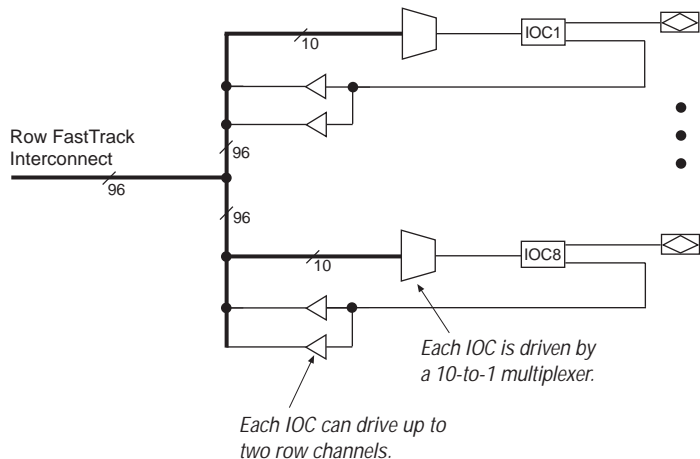
In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. [Figure 6](#) shows the interconnection of four adjacent LABs with row and column interconnects.

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-I/O Cell Connections

Figure 8 illustrates the connections between row interconnect channels and I/O cells. An input signal from an I/O cell can drive two separate row channels. When an I/O cell is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight I/O cells on the periphery of the device.

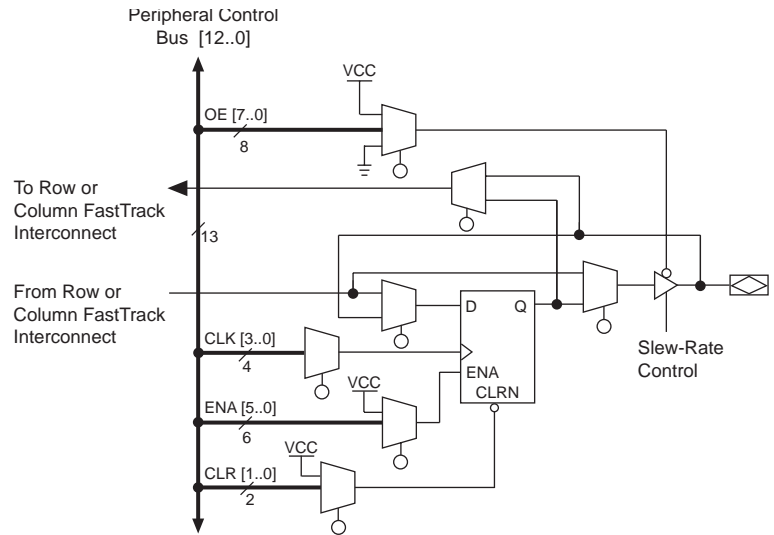
Figure 8. MAX 9000 Row-to-I/O Connections



Column-to-I/O Cell Connections

Each end of a column channel has up to 10 I/O cells (see **Figure 9**). An input signal from an I/O cell can drive two separate column channels. When an I/O cell is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Figure 10. MAX 9000 IOC



I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This “peripheral bus” can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. [Table 6 on page 18](#) shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

In-System Programmability (ISP)

The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} .

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 9000 device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

The programming times described in Tables 7 through 9 are associated with the worst-case method using the ISP algorithm.

Table 7. MAX 9000 t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM9320 EPM9320A	11.79	2,966,000	0.15	1,806,000
EPM9400	12.00	3,365,000	0.15	2,090,000
EPM9480	12.21	3,764,000	0.15	2,374,000
EPM9560 EPM9560A	12.42	4,164,000	0.15	2,658,000

Tables 8 and 9 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 8. MAX 9000 In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	12.09	12.38	13.27	14.76	17.72	26.62	41.45	71.11	s
EPM9400	12.34	12.67	13.68	15.37	18.73	28.83	45.65	79.30	s
EPM9480	12.59	12.96	14.09	15.98	19.74	31.03	49.85	87.49	s
EPM9560 EPM9560A	12.84	13.26	14.50	16.59	20.75	33.24	54.06	95.70	s

Table 9. MAX 9000 Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	0.33	0.52	1.06	1.96	3.77	9.18	18.21	36.27	s
EPM9400	0.36	0.57	1.20	2.24	4.33	10.60	21.05	41.95	s
EPM9480	0.39	0.63	1.34	2.53	4.90	12.02	23.89	47.63	s
EPM9560 EPM9560A	0.42	0.69	1.48	2.81	5.47	13.44	26.73	53.31	s

Programming with External Hardware



MAX 9000 devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the [Altera Programming Hardware Data Sheet](#).

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 9000 device with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see [Programming Hardware Manufacturers](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 9000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. [Table 10](#) describes the JTAG instructions supported by the MAX 9000 family. The pin-out tables starting on [page 38](#) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 10. MAX 9000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be shifted out of TDO. Supported by the EPM9320A, EPM9400, EPM9480, and EPM9560A devices only.
UESCODE	Selects the user electronic signature (UESCODE) register and allows the UESCODE to be shifted out of TDO serially. This instruction is supported by MAX 9000A devices only.
ISP Instructions	These instructions are used when programming MAX 9000 devices via the JTAG ports with the BitBlaster or ByteBlasterMV download cable, or using a Jam File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format (.svf) File via an embedded processor or test equipment.

The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. [Tables 11 and 12](#) show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

Table 11. MAX 9000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

Table 12. 32-Bit MAX 9000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) (2)	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A (3)	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A (3)	0000	1001 0101 0110 0000	00001101110	1

Notes:

- (1) The IDCODE's least significant bit (LSB) is always 1.
- (2) The most significant bit (MSB) is on the left.
- (3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

[Figure 11](#) shows the timing requirements for the JTAG signals.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. Because most logic applications require only a small fraction of all gates to operate at maximum frequency, this feature allows total power dissipation to be reduced by 50% or more.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

Design Security

All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

Figure 12. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V outputs. Numbers without parentheses are for 5.0-V devices or outputs.

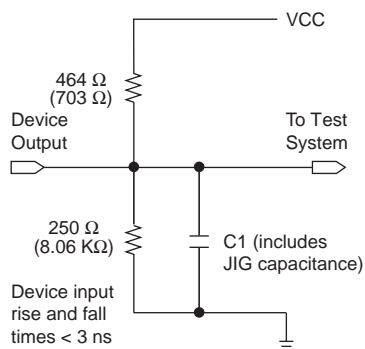


Table 20. MAX 9000A Device Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320A	EPM9560A	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load (11)	99	174	mA

Notes to tables:

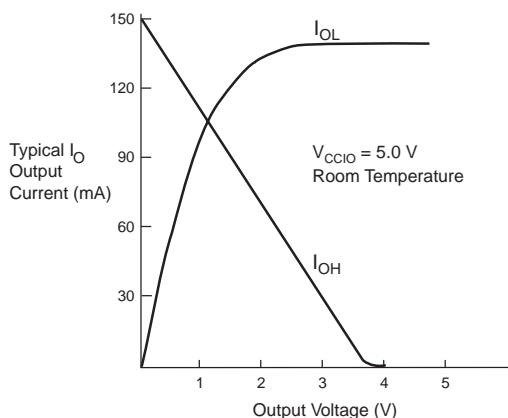
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input on I/O pins is -0.5 V and on the four dedicated input pins is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (3) V_{CC} must rise monotonically.
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Typical values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0$ V.
- (6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 15 on page 27.
- (7) During in-system programming, the minimum V_{IH} of the JTAG TCK pin is 3.6 V. The minimum V_{IH} of this pin during JTAG testing remains at 2.0 V. To attain this 3.6 -V V_{IH} during programming, the ByteBlaster and ByteBlasterMV download cables must have a 5.0 -V V_{CC} .
- (8) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to the low-level TTL or CMOS output current.
- (9) JTAG pin input leakage is typically -60 μA .
- (10) Capacitance is sample-tested only and is measured at 25°C .
- (11) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0°C .

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0 -V and 3.3 -V V_{CCIO} .

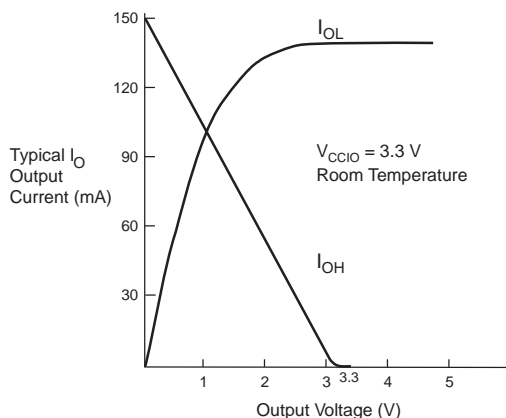
Figure 13. Output Drive Characteristics of MAX 9000 Devices

Note (1)

5.0-V



3.3-V

**Note:**

- (1) Output drive characteristics include the JTAG TDO pin.

Figure 14. MAX 9000 Timing Model

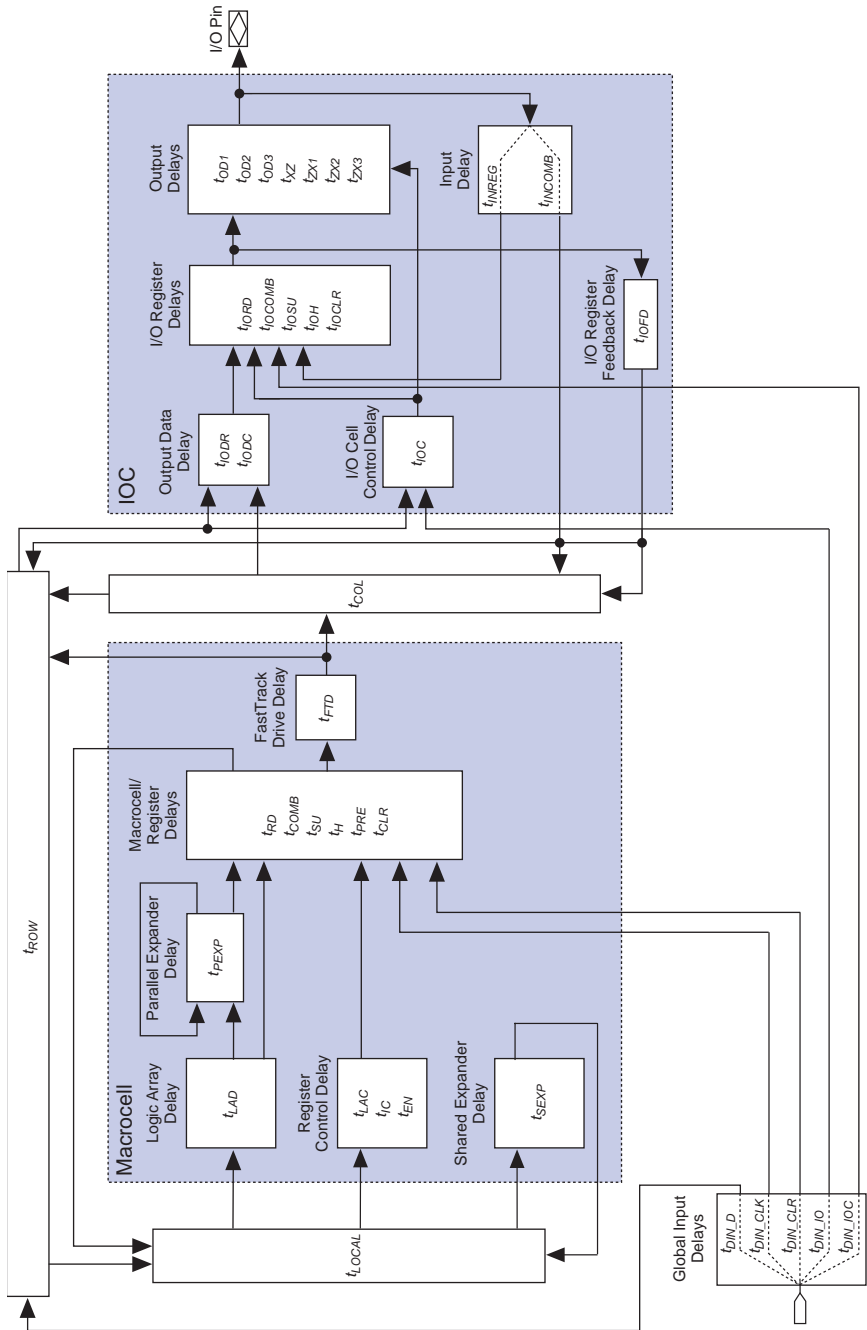


Table 22. MAX 9000 Internal Timing Characteristics *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LAD}	Logic array delay			3.5		4.0		4.5	ns
t_{LAC}	Logic control array delay			3.5		4.0		4.5	ns
t_{IC}	Array clock delay			3.5		4.0		4.5	ns
t_{EN}	Register enable time			3.5		4.0		4.5	ns
t_{SEXP}	Shared expander delay			3.5		5.0		7.5	ns
t_{PEXP}	Parallel expander delay			0.5		1.0		2.0	ns
t_{RD}	Register delay			0.5		1.0		1.0	ns
t_{COMB}	Combinatorial delay			0.4		1.0		1.0	ns
t_{SU}	Register setup time		2.4		3.0		4.0		ns
t_H	Register hold time		2.0		3.5		4.5		ns
t_{PRE}	Register preset time			3.5		4.0		4.5	ns
t_{CLR}	Register clear time			3.7		4.0		4.5	ns
t_{FTD}	FastTrack drive delay			0.5		1.0		2.0	ns
t_{LPA}	Low-power adder	(5)		10.0		15.0		20.0	ns

The parameters in this equation are shown below:

- MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
 MC_{DEV} = Number of macrocells in the device
 MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File
 f_{MAX} = Highest clock frequency to the device
 log_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in [Table 25](#)

Table 25. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9320A	0.56	0.31	0.024
EPM9400	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052
EPM9560A	0.56	0.31	0.024

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} values should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions. [Figure 15](#) shows typical supply current versus frequency for MAX 9000 devices.

