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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	35
Number of Macrocells	560
Number of Gates	12000
Number of I/O	191
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm9560rc240-15yy

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the **PCI Local Bus Specification, Revision 2.2**. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-10	-15	-20
EPM9320		✓	✓
EPM9320A	✓		
EPM9400		✓	✓
EPM9480		✓	✓
EPM9560		✓	✓
EPM9560A	✓		

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance Note (1)

Application	Macrocells Used	Speed Grade			Units
		-10	-15	-20	
16-bit loadable counter	16	144	118	100	MHz
16-bit up/down counter	16	144	118	100	MHz
16-bit prescaled counter	16	144	118	100	MHz
16-bit address decode	1	5.6 (10)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	7.7 (12.1)	10.9 (18)	16 (26)	ns

Note:

- (1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2.0.0 and 3.0.0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.



Functional Description

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins (DIN1 and DIN2).

Each register also supports asynchronous preset and clear functions. As shown in [Figure 3](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Expander Product Terms

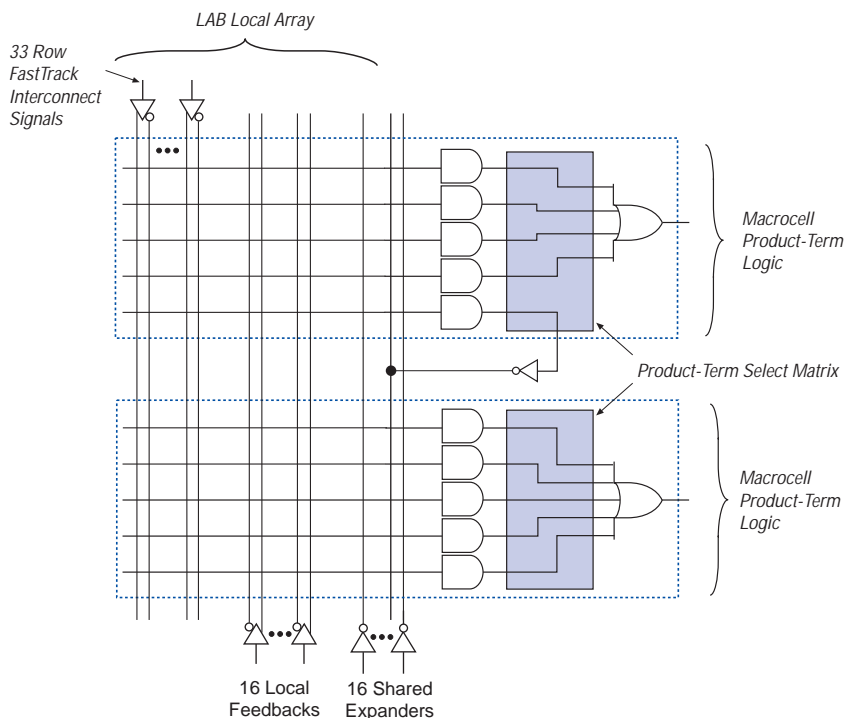
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. MAX 9000 Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.

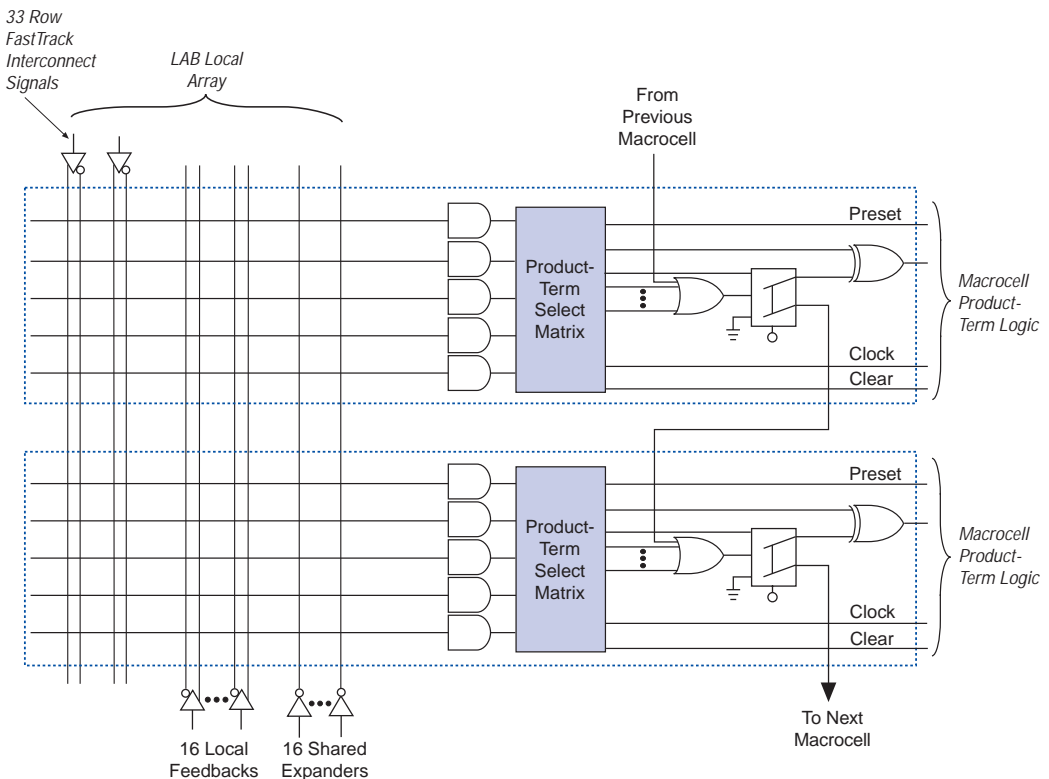


Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. **Figure 5** shows how parallel expanders can feed the neighboring macrocell.

Figure 5. MAX 9000 Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

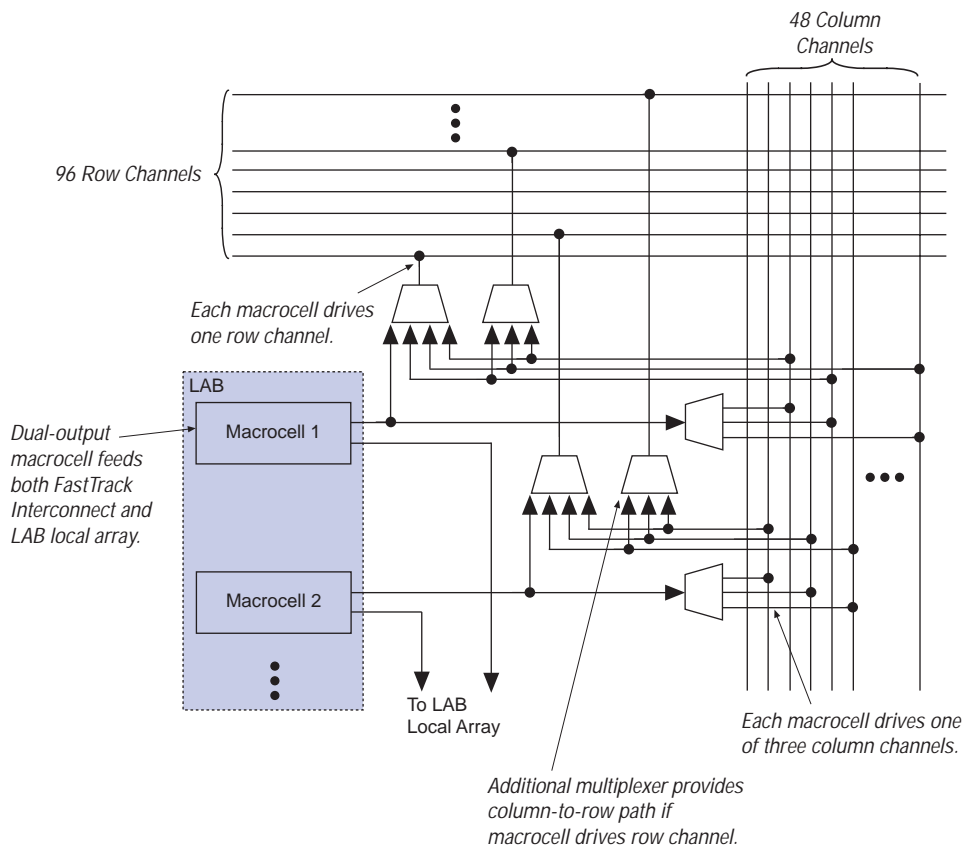
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. [Figure 6](#) shows the interconnection of four adjacent LABs with row and column interconnects.

Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. MAX 9000 LAB Connections to Row & Column Interconnect



Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler optimizes connections to a column channel automatically.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 9000 Device

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The programming times described in [Tables 7 through 9](#) are associated with the worst-case method using the ISP algorithm.

Table 7. MAX 9000 t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM9320 EPM9320A	11.79	2,966,000	0.15	1,806,000
EPM9400	12.00	3,365,000	0.15	2,090,000
EPM9480	12.21	3,764,000	0.15	2,374,000
EPM9560 EPM9560A	12.42	4,164,000	0.15	2,658,000

[Tables 8 and 9](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 8. MAX 9000 In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	12.09	12.38	13.27	14.76	17.72	26.62	41.45	71.11	s
EPM9400	12.34	12.67	13.68	15.37	18.73	28.83	45.65	79.30	s
EPM9480	12.59	12.96	14.09	15.98	19.74	31.03	49.85	87.49	s
EPM9560 EPM9560A	12.84	13.26	14.50	16.59	20.75	33.24	54.06	95.70	s

Table 9. MAX 9000 Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM9320 EPM9320A	0.33	0.52	1.06	1.96	3.77	9.18	18.21	36.27	s
EPM9400	0.36	0.57	1.20	2.24	4.33	10.60	21.05	41.95	s
EPM9480	0.39	0.63	1.34	2.53	4.90	12.02	23.89	47.63	s
EPM9560 EPM9560A	0.42	0.69	1.48	2.81	5.47	13.44	26.73	53.31	s

The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. [Tables 11 and 12](#) show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

Table 11. MAX 9000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

Table 12. 32-Bit MAX 9000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) (2)	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A (3)	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A (3)	0000	1001 0101 0110 0000	00001101110	1

Notes:

- (1) The IDCODE's least significant bit (LSB) is always 1.
- (2) The most significant bit (MSB) is on the left.
- (3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

[Figure 11](#) shows the timing requirements for the JTAG signals.

Figure 11. MAX 9000 JTAG Waveforms

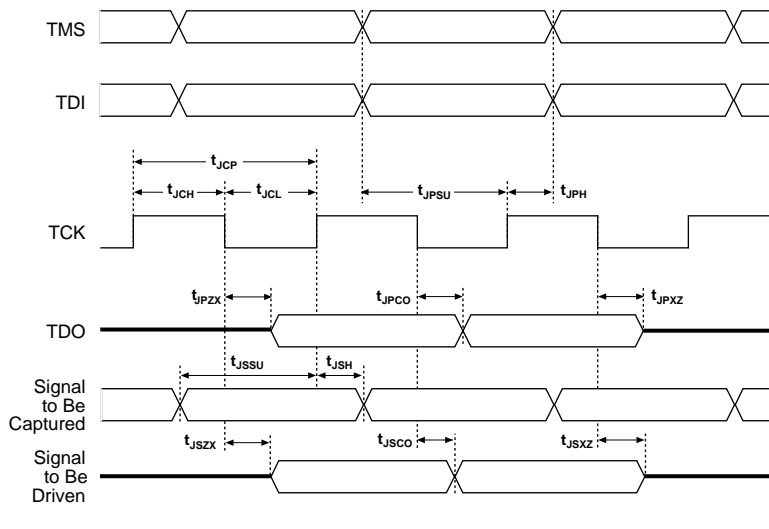


Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

Table 13. JTAG Timing Parameters & Values for MAX 9000 Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns



For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Figure 14. MAX 9000 Timing Model

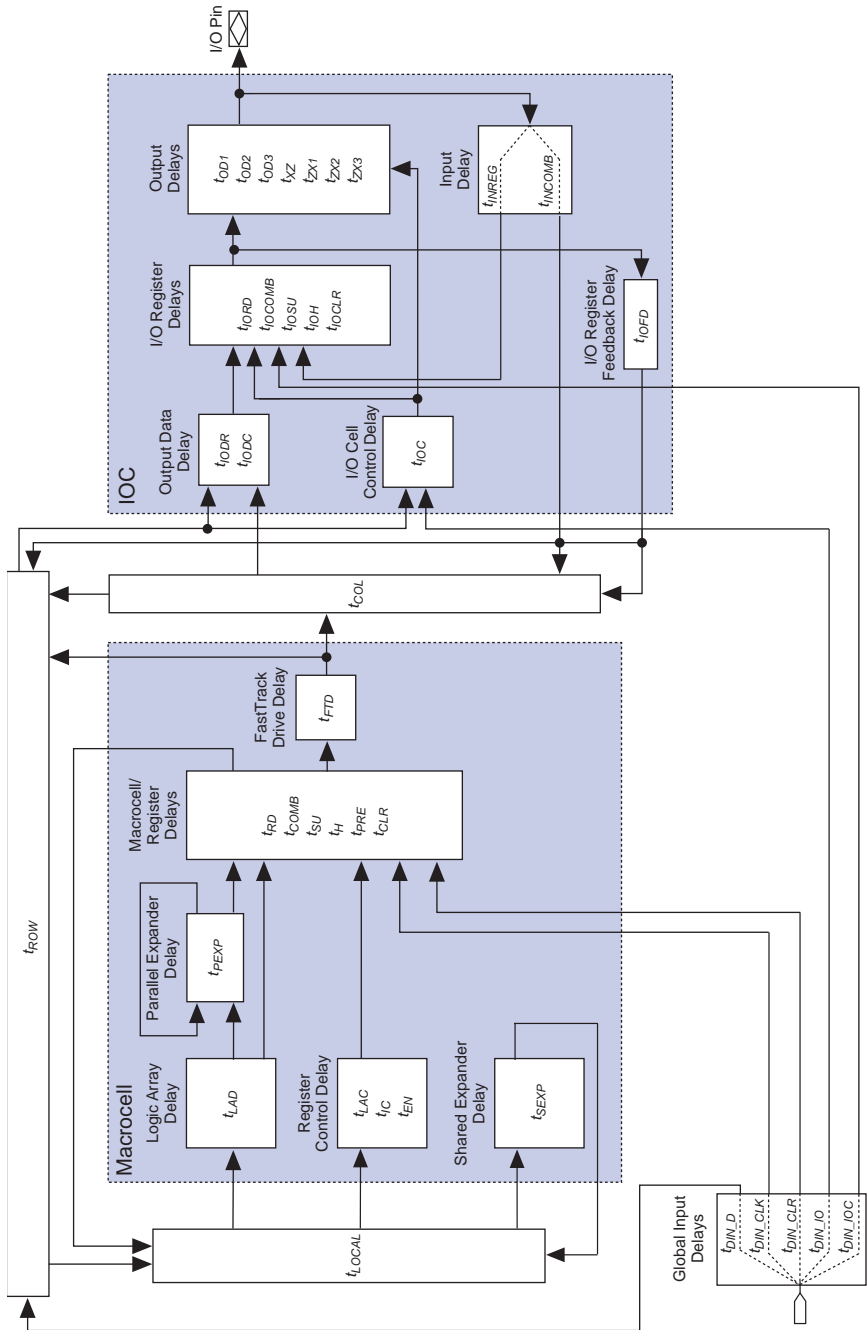


Table 22. MAX 9000 Internal Timing Characteristics *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LAD}	Logic array delay			3.5		4.0		4.5	ns
t_{LAC}	Logic control array delay			3.5		4.0		4.5	ns
t_{IC}	Array clock delay			3.5		4.0		4.5	ns
t_{EN}	Register enable time			3.5		4.0		4.5	ns
t_{SEXP}	Shared expander delay			3.5		5.0		7.5	ns
t_{PEXP}	Parallel expander delay			0.5		1.0		2.0	ns
t_{RD}	Register delay			0.5		1.0		1.0	ns
t_{COMB}	Combinatorial delay			0.4		1.0		1.0	ns
t_{SU}	Register setup time		2.4		3.0		4.0		ns
t_H	Register hold time		2.0		3.5		4.5		ns
t_{PRE}	Register preset time			3.5		4.0		4.5	ns
t_{CLR}	Register clear time			3.7		4.0		4.5	ns
t_{FTD}	FastTrack drive delay			0.5		1.0		2.0	ns
t_{LPA}	Low-power adder	(5)		10.0		15.0		20.0	ns

Table 24. Interconnect Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LOCAL}	LAB local array delay			0.5		0.5		0.5	ns
t_{ROW}	FastTrack row delay	(6)		0.9		1.4		2.0	ns
t_{COL}	FastTrack column delay	(6)		0.9		1.7		3.0	ns
t_{DIN_D}	Dedicated input data delay			4.0		4.5		5.0	ns
t_{DIN_CLK}	Dedicated input clock delay			2.7		3.5		4.0	ns
t_{DIN_CLR}	Dedicated input clear delay			4.5		5.0		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register clock delay			2.5		3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

Notes to tables:

- (1) These values are specified under the MAX 9000 device recommended operating conditions, shown in [Table 15 on page 27](#).
- (2) See [Application Note 77 \(Understanding MAX 9000 Timing\)](#) for more information on test conditions for t_{PD1} and t_{PD2} delays.
- (3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.
- (4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
- (5) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.
- (6) The t_{ROW} , t_{COL} , and t_{IOC} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Power Consumption

The supply power (P) versus frequency (f_{MAX}) for MAX 9000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#). The I_{CCINT} value depends on the switching frequency and the application logic.

The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \log_{LC})$$

The parameters in this equation are shown below:

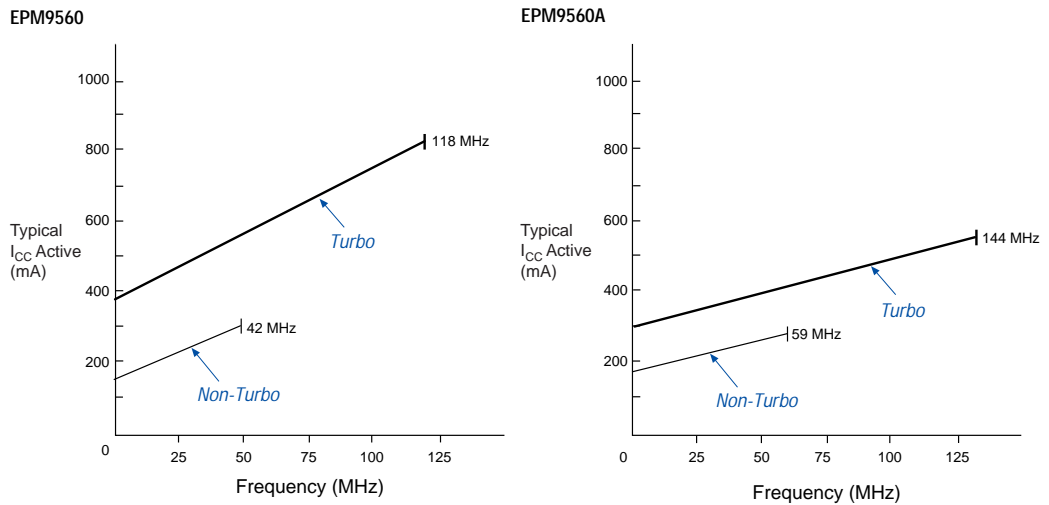
- MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
 MC_{DEV} = Number of macrocells in the device
 MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File
 f_{MAX} = Highest clock frequency to the device
 log_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 25

Table 25. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9320A	0.56	0.31	0.024
EPM9400	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052
EPM9560A	0.56	0.31	0.024

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} values should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions. Figure 15 shows typical supply current versus frequency for MAX 9000 devices.

Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices (Part 2 of 2)



Device
Pin-Outs

Tables 26 through 29 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2) Note (1)				
Pin Name	84-Pin PLCC (2)	208-Pin RQFP	280-Pin PGA (3)	356-Pin BGA
DIN1 (GCLK1)	1	182	V10	AD13
DIN2 (GCLK2)	84	183	U10	AF14
DIN3 (GCLR)	13	153	V17	AD1
DIN4 (GOE)	72	4	W2	AC24
TCK	43	78	A9	A18
TMS	55	49	D6	E23
TDI	42	79	C11	A13
TDO	30	108	A18	D3

Notes:

- (1) All pins not listed are user I/O pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. See [Application Note 74 \(Evaluating Power for Altera Devices\)](#).
- (3) EPM9320A devices are not offered in this package.
- (4) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
- (5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 27. EPM9400 Dedicated Pin-Outs *Note (1)*

Pin Name	84-Pin PLCC (2)	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	—	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP (3)	55	48	67
Total User I/O Pins (4)	59	139	159

Notes:

- (1) All pins not listed are user I/O pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. See [Application Note 74 \(Evaluating Power for Altera Devices\)](#) for more information.
- (3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
- (4) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 28. EPM9480 Dedicated Pin-Outs *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP (2)	48	67
Total User I/O Pins (3)	146	175

Notes:

- (1) All pins not listed are user I/O pins.
- (2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
- (3) The user I/O pin count includes dedicated input pins and all I/O pins.

Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.5 supersedes information published in previous versions.

Version 6.5

Version 6.6 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change:

- Added **Tables 7 through 9**.
- Added **“Programming Sequence” on page 20** and **“Programming Times” on page 20**

Version 6.4

Version 6.4 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: Updated text on **page 23**.

Version 6.3

Version 6.3 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: added **Note (7)** to **Table 16**.



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