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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	35
Number of Macrocells	560
Number of Gates	12000
Number of I/O	191
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm9560rc240-20

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 devices offer the MultiVolt feature, which allows output drivers to be set for either 3.3-V or 5.0-V operation in mixed-voltage systems.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins (`DIN1` and `DIN2`).

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (`DIN3`). The global clear can be programmed for active-high or active-low operation.

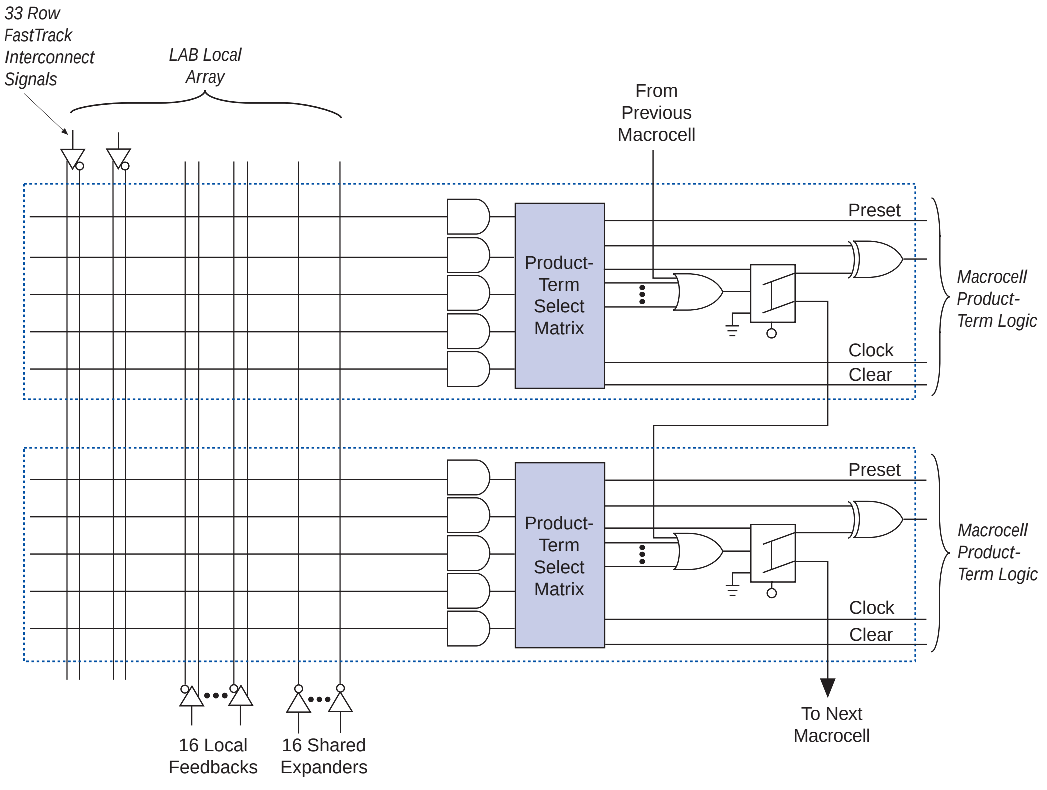
All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. MAX 9000 Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



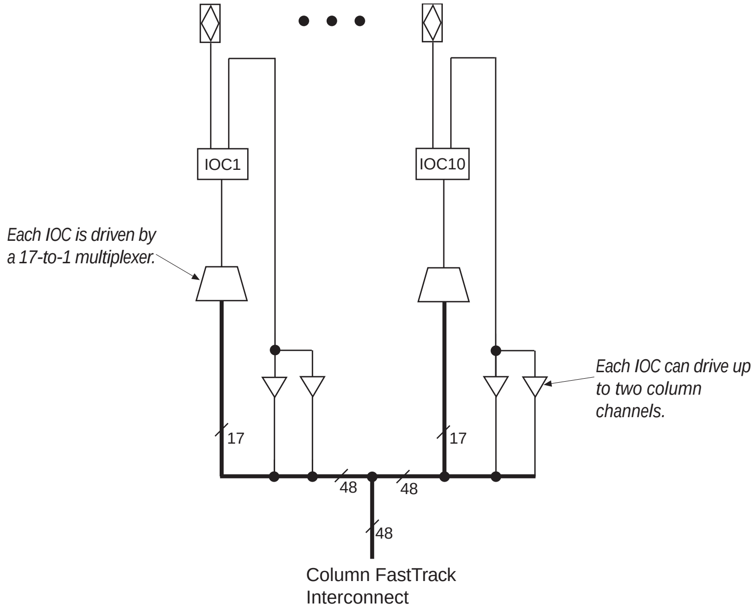
The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

Figure 9. MAX 9000 Column-to-IOC Connections



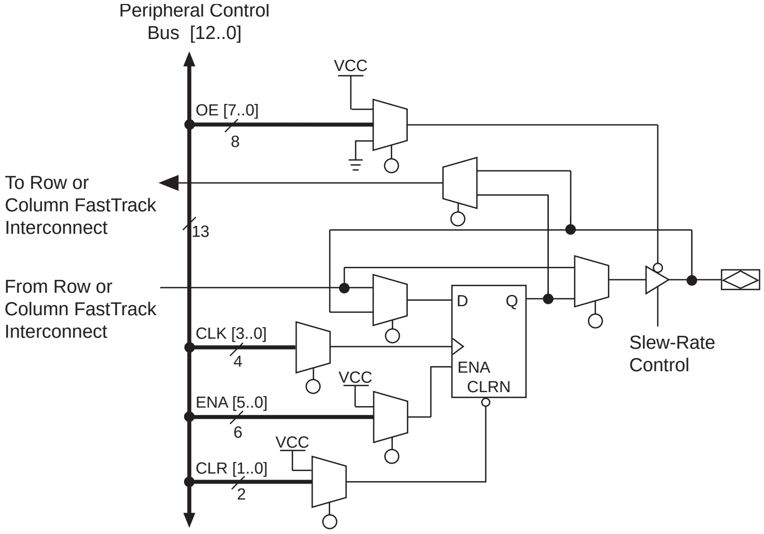
Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect (see Figure 2 on page 7).

I/O Cells

Figure 10 shows the IOC block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

Figure 10. MAX 9000 IOC



I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This “peripheral bus” can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 on page 18 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis. The slew rate control affects both rising and falling edges of the output signals.

Table 6. Peripheral Bus Sources

Peripheral Control Signal	Source			
	EPM9320 EPM9320A	EPM9400	EPM9480	EPM9560 EPM9560A
OE0/ENA0	Row C	Row E	Row F	Row G
OE1/ENA1	Row B	Row E	Row F	Row F
OE2/ENA2	Row A	Row E	Row E	Row E
OE3/ENA3	Row B	Row B	Row B	Row B
OE4/ENA4	Row A	Row A	Row A	Row A
OE5	Row D	Row D	Row D	Row D
OE6	Row C	Row C	Row C	Row C
OE7/CLR1	Row B/GOE	Row B/GOE	Row B/GOE	Row B/GOE
CLR0/ENA5	Row A/GCLR	Row A/GCLR	Row A/GCLR	Row A/GCLR
CLK0	GCLK1	GCLK1	GCLK1	GCLK1
CLK1	GCLK2	GCLK2	GCLK2	GCLK2
CLK2	Row D	Row D	Row D	Row D
CLK3	Row C	Row C	Row C	Row C

Output Configuration

The MAX 9000 device architecture supports the MultiVolt I/O interface feature, which allows MAX 9000 devices to interface with systems of differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

In-System Programma-bility (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an “F” suffix in the ordering code.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 9000 device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 9000 Device

The time required to program a single MAX 9000 device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:
- t_{PROG} = Programming time
- t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
- $Cycle_{PTCK}$ = Number of TCK cycles to program a device
- f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 9000 device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:
- t_{VER} = Verify time
- t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
- $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. Tables 11 and 12 show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

Table 11. MAX 9000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

Table 12. 32-Bit MAX 9000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) *(2)*	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A *(3)*	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A *(3)*	0000	1001 0101 0110 0000	00001101110	1

Notes:

(1) The IDCODE's least significant bit (LSB) is always 1.

(2) The most significant bit (MSB) is on the left.

(3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

Figure 11 shows the timing requirements for the JTAG signals.

Figure 11. MAX 9000 JTAG Waveforms

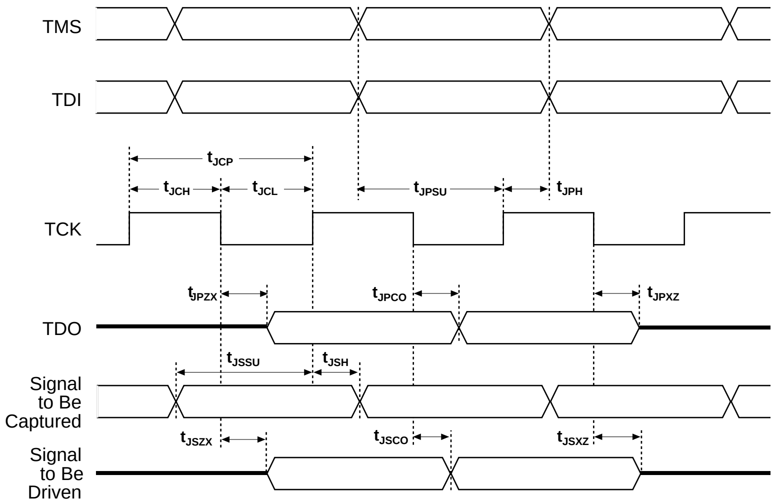


Table 13 shows the JTAG timing parameters and values for MAX 9000 devices.

Table 13. JTAG Timing Parameters & Values for MAX 9000 Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

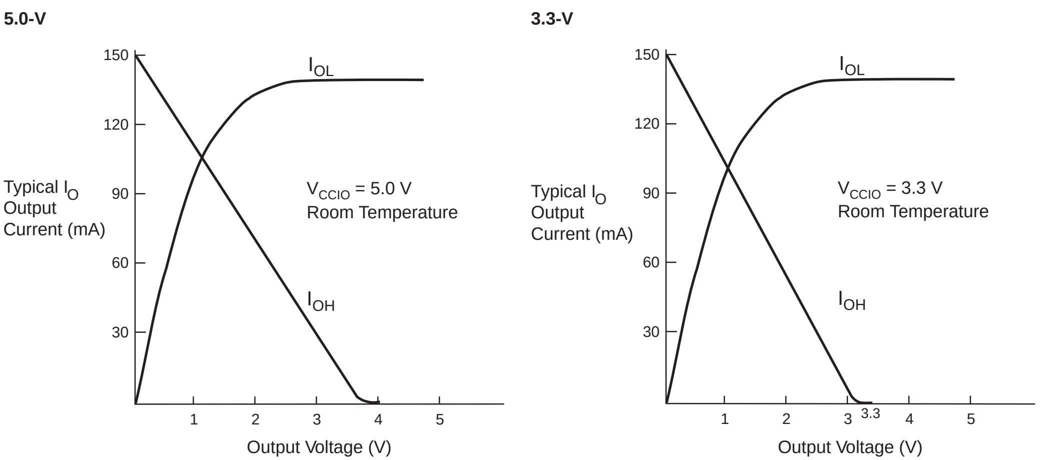
Table 20. MAX 9000A Device Typical I_{CC} Supply Current Values					
Symbol	**Parameter**	**Conditions**	**EPM9320A**	**EPM9560A**	**Unit**
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load *(11)*	99	174	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input on I/O pins is –0.5 V and on the four dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 15 on page 27.
(7) During in-system programming, the minimum V_{IH} of the JTAG TCK pin is 3.6 V. The minimum V_{IH} of this pin during JTAG testing remains at 2.0 V. To attain this 3.6-V V_{IH} during programming, the ByteBlaster and ByteBlasterMV download cables must have a 5.0-V V_{CC}.
(8) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to the low-level TTL or CMOS output current.
(9) JTAG pin input leakage is typically –60 μA.
(10) Capacitance is sample-tested only and is measured at 25° C.
(11) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V V_{CCIO}.

Figure 13. Output Drive Characteristics of MAX 9000 Devices *Note (1)*



Note:

(1) Output drive characteristics include the JTAG TDO pin.

Tables 21 through 24 show timing for MAX 9000 devices.

Table 21. MAX 9000 External Timing Characteristics *Note (1)*

Symbol	Parameter	Conditions		Speed Grade						Unit
				-10		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{PD1}	Row I/O pin input to row I/O pin output	C1 = 35 pF *(2)*			10.0		15.0		20.0	ns
t_{PD2}	Column I/O pin input to column I/O pin output	C1 = 35 pF *(2)*	EPM9320A		10.8					ns
			EPM9320				16.0		23.0	ns
			EPM9400				16.2		23.2	ns
			EPM9480				16.4		23.4	ns
			EPM9560A		11.4					ns
			EPM9560				16.6		23.6	ns
t_{FSU}	Global clock setup time for I/O cell			3.0		5.0		6.0		ns
t_{FH}	Global clock hold time for I/O cell			0.0		0.0		0.0		ns
t_{FCO}	Global clock to I/O cell output delay	C1 = 35 pF		1.0 *(3)*	4.8	1.0 *(3)*	7.0	1.0 *(3)*	8.5	ns
t_{CNT}	Minimum internal global clock period	*(4)*			6.9		8.5		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*		144.9		117.6		100.0		MHz

Table 22. MAX 9000 Internal Timing Characteristics *Note (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			-10		**-15**		**-20**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LAD}	Logic array delay			3.5		4.0		4.5	ns
t_{LAC}	Logic control array delay			3.5		4.0		4.5	ns
t_{IC}	Array clock delay			3.5		4.0		4.5	ns
t_{EN}	Register enable time			3.5		4.0		4.5	ns
t_{SEXP}	Shared expander delay			3.5		5.0		7.5	ns
t_{PEXP}	Parallel expander delay			0.5		1.0		2.0	ns
t_{RD}	Register delay			0.5		1.0		1.0	ns
t_{COMB}	Combinatorial delay			0.4		1.0		1.0	ns
t_{SU}	Register setup time		2.4		3.0		4.0		ns
t_{H}	Register hold time		2.0		3.5		4.5		ns
t_{PRE}	Register preset time			3.5		4.0		4.5	ns
t_{CLR}	Register clear time			3.7		4.0		4.5	ns
t_{FTD}	FastTrack drive delay			0.5		1.0		2.0	ns
t_{LPA}	Low-power adder	*(5)*		10.0		15.0		20.0	ns

The parameters in this equation are shown below:

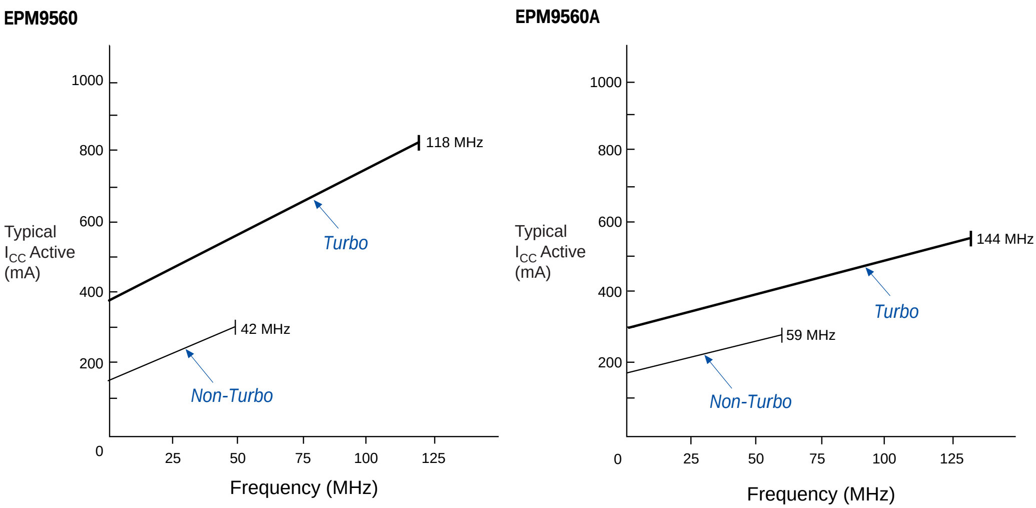
MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 25

Table 25. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9320A	0.56	0.31	0.024
EPM9400	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052
EPM9560A	0.56	0.31	0.024

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} values should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions. Figure 15 shows typical supply current versus frequency for MAX 9000 devices.

Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices (Part 2 of 2)



Device Pin-Outs

Tables 26 through 29 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

Table 26. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2) Note (1)

Pin Name	84-Pin PLCC (2)	208-Pin RQFP	280-Pin PGA (3)	356-Pin BGA
DIN1 (GCLK1)	1	182	V10	AD13
DIN2 (GCLK2)	84	183	U10	AF14
DIN3 (GCLR)	13	153	V17	AD1
DIN4 (GOE)	72	4	W2	AC24
TCK	43	78	A9	A18
TMS	55	49	D6	E23
TDI	42	79	C11	A13
TDO	30	108	A18	D3

Notes:

(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)*.
(3) EPM9320A devices are not offered in this package.
(4) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 27. EPM9400 Dedicated Pin-Outs *Note (1)*

Pin Name	84-Pin PLCC *(2)*	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(3)*	55	48	67
Total User I/O Pins *(4)*	59	139	159

Notes:

(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 28. EPM9480 Dedicated Pin-Outs *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(2)*	48	67
Total User I/O Pins *(3)*	146	175

Notes:

(1) All pins not listed are user I/O pins.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.5 supersedes information published in previous versions.

Version 6.5

Version 6.6 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change:

- Added Tables 7 through 9.
- Added "Programming Sequence" on page 20 and "Programming Times" on page 20

Version 6.4

Version 6.4 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: Updated text on page 23.

Version 6.3

Version 6.3 of the *MAX 9000 Programmable Logic Device Family Data Sheet* contains the following change: added Note (7) to Table 16.

ALTERA®

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com