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What is "Embedded - Microcontrollers"?

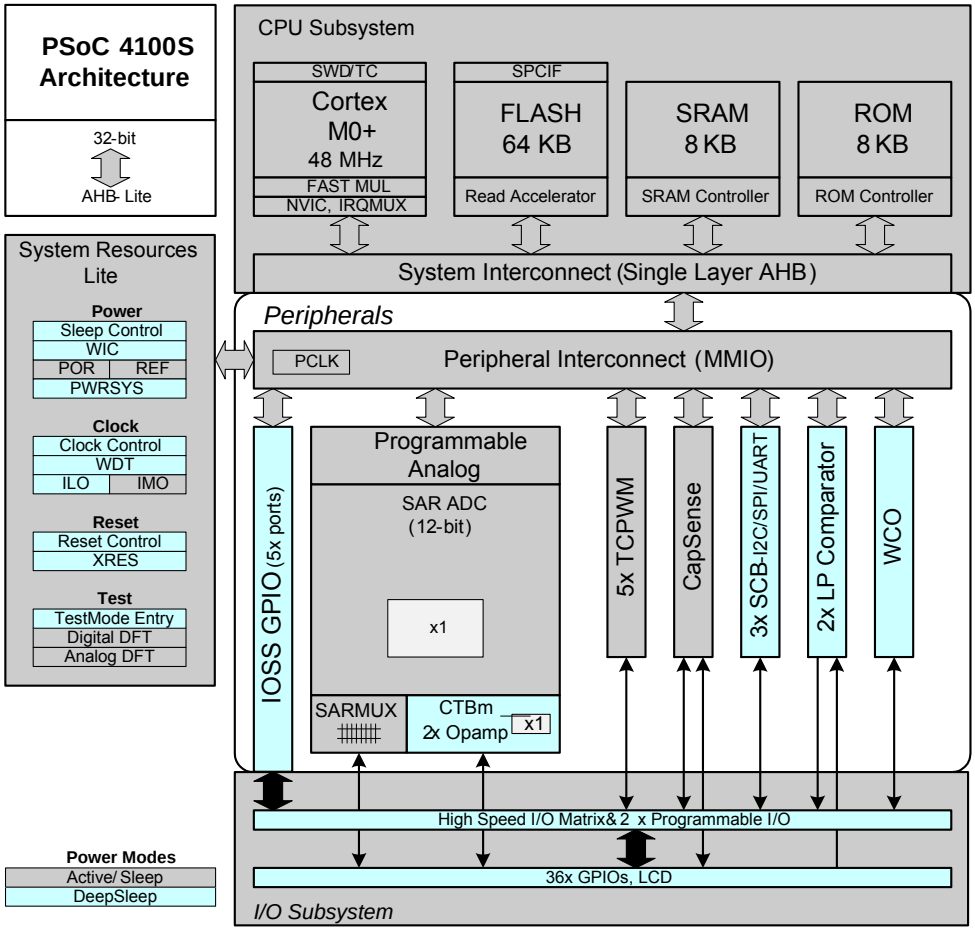
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124azi-s433t

Contents

Figure 1. Block Diagram



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

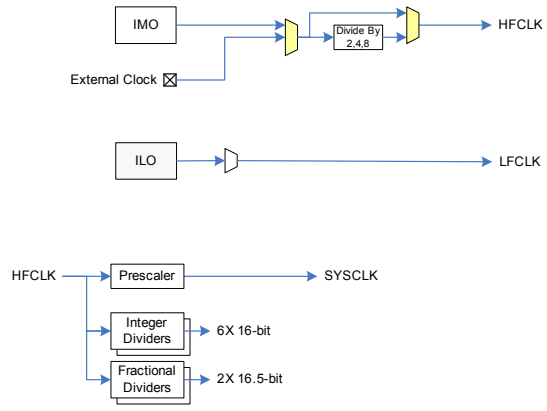
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

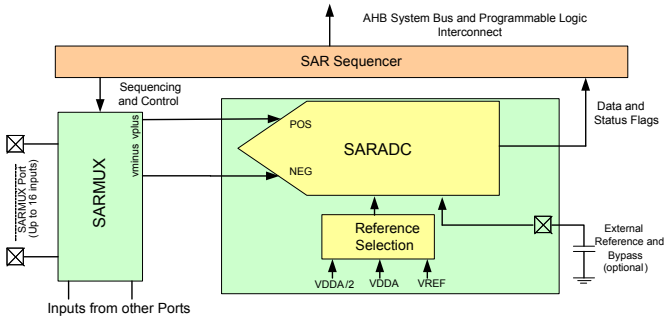
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 3. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

The PSoC 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

The PSoC 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4100S.

Serial Communication Block (SCB)

The PSoC 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I^{2}C Mode: The hardware I^{2}C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also

supports EZI2C that creates a mailbox address range in the memory of the PSoC 4100S and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4100S is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

The PSoC 4100S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100S).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

The PSoC 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Table 3. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I^2C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID25	IDD20	I^2C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHZ. Max is at 85 °C and 5.5 V.
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I^2C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID28A	IDD23A	I^2C wakeup, WDT, and Comparators on	–	1	1.2	mA	12 MHZ. Max is at 85 °C and 5.5 V.
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 3.6 V and 85 °C.
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 5.5 V and 85 °C.
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	65	µA	Max is at 1.89 V and 85 °C.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[3]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[3]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

Note
2. Guaranteed by characterization.

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	power=hi, Iload=10 mA	0.5	–	V_{DDA} -0.5	V	–
SID284	V_{OUT_2}	power=hi, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID285	V_{OUT_3}	power=med, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID286	V_{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V_{DDA} -0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA}-0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA}-0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA}-0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA}-0.2 V, Output is 0.2 V to V_{DDA}-0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA}-0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, T_{rise}=T_{fall} (approx.)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–		25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–		25 °C

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_9	$G_{BW\_LOW\_M!}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V_{DDA}-0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_19	$I_{OUT\_HI\_M!}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

Note
6. Guaranteed by characterization.

Table 14. CSD and IDAC Specifications *(continued)*

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 15. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.

Table 19. SPI DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 20. SPI AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

Memory

Table 25. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[10]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (64 KB)	–	–	35		–
SID180[11]	$T_{DEVPROG}$[10]	Total device program time	–	–	7	Seconds	–
SID181[11]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[11]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A[11]	–	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[11]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 28. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[11]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes
10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

SWD Interface

Table 29. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T		–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Internal Main Oscillator

Table 30. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 31. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 32. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[12]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 33. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[12]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note
12. Guaranteed by characterization.

Table 34. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	µW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

Table 35. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306[13]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	–

Table 36. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[13]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

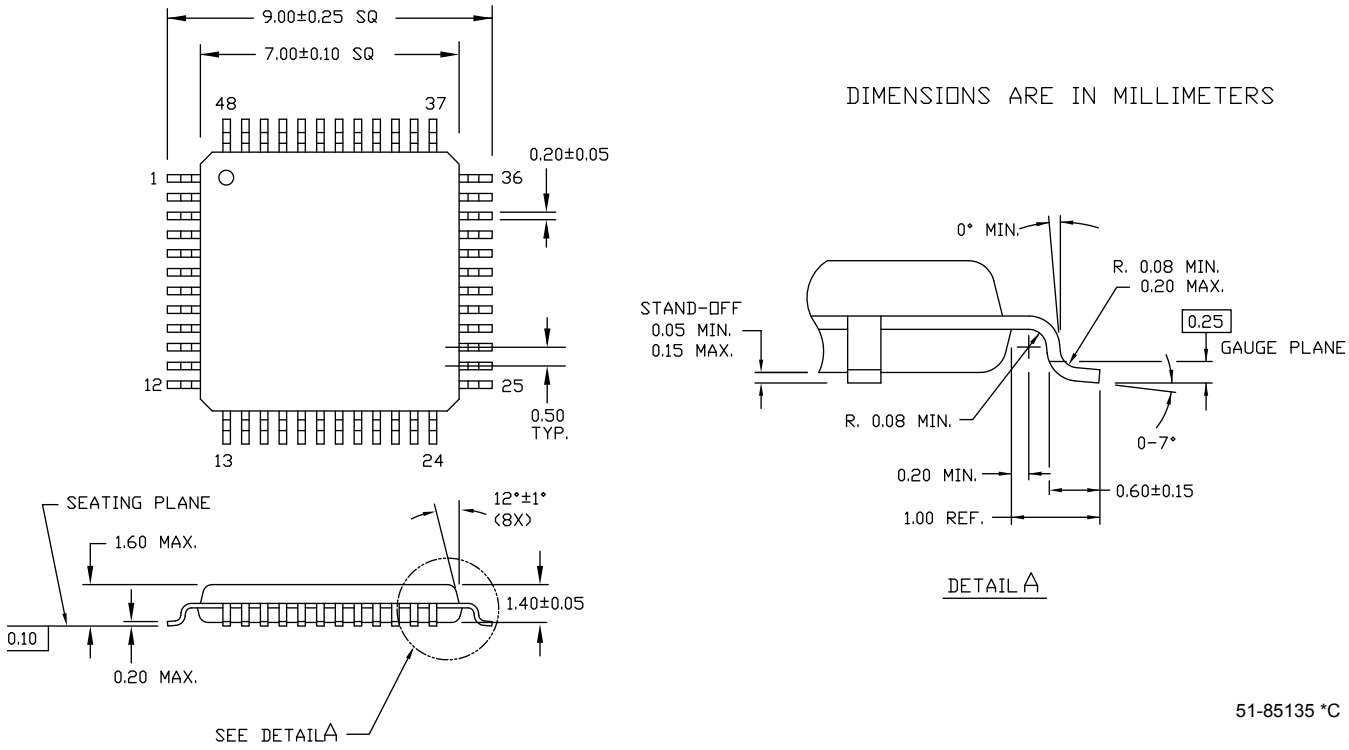
Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

Note
13. Guaranteed by characterization.

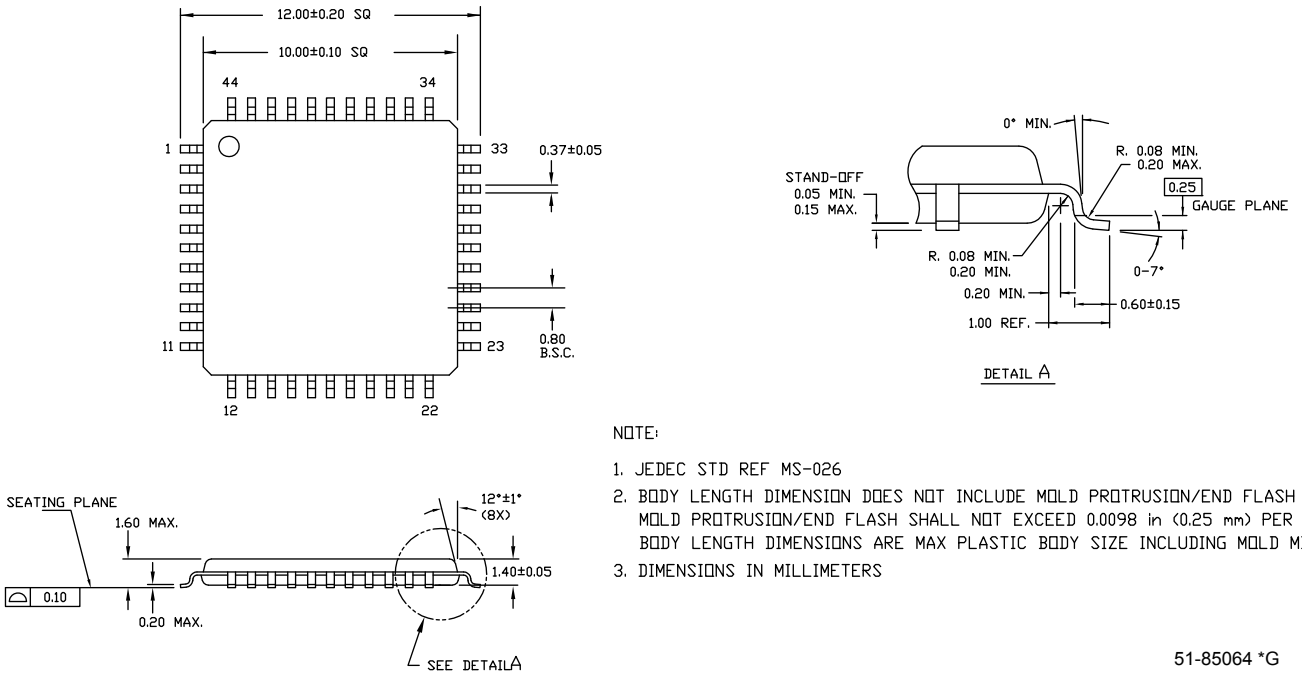
Package Diagrams

Figure 6. 48-pin TQFP Package Outline



51-85135 *C

Figure 7. 44-pin TQFP Package Outline

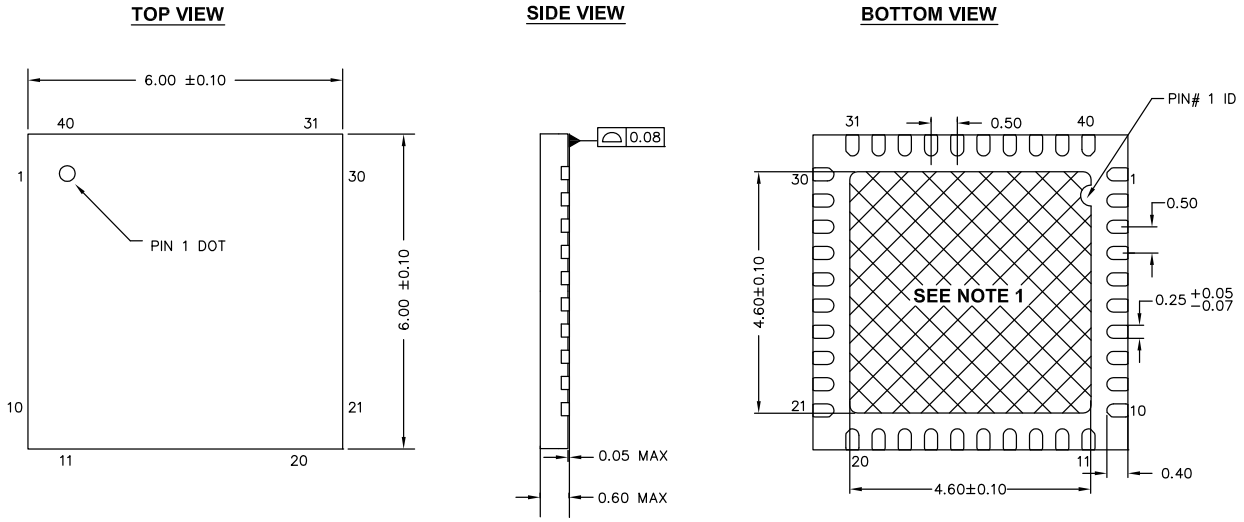


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Figure 8. 40-pin QFN Package Outline

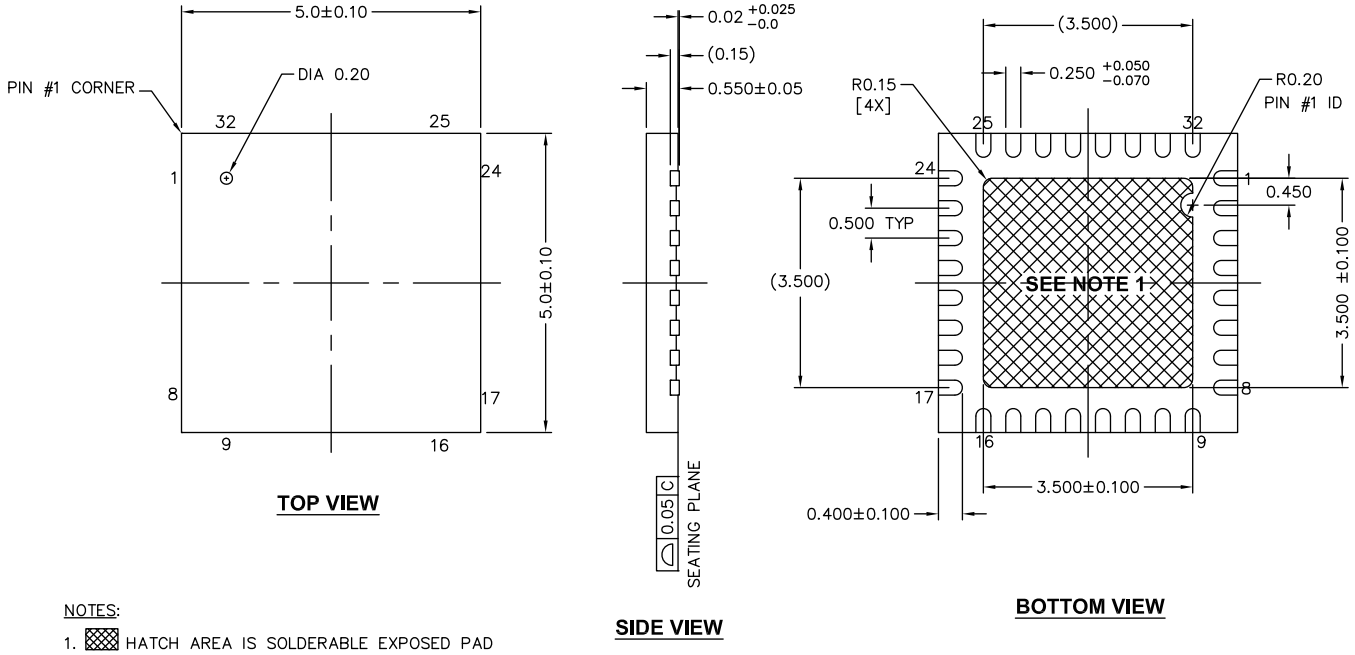


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 9. 32-pin QFN Package Outline



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4100S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00122				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4883809	WKA	08/28/2015	New datasheet
*A	4992376	WKA	10/30/2015	Updated Pinouts. Added V_{DDD} ≥ 2.2V at –40 °C under Conditions for specs SID247A, SID90, SID92. Updated Table 15. Updated Ordering Information.
*B	5037826	SLAN	12/08/2015	Changed datasheet status to Preliminary
*C	5060691	WKA	12/22/2015	Updated SCBs from 2 to 3. Updated SRAM size to 8 KB. Changed WLCSP package to 35-ball WLCSP. Updated Pin List and Alternate Pin Functions. Updated Ordering Information.
*D	5139206	WKA	02/16/2016	Added Errata. Added 35 WLCSP package details. Updated theta J_A and J_C values for all packages. Updated copyright information at the end of the document.
*E	5173961	WKA	03/15/2016	Updated values for SID79, BID194. SID175, and SID176. Updated CSD and IDAC Specifications. Updated 10-bit CapSense ADC Specifications.
*F	5330930	WKA	07/27/2016	Updated CSD and IDAC Specifications. Updated 10-bit CapSense ADC Specifications. Removed errata.
*G	5473409	WKA	10/13/2016	Added 44 TQFP pin and package details.
*H	5561833	WKA	01/09/2017	Updated Figure 3. Changed PRGIO references to Smart I/O. Updated DC Specifications. Updated Ordering Information.