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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124lqi-s433t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124lqi-s433t</a>

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## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

#### SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

#### SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V  $\pm 5\%$  (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35  $\mu$ s. The opamps can remain operational in Deep Sleep mode.

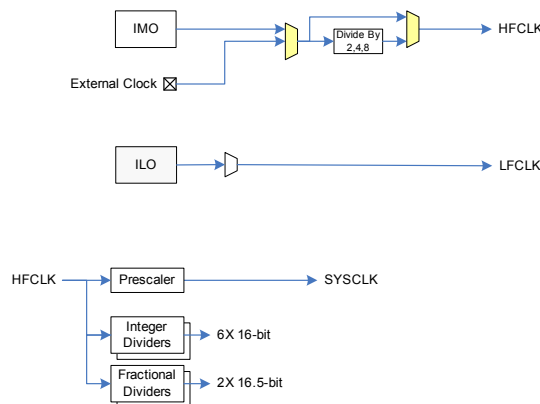
#### Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

**Figure 2. PSoC 4100S MCU Clocking Architecture**



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is  $\pm 2\%$ .

#### ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

## Reset

The PSoC 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

## Analog Blocks

### 12-bit SAR ADC

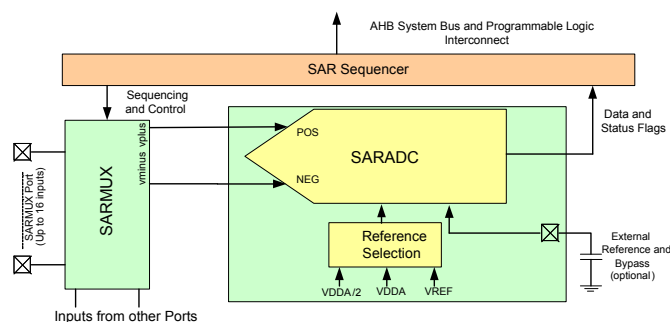
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 3. SAR ADC**



### Two Opamps (Continuous-Time Block; CTB)

The PSoC 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage

Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

### Low-power Comparators (LPC)

The PSoC 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

### Current DACs

The PSoC 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

### Analog Multiplexed Buses

The PSoC 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

## Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

## Fixed Function Digital

### Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4100S.

### Serial Communication Block (SCB)

The PSoC 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also

supports EZI2C that creates a mailbox address range in the memory of the PSoC 4100S and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode and Fast-mode devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4100S is not completely compliant with the I<sup>2</sup>C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.

**UART Mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

## GPIO

The PSoC 4100S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100S).

## Special Function Peripherals

### CapSense

CapSense is supported in the PSoC 4100S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

### LCD Segment Drive

The PSoC 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

## Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

**Table 1. Pin List**

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				



Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_miso:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	–	60	–	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID74	F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F <sub>GPIOOUT3</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F <sub>GPIOOUT4</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	48		90/10% V <sub>IO</sub>

XRES

**Table 7. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3 × V <sub>DD</sub>		
SID79	R <sub>PULLUP</sub>	Pull-up resistor	–	60	–	kΩ	–
SID80	C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
SID81 <sup>[5]</sup>	V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V <sub>DD</sub> > 4.5 V
SID82	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	

**Table 8. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 <sup>[5]</sup>	T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–
BID194 <sup>[5]</sup>	T <sub>RESETWAKE</sub>	Wake-up time from reset release	–	–	2.7	ms	–

**Note**

5. Guaranteed by characterization.



## Analog Peripherals

**Table 9. CTBm Opamp Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I <sub>DD</sub>	Opamp block current, External load					
SID269	I <sub>DD_HI</sub>	power=hi	–	1100	1850	μA	–
SID270	I <sub>DD_MED</sub>	power=med	–	550	950		–
SID271	I <sub>DD_LOW</sub>	power=lo	–	150	350		–
	G <sub>BW</sub>	Load = 20 pF, 0.1 mA V <sub>DDA</sub> = 2.7 V					
SID272	G <sub>BW_HI</sub>	power=hi	6	–	–	MHz	Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V
SID273	G <sub>BW_MED</sub>	power=med	3	–	–		Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V
SID274	G <sub>BW_LO</sub>	power=lo	–	1	–		Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V
	I <sub>OUT_MAX</sub>	V <sub>DDA</sub> = 2.7 V, 500 mV from rail					
SID275	I <sub>OUT_MAX_HI</sub>	power=hi	10	–	–	mA	Output is 0.5 V V <sub>DDA</sub> -0.5 V
SID276	I <sub>OUT_MAX_MID</sub>	power=mid	10	–	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V
SID277	I <sub>OUT_MAX_LO</sub>	power=lo	–	5	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V
	I <sub>OUT</sub>	V <sub>DDA</sub> = 1.71 V, 500 mV from rail					
SID278	I <sub>OUT_MAX_HI</sub>	power=hi	4	–	–	mA	Output is 0.5 V V <sub>DDA</sub> -0.5 V
SID279	I <sub>OUT_MAX_MID</sub>	power=mid	4	–	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V
SID280	I <sub>OUT_MAX_LO</sub>	power=lo	–	2	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V
	I <sub>DD_Int</sub>	Opamp block current Internal Load					
SID269_I	I <sub>DD_HI_Int</sub>	power=hi	–	1500	1700	μA	–
SID270_I	I <sub>DD_MED_Int</sub>	power=med	–	700	900		–
SID271_I	I <sub>DD_LOW_Int</sub>	power=lo	–	–	–		–
	G <sub>BW</sub>	V <sub>DDA</sub> = 2.7 V	–	–	–		–
SID272_I	G <sub>BW_HI_Int</sub>	power=hi	8	–	–	MHz	Output is 0.25 V to V <sub>DDA</sub> -0.25 V

**Table 9. CTBm Opamp Specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, $T_{rise}=T_{fall}$ (approx.)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I <sub>DD_HI_M1</sub>	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	I <sub>DD_MED_M1</sub>	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I <sub>DD_LOW_M1</sub>	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I <sub>DD_HI_M2</sub>	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I <sub>DD_MED_M2</sub>	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I <sub>DD_LOW_M2</sub>	Mode 2, Low current	–	15	–		25 °C

**Table 13. SAR Specifications** (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
SID102	A_VIND	Input voltage range - differential[	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
<b>SAR ADC AC Specifications</b>							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F <sub>IN</sub> = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	
SID111	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID111A	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1.71 to V <sub>DD</sub>
SID111B	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID112	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID112A	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V <sub>REF</sub> = 1.71 to V <sub>DD</sub>
SID112B	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F <sub>in</sub> = 10 kHz
SID261	FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

**Table 19. SPI DC Specifications<sup>[9]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	μA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

**Table 20. SPI AC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		T <sub>CPU</sub> = 1/F <sub>CPU</sub>
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

**Table 21. UART DC Specifications<sup>[9]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbps	–	–	312	μA	–

**Table 22. UART AC Specifications<sup>[9]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F <sub>UART</sub>	Bit rate	–	–	1	Mbps	–

**Table 23. LCD Direct Drive DC Specifications<sup>[9]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I <sub>LCDLOW</sub>	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	–	20	–	mV	–
SID157	I <sub>LCDOP1</sub>	LCD system operating current V <sub>bias</sub> = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I <sub>LCDOP2</sub>	LCD system operating current V <sub>bias</sub> = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25 °C

**Table 24. LCD Direct Drive AC Specifications<sup>[9]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	–

**Note**

9. Guaranteed by characterization.

## Memory

**Table 25. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	–

**Table 26. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub> <sup>[10]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T <sub>ROWERASE</sub> <sup>[10]</sup>	Row erase time	–	–	16		–
SID176	T <sub>ROWPROGRAM</sub> <sup>[10]</sup>	Row program time after erase	–	–	4		–
SID178	T <sub>BULKERASE</sub> <sup>[10]</sup>	Bulk erase time (64 KB)	–	–	35		–
SID180 <sup>[11]</sup>	T <sub>DEVPROG</sub> <sup>[10]</sup>	Total device program time	–	–	7	Seconds	–
SID181 <sup>[11]</sup>	F <sub>END</sub>	Flash endurance	100 K	–	–	Cycles	–
SID182 <sup>[11]</sup>	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A <sup>[11]</sup>	–	Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

## System Resources

### Power-on Reset (POR)

**Table 27. Power On Reset (PRES)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 <sup>[11]</sup>	V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.5	V	–
SID186 <sup>[11]</sup>	V <sub>FALLIPOR</sub>	Falling trip voltage	0.70	–	1.4		–

**Table 28. Brown-out Detect (BOD) for V<sub>CCD</sub>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 <sup>[11]</sup>	V <sub>FALLPPOR</sub>	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 <sup>[11]</sup>	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

### Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

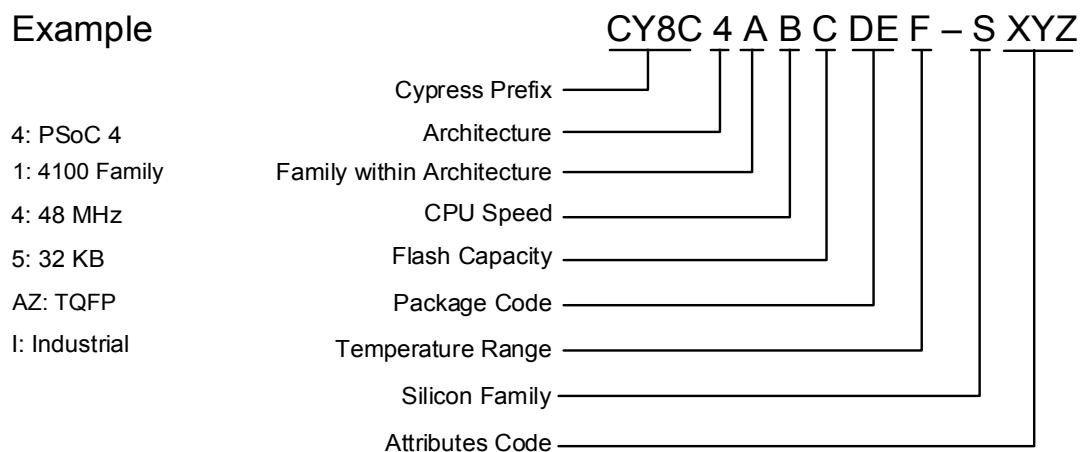
11. Guaranteed by characterization.

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

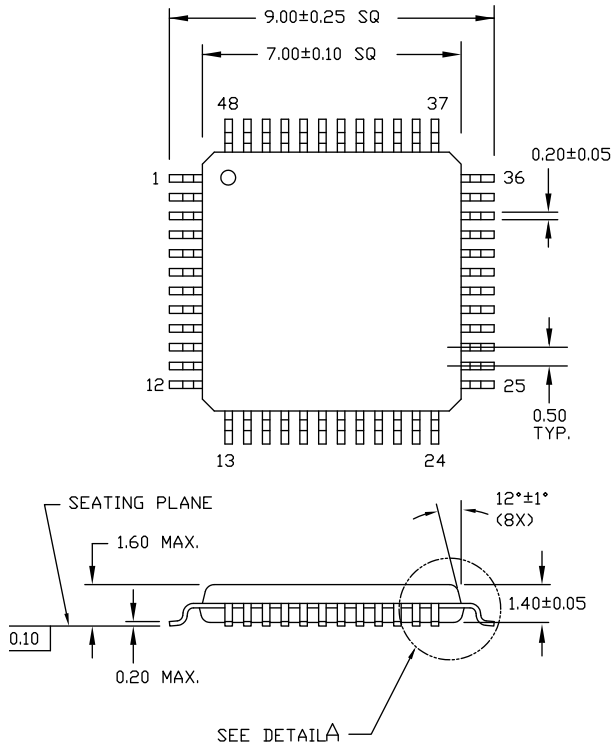
### Example



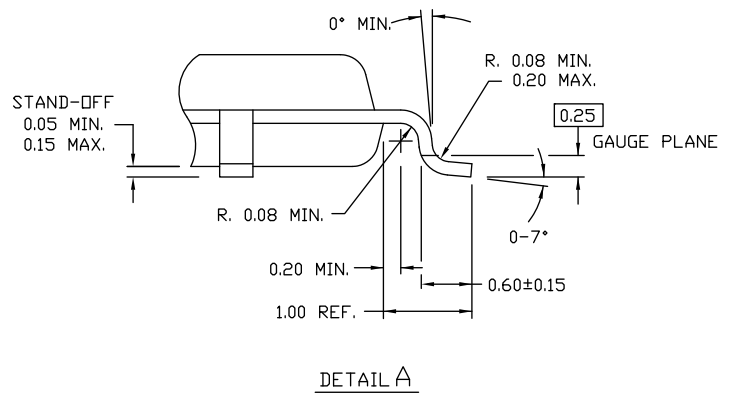


## Package Diagrams

**Figure 6. 48-pin TQFP Package Outline**

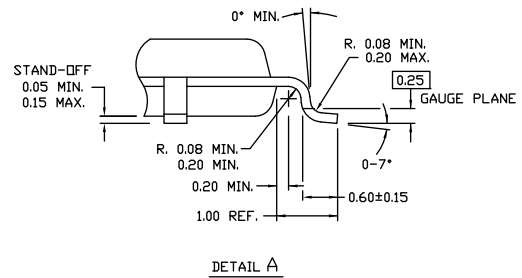
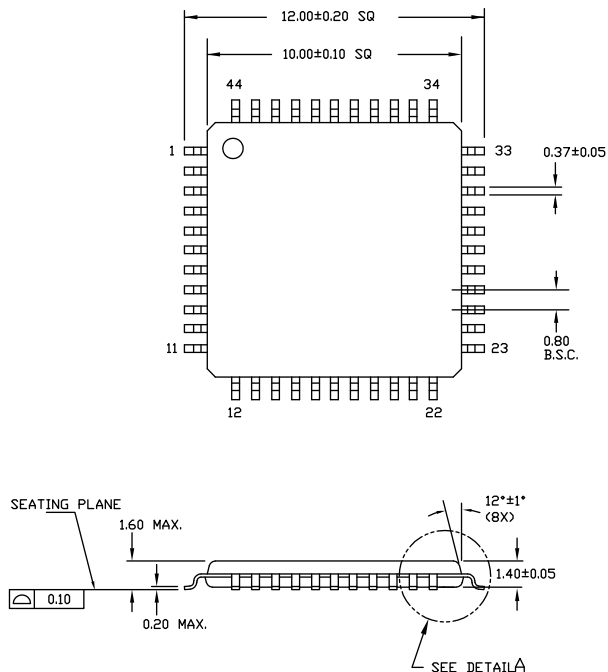


DIMENSIONS ARE IN MILLIMETERS



51-85135 \*C

**Figure 7. 44-pin TQFP Package Outline**

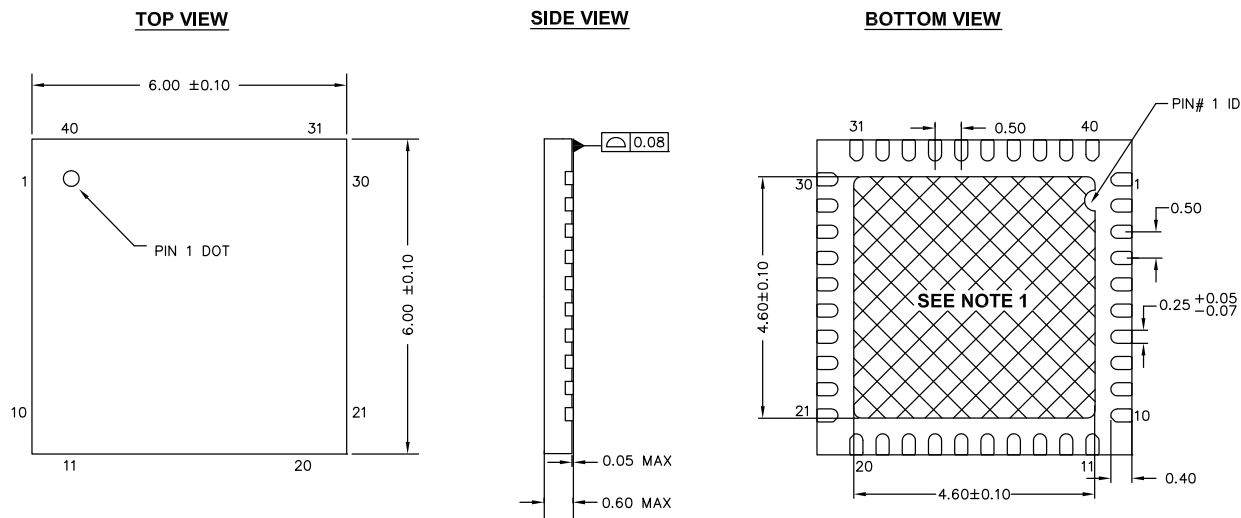


**NOTE:**


1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 \*G

**Figure 8. 40-pin QFN Package Outline**

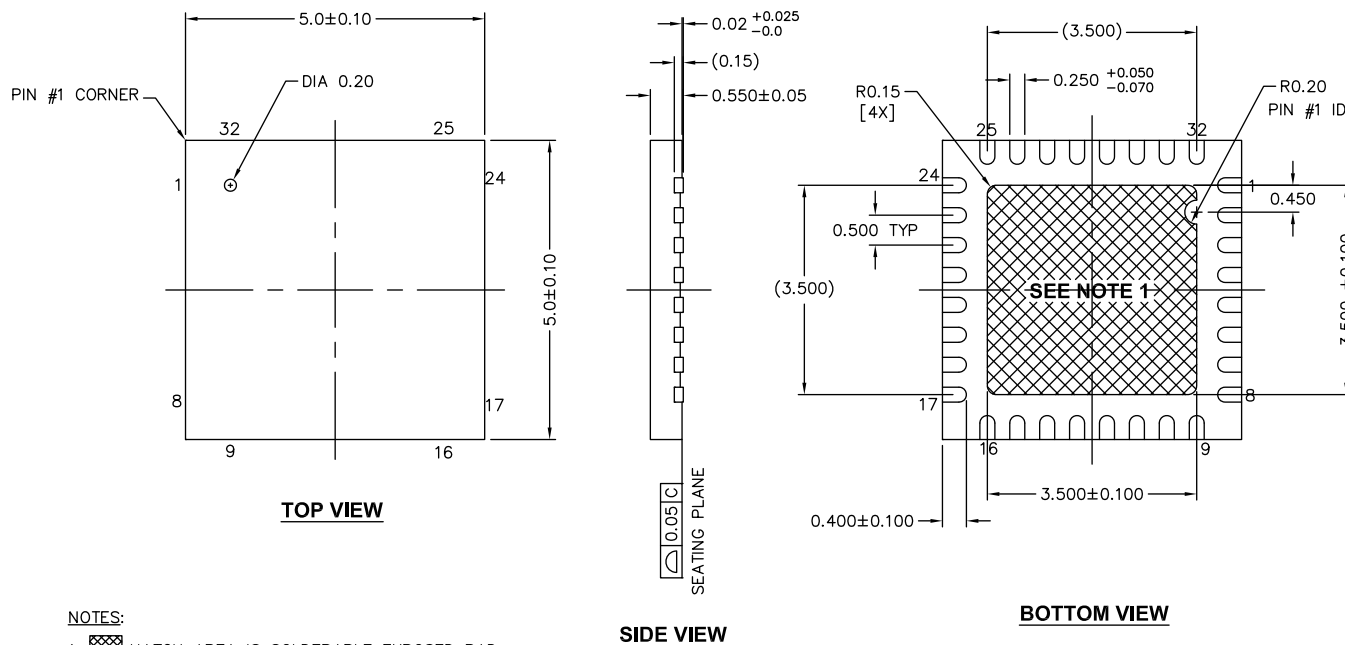


**NOTES:**


1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 \*A

**Figure 9. 32-pin QFN Package Outline**

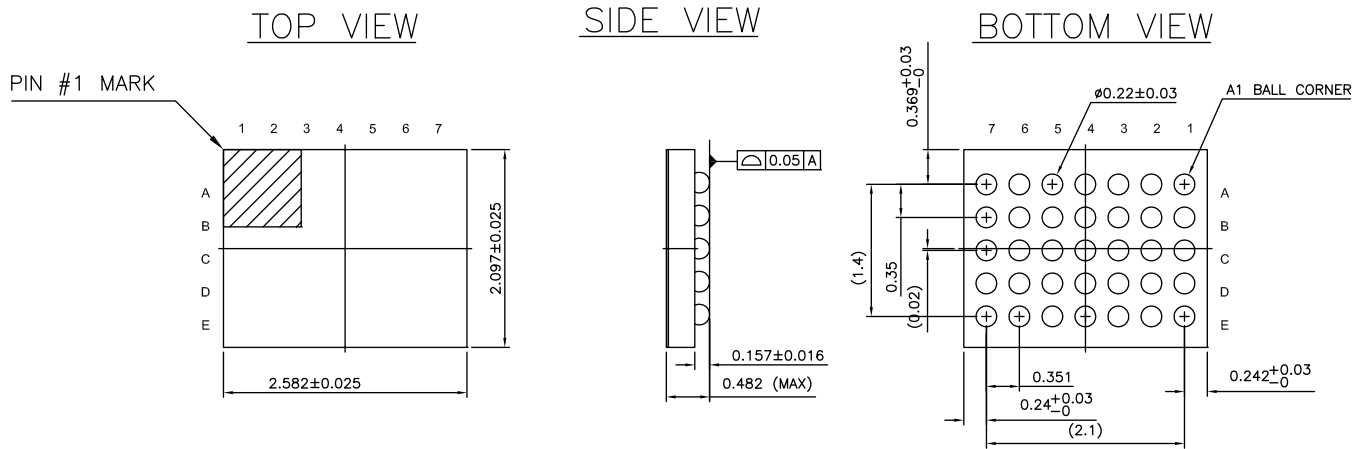


**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 \*E

**Figure 10. 35-Ball WLCSP Package Outline**



ALL DIMENSIONS ARE IN MM  
JEDEC Publication 95; Design Guide 4.18

002-09958 \*C

**Table 42. Acronyms Used in this Document** *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

**Table 42. Acronyms Used in this Document** *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## Document Conventions

### Units of Measure

**Table 43. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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