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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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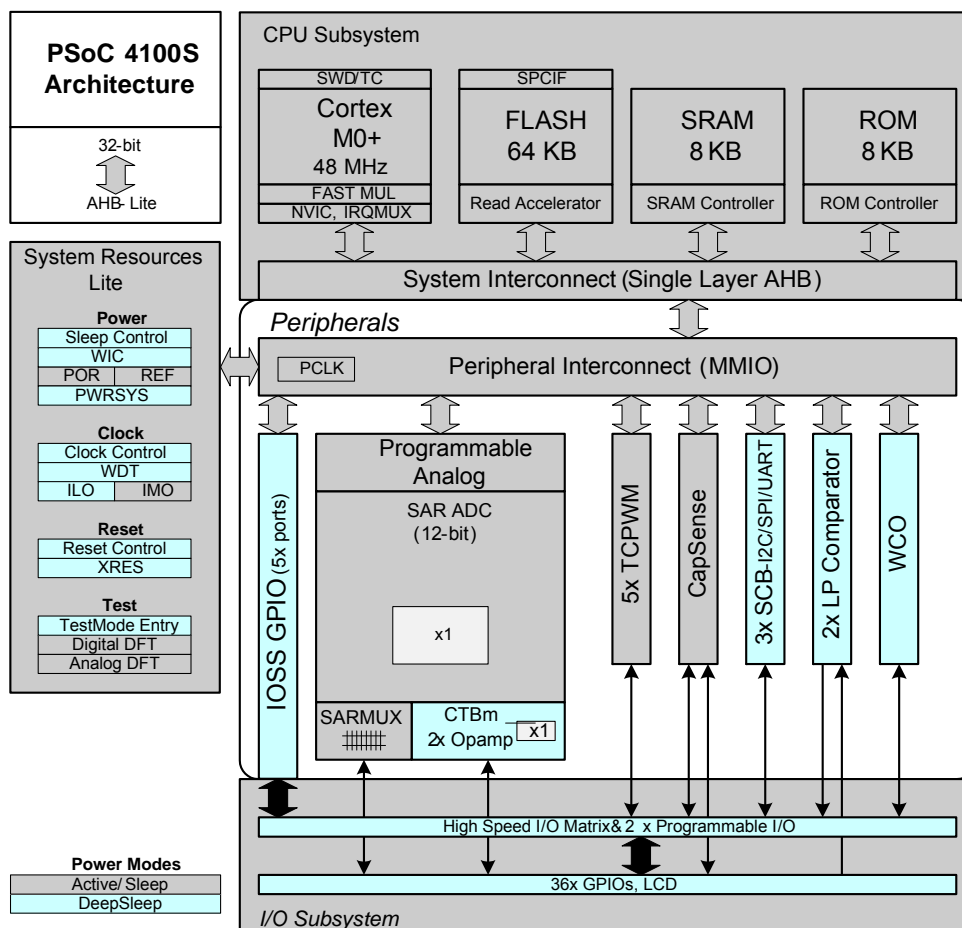
Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	35-XFBGA, WLCSP
Supplier Device Package	35-WLCSP (2.58x2.1)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125fni-s413t

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Figure 1. Block Diagram



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V $\pm 5\%$ (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

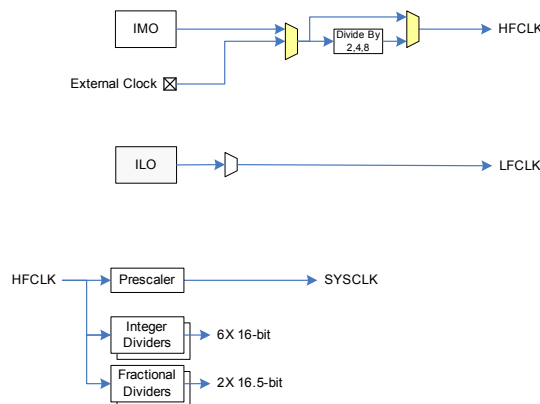
Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is $\pm 2\%$.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

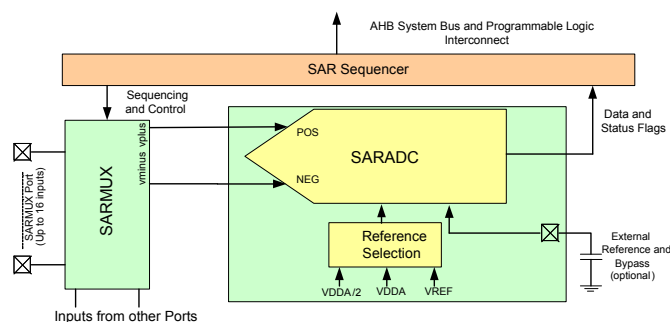
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 3. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

The PSoC 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage

Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

The PSoC 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4100S.

Serial Communication Block (SCB)

The PSoC 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also

supports EZI2C that creates a mailbox address range in the memory of the PSoC 4100S and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4100S is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

The PSoC 4100S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100S).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

The PSoC 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1. Pin List

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				

Table 3. DC Specifications (continued)

Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I ² C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID25	IDD20	I ² C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHZ. Max is at 85 °C and 5.5 V.
Sleep Mode, VDD = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I ² C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID28A	IDD23A	I ² C wakeup, WDT, and Comparators on	–	1	1.2	mA	12 MHZ. Max is at 85 °C and 5.5 V.
Deep Sleep Mode, VDD = 1.8 V to 3.6 V (Regulator on)							
SID31	I _{DD26}	I ² C wakeup and WDT on	–	2.5	60	μA	Max is at 3.6 V and 85 °C.
Deep Sleep Mode, VDD = 3.6 V to 5.5 V (Regulator on)							
SID34	I _{DD29}	I ² C wakeup and WDT on	–	2.5	60	μA	Max is at 5.5 V and 85 °C.
Deep Sleep Mode, VDD = VCCD = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I _{DD32}	I ² C wakeup and WDT on	–	2.5	65	μA	Max is at 1.89 V and 85 °C.
XRES Current							
SID307	I _{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 ^[3]	T _{SLEEP}	Wakeup from Sleep mode	–	0	–	μs	
SID50 ^[3]	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	35	–		

Note

2. Guaranteed by characterization.

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} < 2.7$ V	$0.7 \times V_{DDD}$	–	–		–
SID242	V_{IL}	LVTTL input, $V_{DDD} < 2.7$ V	–	–	$0.3 \times V_{DDD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	$V_{DDD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	$V_{DDD} - 0.5$	–	–		$I_{OH} = 1$ mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DDD} = 3.0$ V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD} , Load = 25 pF

Notes

- V_{IH} must not exceed $V_{DDD} + 0.2$ V.
- Guaranteed by characterization.

Table 6. GPIO AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Load = 25 pF
SID74	$F_{GPIOOUT1}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOOUT2}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOOUT3}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOOUT4}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5$ V	–	–	48		90/10% V_{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	k Ω	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81 ^[5]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for $V_{DD} > 4.5$ V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 ^[5]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	–
BID194 ^[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note

5. Guaranteed by characterization.

Analog Peripherals

Table 9. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current, External load					
SID269	I _{DD_HI}	power=hi	–	1100	1850	μA	–
SID270	I _{DD_MED}	power=med	–	550	950		–
SID271	I _{DD_LOW}	power=lo	–	150	350		–
	G _{BW}	Load = 20 pF, 0.1 mA V _{DDA} = 2.7 V					
SID272	G _{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V _{DDA} -0.2 V
SID273	G _{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V _{DDA} -0.2 V
SID274	G _{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V _{DDA} -0.2 V
	I _{OUT_MAX}	V _{DDA} = 2.7 V, 500 mV from rail					
SID275	I _{OUT_MAX_HI}	power=hi	10	–	–	mA	Output is 0.5 V V _{DDA} -0.5 V
SID276	I _{OUT_MAX_MID}	power=mid	10	–	–		Output is 0.5 V V _{DDA} -0.5 V
SID277	I _{OUT_MAX_LO}	power=lo	–	5	–		Output is 0.5 V V _{DDA} -0.5 V
	I _{OUT}	V _{DDA} = 1.71 V, 500 mV from rail					
SID278	I _{OUT_MAX_HI}	power=hi	4	–	–	mA	Output is 0.5 V V _{DDA} -0.5 V
SID279	I _{OUT_MAX_MID}	power=mid	4	–	–		Output is 0.5 V V _{DDA} -0.5 V
SID280	I _{OUT_MAX_LO}	power=lo	–	2	–		Output is 0.5 V V _{DDA} -0.5 V
	I _{DD_Int}	Opamp block current Internal Load					
SID269_I	I _{DD_HI_Int}	power=hi	–	1500	1700	μA	–
SID270_I	I _{DD_MED_Int}	power=med	–	700	900		–
SID271_I	I _{DD_LOW_Int}	power=lo	–	–	–		–
	G _{BW}	V _{DDA} = 2.7 V	–	–	–		–
SID272_I	G _{BW_HI_Int}	power=hi	8	–	–	MHz	Output is 0.25 V to V _{DDA} -0.25 V

Table 9. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, $T_{rise}=T_{fall}$ (approx.)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	I _{DD_MED_M1}	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I _{DD_HI_M2}	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I _{DD_MED_M2}	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, Low current	–	15	–		25 °C

Table 13. SAR Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	
SID102	A_VIND	Input voltage range - differential[V _{SS}	–	V _{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F _{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A _{samp} /2	kHz	
SID111	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V _{REF} = 1 to V _{DD}
SID111A	A_INL	Integral non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V _{REF} = 1.71 to V _{DD}
SID111B	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V _{REF} = 1 to V _{DD}
SID112	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID112A	A_DNL	Differential non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V _{REF} = 1.71 to V _{DD}
SID112B	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F _{in} = 10 kHz
SID261	FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

Table 15. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksp	–	–	2	LSB	V _{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksp	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 16. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

²C

Table 17. Fixed I²C DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4		

Table 18. Fixed I²C AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Msp	–

Notes

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

Note

8. Guaranteed by characterization.

SWD Interface

Table 29. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCLK \leq 1/3 CPU clock frequency
SID215 ^[12]	T_SWDI_SETUP	$T = 1/f\text{ SWDCLK}$	$0.25 \cdot T$	–	–	ns	–
SID216 ^[12]	T_SWDI_HOLD	$T = 1/f\text{ SWDCLK}$	$0.25 \cdot T$	–	–		–
SID217 ^[12]	T_SWDO_VALID	$T = 1/f\text{ SWDCLK}$	–	–	$0.5 \cdot T$		–
SID217A ^[12]	T_SWDO_HOLD	$T = 1/f\text{ SWDCLK}$	1	–	–		–

Internal Main Oscillator

Table 30. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

Table 31. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	–
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 32. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[12]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	–

Table 33. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[12]	T _{STARTILO1}	ILO startup time	–	–	2	ms	–
SID236 ^[12]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	–
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	–

Note

12. Guaranteed by characterization.

Table 34. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

Table 35. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 ^[13]	ExtClkDuty	Duty cycle; measured at V _{DD/2}	45	–	55	%	–

Table 36. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[13]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

Note

13. Guaranteed by characterization.

Packaging

The PSoC 4100S will be offered in 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball WLCSP packages. Package dimensions and Cypress drawing numbers are in the following table.

Table 38. Package List

Spec ID#	Package	Description	Package Dwg
BID20	48-pin TQFP	7 × 7 × 1.4-mm height with 0.5-mm pitch	51-85135
BID20A	44-pin TQFP	10 × 10 × 1.6-mm height with 0.8-mm pitch	51-85064
BID27	40-pin QFN	6 × 6 × 0.6-mm height with 0.5-mm pitch	001-80659
BID34A	32-pin QFN	5 × 5 × 0.6-mm height with 0.5-mm pitch	001-42168
BID34D	35-ball WLCSP	2.6 × 2.1 × 0.48-mm height with 0.35-mm pitch	002-09958

Table 39. Package Thermal Characteristics

Parameter	Description	Package	Min	Typ	Max	Units
T _A	Operating Ambient temperature		−40	25	85	°C
T _J	Operating junction temperature		−40	—	100	°C
T _{JA}	Package θ _{JA}	48-pin TQFP	—	74.8	—	°C/Watt
T _{JC}	Package θ _{JC}	48-pin TQFP	—	35.7	—	°C/Watt
T _{JA}	Package θ _{JA}	44-pin TQFP	—	57.2	—	°C/Watt
T _{JC}	Package θ _{JC}	44-pin TQFP	—	17.5	—	°C/Watt
T _{JA}	Package θ _{JA}	40-pin QFN	—	17.8	—	°C/Watt
T _{JC}	Package θ _{JC}	40-pin QFN	—	2.8	—	°C/Watt
T _{JA}	Package θ _{JA}	32-pin QFN	—	19.9	—	°C/Watt
T _{JC}	Package θ _{JC}	32-pin QFN	—	4.3	—	°C/Watt
T _{JA}	Package θ _{JA}	35-ball WLCSP	—	43	—	°C/Watt
T _{JC}	Package θ _{JC}	35-ball WLCSP	—	0.3	—	°C/Watt

Table 40. Solder Reflow Peak Temperature

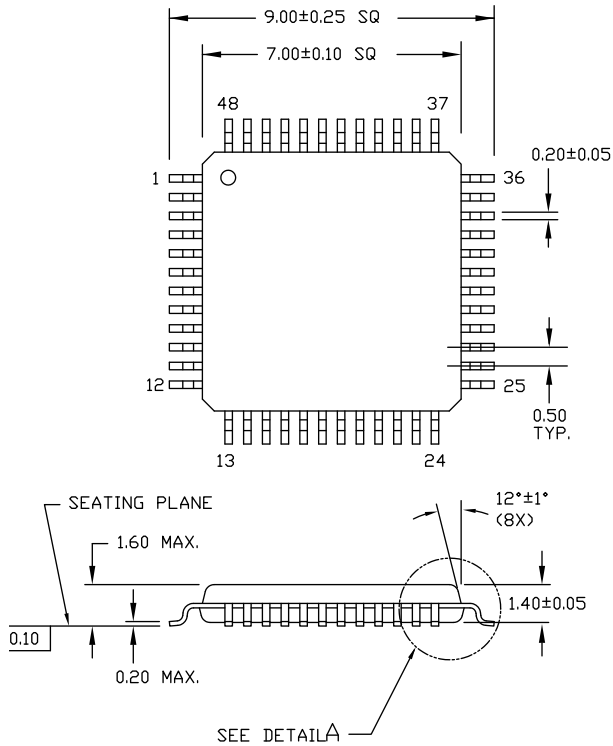
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

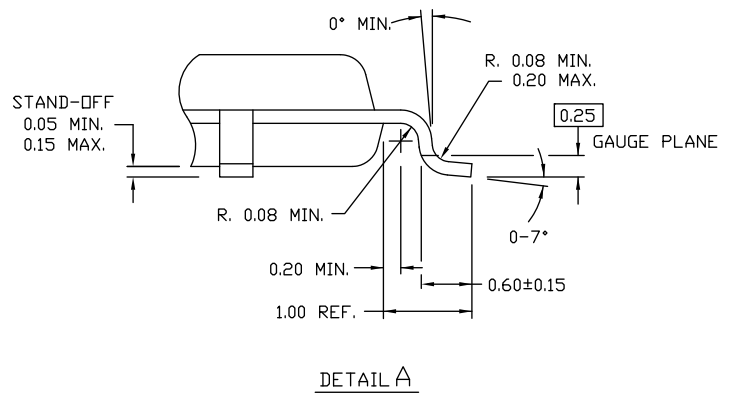
Package	MSL
All except WLCSP	MSL 3
35-ball WLCSP	MSL 1

Package Diagrams

Figure 6. 48-pin TQFP Package Outline

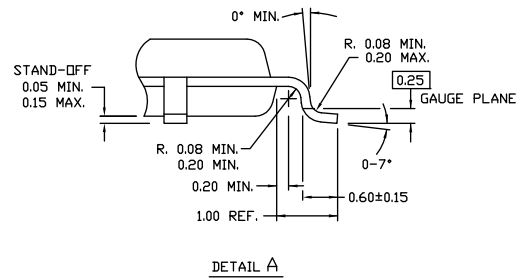
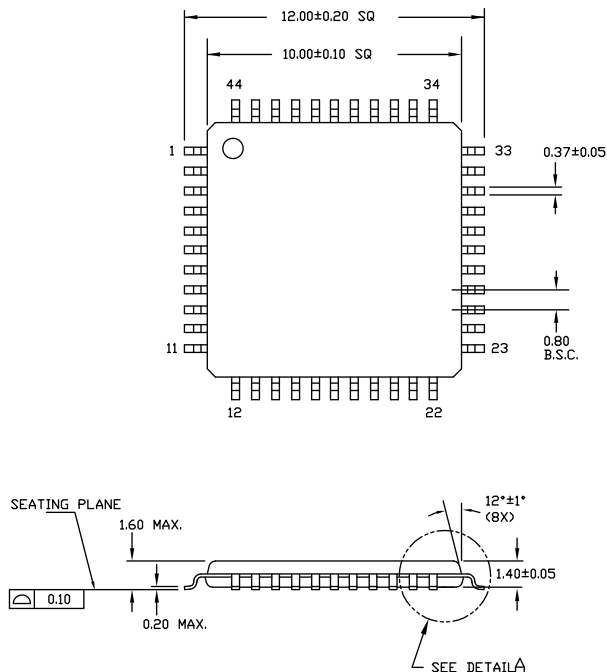


DIMENSIONS ARE IN MILLIMETERS



51-85135 *C

Figure 7. 44-pin TQFP Package Outline

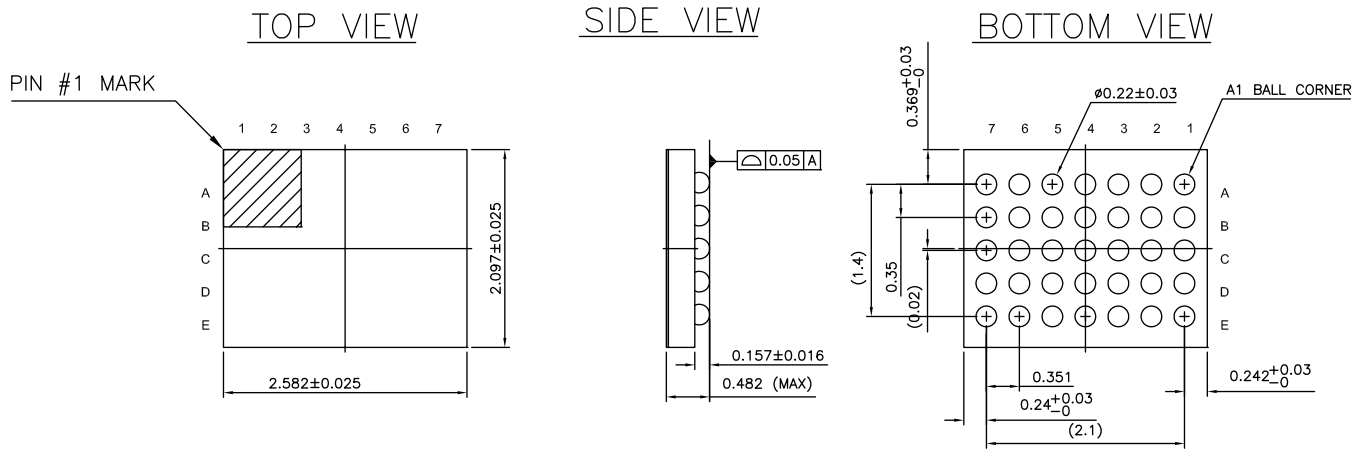


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Figure 10. 35-Ball WLCSP Package Outline



ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-09958 *C

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt