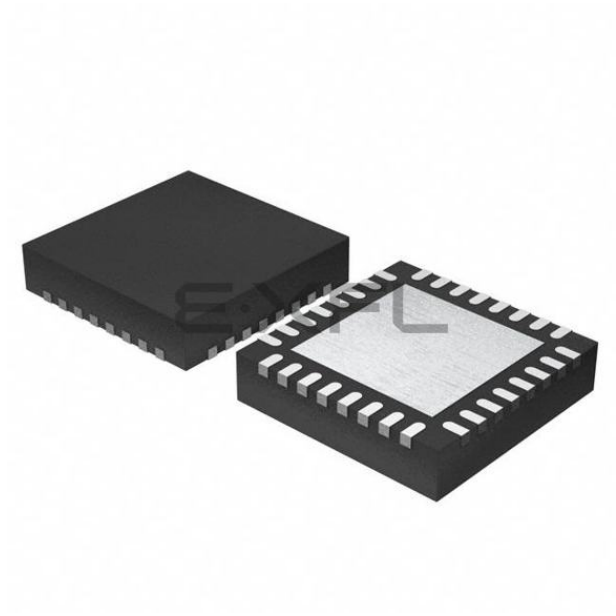


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

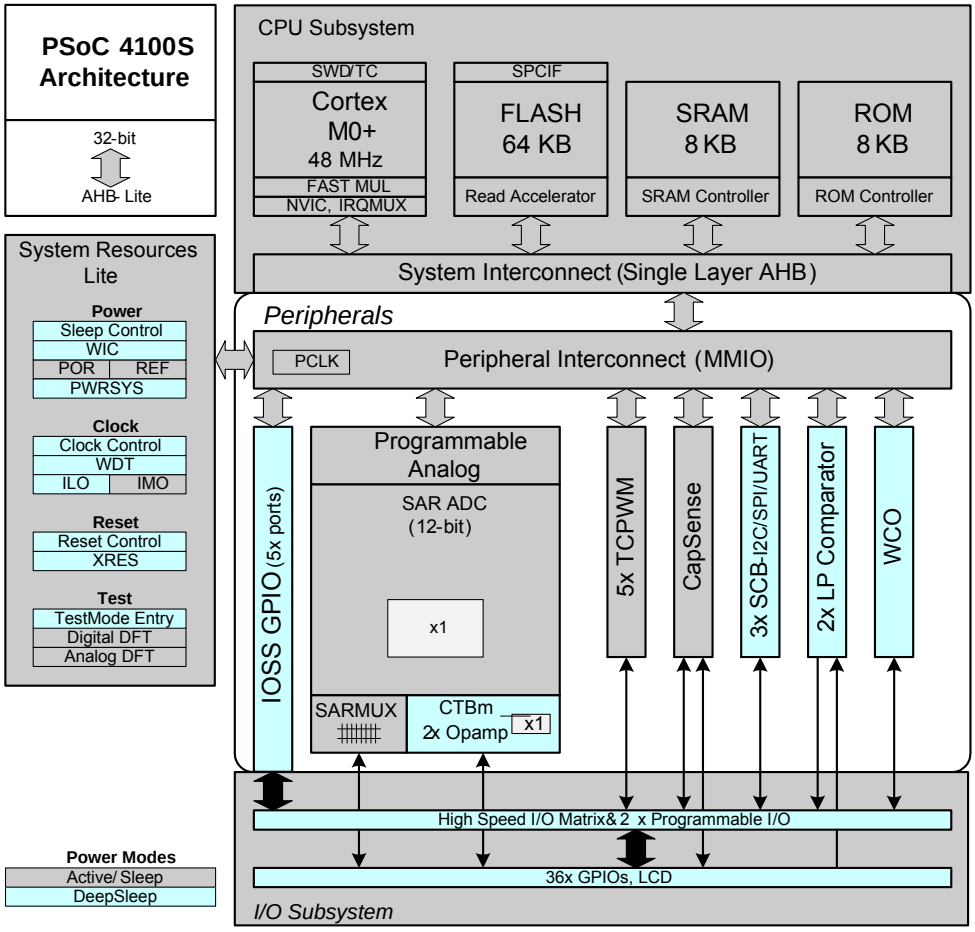
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x10b Slope; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125lqi-s412t |

## Contents

**Figure 1. Block Diagram**




PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

# Functional Definition

## CPU and Memory Subsystem

### *CPU*

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

### *Flash*

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

### *SRAM*

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

### *SROM*

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### *Power System*

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

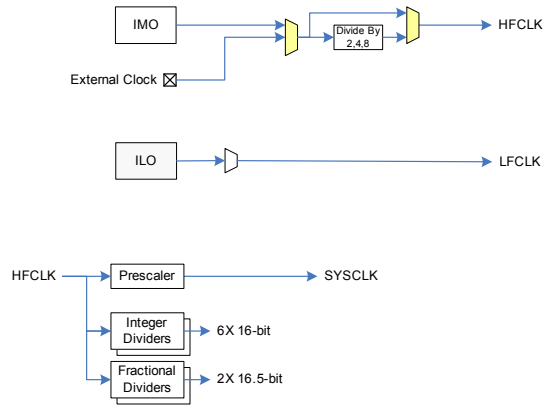
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

### *Clock System*

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

**Figure 2. PSoC 4100S MCU Clocking Architecture**




The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

### *IMO Clock Source*

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

### *ILO Clock Source*

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### *Watch Crystal Oscillator (WCO)*

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

### *Watchdog Timer*

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

## Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

**Table 1. Pin List**

| 48-TQFP | | 44-TQFP | | 40-QFN | | 32-QFN | | 35-CSP | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 28 | P0.0 | 24 | P0.0 | 22 | P0.0 | 17 | P0.0 | C3 | P0.0 |
| 29 | P0.1 | 25 | P0.1 | 23 | P0.1 | 18 | P0.1 | A5 | P0.1 |
| 30 | P0.2 | 26 | P0.2 | 24 | P0.2 | 19 | P0.2 | A4 | P0.2 |
| 31 | P0.3 | 27 | P0.3 | 25 | P0.3 | 20 | P0.3 | A3 | P0.3 |
| 32 | P0.4 | 28 | P0.4 | 26 | P0.4 | 21 | P0.4 | B3 | P0.4 |
| 33 | P0.5 | 29 | P0.5 | 27 | P0.5 | 22 | P0.5 | A6 | P0.5 |
| 34 | P0.6 | 30 | P0.6 | 28 | P0.6 | 23 | P0.6 | B4 | P0.6 |
| 35 | P0.7 | 31 | P0.7 | 29 | P0.7 | | | B5 | P0.7 |
| 36 | XRES | 32 | XRES | 30 | XRES | 24 | XRES | B6 | XRES |
| 37 | VCCD | 33 | VCCD | 31 | VCCD | 25 | VCCD | A7 | VCCD |
| 38 | VSSD | | | DN | VSSD | 26 | VSSD | B7 | VSS |
| 39 | VDDD | 34 | VDDD | 32 | VDDD | | | C7 | VDD |
| 40 | VDDA | 35 | VDDA | 33 | VDDA | 27 | VDD | C7 | VDD |
| 41 | VSSA | 36 | VSSA | 34 | VSSA | 28 | VSSA | B7 | VSS |
| 42 | P1.0 | 37 | P1.0 | 35 | P1.0 | 29 | P1.0 | C4 | P1.0 |
| 43 | P1.1 | 38 | P1.1 | 36 | P1.1 | 30 | P1.1 | C5 | P1.1 |
| 44 | P1.2 | 39 | P1.2 | 37 | P1.2 | 31 | P1.2 | C6 | P1.2 |
| 45 | P1.3 | 40 | P1.3 | 38 | P1.3 | 32 | P1.3 | D7 | P1.3 |
| 46 | P1.4 | 41 | P1.4 | 39 | P1.4 | | | D4 | P1.4 |
| 47 | P1.5 | 42 | P1.5 | | | | | D5 | P1.5 |
| 48 | P1.6 | 43 | P1.6 | | | | | D6 | P1.6 |
| 1 | P1.7/VREF | 44 | P1.7/VREF | 40 | P1.7/VREF | 1 | P1.7/VREF | E7 | P1.7/VREF |
| | | 1 | VSSD | | | | | | |
| 2 | P2.0 | 2 | P2.0 | 1 | P2.0 | 2 | P2.0 | | |
| 3 | P2.1 | 3 | P2.1 | 2 | P2.1 | 3 | P2.1 | | |
| 4 | P2.2 | 4 | P2.2 | 3 | P2.2 | 4 | P2.2 | D3 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | 4 | P2.3 | 5 | P2.3 | E4 | P2.3 |
| 6 | P2.4 | 6 | P2.4 | 5 | P2.4 | | | E5 | P2.4 |
| 7 | P2.5 | 7 | P2.5 | 6 | P2.5 | 6 | P2.5 | E6 | P2.5 |
| 8 | P2.6 | 8 | P2.6 | 7 | P2.6 | 7 | P2.6 | E3 | P2.6 |
| 9 | P2.7 | 9 | P2.7 | 8 | P2.7 | 8 | P2.7 | E2 | P2.7 |
| 10 | VSSD | 10 | VSSD | 9 | VSSD | | | | |
| 12 | P3.0 | 11 | P3.0 | 10 | P3.0 | 9 | P3.0 | E1 | P3.0 |
| 13 | P3.1 | 12 | P3.1 | 11 | P3.1 | 10 | P3.1 | D2 | P3.1 |
| 14 | P3.2 | 13 | P3.2 | 12 | P3.2 | 11 | P3.2 | D1 | P3.2 |
| 16 | P3.3 | 14 | P3.3 | 13 | P3.3 | 12 | P3.3 | C1 | P3.3 |
| 17 | P3.4 | 15 | P3.4 | 14 | P3.4 | | | C2 | P3.4 |
| 18 | P3.5 | 16 | P3.5 | 15 | P3.5 | | | | |

### Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

| Port/Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|---|---|---|---|---|---|---|---|
| P0.0 | lpcomp.in_p[0] | | | | tcpwm.tr_in[0] | scb[2].i2c_scl:0 | scb[0].spi_select1:0 |
| P0.1 | lpcomp.in_n[0] | | | | tcpwm.tr_in[1] | scb[2].i2c_sda:0 | scb[0].spi_select2:0 |
| P0.2 | lpcomp.in_p[1] | | | | | | scb[0].spi_select3:0 |
| P0.3 | lpcomp.in_n[1] | | | | | | scb[2].spi_select0 |
| P0.4 | wco.wco_in | | | scb[1].uart_rx:0 | scb[2].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:1 |
| P0.5 | wco.wco_out | | | scb[1].uart_tx:0 | scb[2].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:1 |
| P0.6 | | | srss.ext_clk | scb[1].uart_cts:0 | scb[2].uart_tx:1 | | scb[1].spi_clk:1 |
| P0.7 | | | tcpwm.line[0]:2 | scb[1].uart_rts:0 | | | scb[1].spi_select0:1 |
| P1.0 | ctb0_oa0+ | | tcpwm.line[2]:1 | scb[0].uart_rx:1 | | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | ctb0_oa0- | | tcpwm.line_compl[2]:1 | scb[0].uart_tx:1 | | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | ctb0_oa0_out | | tcpwm.line[3]:1 | scb[0].uart_cts:1 | tcpwm.tr_in[2] | scb[2].i2c_scl:1 | scb[0].spi_clk:1 |
| P1.3 | ctb0_oa1_out | | tcpwm.line_compl[3]:1 | scb[0].uart_rts:1 | tcpwm.tr_in[3] | scb[2].i2c_sda:1 | scb[0].spi_select0:1 |
| P1.4 | ctb0_oa1- | | | | | | scb[0].spi_select1:1 |
| P1.5 | ctb0_oa1+ | | | | | | scb[0].spi_select2:1 |
| P1.6 | ctb0_oa0+ | | | | | | scb[0].spi_select3:1 |
| P1.7 | ctb0_oa1+<br>sar_ext_vref0<br>sar_ext_vref1 | | | | | | scb[2].spi_clk |
| P2.0 | sarmux[0] | prgio[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | sarmux[1] | prgio[0].io[1] | tcpwm.line_compl[4]:0 | | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | sarmux[2] | prgio[0].io[2] | | | | | scb[1].spi_clk:2 |
| P2.3 | sarmux[3] | prgio[0].io[3] | | | | | scb[1].spi_select0:2 |

| Port/Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|---|---|---|---|---|---|---|---|
| P2.4 | sarmux[4] | prgio[0].io[4] | tcpwm.line[0]:1 | | | | scb[1].spi_select1:1 |
| P2.5 | sarmux[5] | prgio[0].io[5] | tcpwm.line_compl[0]:1 | | | | scb[1].spi_select2:1 |
| P2.6 | sarmux[6] | prgio[0].io[6] | tcpwm.line[1]:1 | | | | scb[1].spi_select3:1 |
| P2.7 | sarmux[7] | prgio[0].io[7] | tcpwm.line_compl[1]:1 | | | lpcomp.comp[0]:1 | scb[2].spi_mosi |
| P3.0 | | prgio[1].io[0] | tcpwm.line[0]:0 | scb[1].uart_rx:1 | | scb[1].i2c_scl:2 | scb[1].spi_mosi:0 |
| P3.1 | | prgio[1].io[1] | tcpwm.line_compl[0]:0 | scb[1].uart_tx:1 | | scb[1].i2c_sda:2 | scb[1].spi_miso:0 |
| P3.2 | | prgio[1].io[2] | tcpwm.line[1]:0 | scb[1].uart_cts:1 | | cpuss.swd_data | scb[1].spi_clk:0 |
| P3.3 | | prgio[1].io[3] | tcpwm.line_compl[1]:0 | scb[1].uart_rts:1 | | cpuss.swd_clk | scb[1].spi_select0:0 |
| P3.4 | | prgio[1].io[4] | tcpwm.line[2]:0 | | tcpwm.tr_in[6] | | scb[1].spi_select1:0 |
| P3.5 | | prgio[1].io[5] | tcpwm.line_compl[2]:0 | | | | scb[1].spi_select2:0 |
| P3.6 | | prgio[1].io[6] | tcpwm.line[3]:0 | | | | scb[1].spi_select3:0 |
| P3.7 | | prgio[1].io[7] | tcpwm.line_compl[3]:0 | | | lpcomp.comp[1]:1 | scb[2].spi_miso |
| P4.0 | csd.vref_ext | | | scb[0].uart_rx:0 | | scb[0].i2c_scl:1 | scb[0].spi_mosi:0 |
| P4.1 | csd.cshieldpads | | | scb[0].uart_tx:0 | | scb[0].i2c_sda:1 | scb[0].spi_miso:0 |
| P4.2 | csd.cmodpad | | | scb[0].uart_cts:0 | | lpcomp.comp[0]:0 | scb[0].spi_clk:0 |
| P4.3 | csd.csh_tank | | | scb[0].uart_rts:0 | | lpcomp.comp[1]:0 | scb[0].spi_select0:0 |
| | | | | | | | |

**Table 3. DC Specifications** *(continued)*

Typical values measured at $V_{DD}$ = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| **Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)** | | | | | | | |
| SID22 | IDD17 | $I^2C$ wakeup WDT, and Comparators on | – | 1.7 | 2.2 | mA | 6 MHZ. Max is at 85 °C and 5.5 V. |
| SID25 | IDD20 | $I^2C$ wakeup, WDT, and Comparators on. | – | 2.2 | 2.5 | | 12 MHZ. Max is at 85 °C and 5.5 V. |
| **Sleep Mode, $V_{DDD}$ = 1.71 V to 1.89 V (Regulator bypassed)** | | | | | | | |
| SID28 | IDD23 | $I^2C$ wakeup, WDT, and Comparators on | – | 0.7 | 0.9 | mA | 6 MHZ. Max is at 85 °C and 5.5 V. |
| SID28A | IDD23A | $I^2C$ wakeup, WDT, and Comparators on | – | 1 | 1.2 | mA | 12 MHZ. Max is at 85 °C and 5.5 V. |
| **Deep Sleep Mode, $V_{DD}$ = 1.8 V to 3.6 V (Regulator on)** | | | | | | | |
| SID31 | $I_{DD26}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 60 | µA | Max is at 3.6 V and 85 °C. |
| **Deep Sleep Mode, $V_{DD}$ = 3.6 V to 5.5 V (Regulator on)** | | | | | | | |
| SID34 | $I_{DD29}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 60 | µA | Max is at 5.5 V and 85 °C. |
| **Deep Sleep Mode, $V_{DD}$ = $V_{CCD}$ = 1.71 V to 1.89 V (Regulator bypassed)** | | | | | | | |
| SID37 | $I_{DD32}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 65 | µA | Max is at 1.89 V and 85 °C. |
| **XRES Current** | | | | | | | |
| SID307 | $I_{DD\_XR}$ | Supply current while XRES asserted | – | 2 | 5 | mA | – |

**Table 4. AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID48 | $F_{CPU}$ | CPU frequency | DC | – | 48 | MHz | $1.71 \le V_{DD} \le 5.5$ |
| SID49[3] | $T_{SLEEP}$ | Wakeup from Sleep mode | – | 0 | – | µs | |
| SID50[3] | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | | |

**Note**
2. Guaranteed by characterization.

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID73 | $T_{FALLS}$ | Fall time in slow strong mode | 10 | – | 60 | – | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID74 | $F_{GPIOUT1}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Fast strong mode | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO $F_{OUT}$; 1.71 V≤ $V_{DDD}$≤ 3.3 V Fast strong mode | – | – | 16.7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Slow strong mode | – | – | 7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO $F_{OUT}$; 1.71 V ≤ $V_{DDD}$ ≤ 3.3 V Slow strong mode. | – | – | 3.5 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | $F_{GPIOIN}$ | GPIO input operating frequency; 1.71 V ≤ $V_{DDD}$ ≤ 5.5 V | – | – | 48 | | 90/10% $V_{IO}$ |

*XRES*

**Table 7. XRES DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID77 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID78 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | | |
| SID79 | $R_{PULLUP}$ | Pull-up resistor | – | 60 | – | kΩ | – |
| SID80 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID81[5] | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Typical hysteresis is 200 mV for $V_{DD}$ > 4.5 V |
| SID82 | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | |

**Table 8. XRES AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID83[5] | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | µs | – |
| BID194[5] | $T_{RESETWAKE}$ | Wake-up time from reset release | – | – | 2.7 | ms | – |

**Note**
5. Guaranteed by characterization.

**Table 10. Comparator DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID84 | $V_{OFFSET1}$ | Input offset voltage, Factory trim | – | – | ±10 | mV | |
| SID85 | $V_{OFFSET2}$ | Input offset voltage, Custom trim | – | – | ±4 | | |
| SID86 | $V_{HYST}$ | Hysteresis when enabled | – | 10 | 35 | | |
| SID87 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$-0.1 | V | Modes 1 and 2 |
| SID247 | $V_{ICM2}$ | Input common mode voltage in low power mode | 0 | – | $V_{DDD}$ | | |
| SID247A | $V_{ICM3}$ | Input common mode voltage in ultra low power mode | 0 | – | $V_{DDD}$-1.15 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID88 | $C_{MRR}$ | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD}$ ≥ 2.7V |
| SID88A | $C_{MRR}$ | Common mode rejection ratio | 42 | – | – | | $V_{DDD}$ ≤ 2.7V |
| SID89 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | |
| SID248 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | | |
| SID259 | $I_{CMP3}$ | Block current in ultra low-power mode | – | – | 6 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID90 | $Z_{CMP}$ | DC Input impedance of comparator | 35 | – | – | MΩ | |

**Table 11. Comparator AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID91 | TRESP1 | Response time, normal mode, 50 mV overdrive | – | 38 | 110 | ns | |
| SID258 | TRESP2 | Response time, low power mode, 50 mV overdrive | – | 70 | 200 | | |
| SID92 | TRESP3 | Response time, ultra-low power mode, 200 mV overdrive | – | 2.3 | 15 | µs | $V_{DDD}$ ≥ 2.2 V at –40 °C |

**Table 12. Temperature Sensor Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID93 | TSENSACC | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

**Table 13. SAR Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| **SAR ADC DC Specifications** | | | | | | | |
| SID94 | A_RES | Resolution | – | – | 12 | bits | |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 4 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | | Yes. |
| SID98 | A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference. |

**Table 13. SAR Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR | Current consumption | – | – | 1 | mA | |
| SID101 | A_VINS | Input voltage range - single ended | $V_{SS}$ | – | $V_{DDA}$ | V | |
| SID102 | A_VIND | Input voltage range - differential[ | $V_{SS}$ | – | $V_{DDA}$ | V | |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | KΩ | |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | |
| SID260 | VREFSAR | Trimmed internal reference to SAR | – | – | TBD | V | |
| **SAR ADC AC Specifications** | | | | | | | |
| SID106 | A_PSRR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| SID108 | A_SAMP | Sample rate | – | – | 1 | Msps | |
| SID109 | A_SNR | Signal-to-noise and distortion ratio (SINAD) | 65 | – | – | dB | $F_{IN}$ = 10 kHz |
| SID110 | A_BW | Input bandwidth without aliasing | – | – | A_samp/2 | kHz | |
| SID111 | A_INL | Integral non linearity. $V_{DD}$ = 1.71 to 5.5, 1 Msps | –1.7 | – | 2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID111A | A_INL | Integral non linearity. $V_{DDD}$ = 1.71 to 3.6, 1 Msps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1.71 to $V_{DD}$ |
| SID111B | A_INL | Integral non linearity. $V_{DD}$ = 1.71 to 5.5, 500 ksps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID112 | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 5.5, 1 Msps | –1 | _ | 2.2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID112A | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 3.6, 1 Msps | –1 | _ | 2 | LSB | $V_{REF}$ = 1.71 to $V_{DD}$ |
| SID112B | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 5.5, 500 ksps | –1 | _ | 2.2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID113 | A_THD | Total harmonic distortion | – | – | –65 | dB | Fin = 10 kHz |
| SID261 | FSARINTREF | SAR operating speed without external ref. bypass | _ | _ | 100 | ksps | 12-bit resolution |

*CSD*

**Table 14. CSD and IDAC Specifications**

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD}$ > 2 V (with ripple), 25 °C $T_A$, Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD}$ > 1.75V (with ripple), 25 °C $T_A$, Parasitic Capacitance ($C_P$) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | µA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator. |
| SID.CSD#15 | $V_{REF}$ | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#15A | VREF_EXT | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | µA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | µA | |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA}$ –0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA}$ > 2 V. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID314A | IDAC1CRT2 | Output current of IDAC1(7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID314B | IDAC1CRT3 | Output current of IDAC1(7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID314D | IDAC1CRT22 | Output current of IDAC1(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID314E | IDAC1CRT32 | Output current of IDAC1(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID315D | IDAC2CRT22 | Output current of IDAC2(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID315E | IDAC2CRT32 | Output current of IDAC2(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | µA | LSB = 37.5-nA typ. |

**Table 14. CSD and IDAC Specifications** *(continued)*

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID315G | IDAC3CRT23 | Output current of IDAC in 8-bit mode in medium range | 69 | – | 82 | µA | LSB = 300-nA typ. |
| SID315H | IDAC3CRT33 | Output current of IDAC in 8-bit mode in high range | 540 | – | 660 | µA | LSB = 2.4-µA typ. |
| SID320 | IDACOFFSET | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode |
| SID321 | IDACGAIN | Full-scale error less offset | – | – | ±10 | % | |
| SID322 | IDACMISMATCH1 | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | IDACMISMATCH2 | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 5.6 | LSB | LSB = 300-nA typ. |
| SID322B | IDACMISMATCH3 | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 6.8 | LSB | LSB = 2.4-µA typ. |
| SID323 | IDACSET8 | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | IDACSET7 | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

**Table 15. 10-bit CapSense ADC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SIDA95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | Defined by AMUX Bus. |
| SIDA97 | A-MONO | Monotonicity | – | – | – | Yes | |
| SIDA98 | A_GAINERR | Gain error | – | – | ±2 | % | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA99 | A_OFFSET | Input offset voltage | – | – | 3 | mV | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA100 | A_ISAR | Current consumption | – | – | 0.25 | mA | |
| SIDA101 | A_VINS | Input voltage range - single ended | $V_{SSA}$ | – | $V_{DDA}$ | V | |
| SIDA103 | A_INRES | Input resistance | – | 2.2 | – | KΩ | |
| SIDA104 | A_INCAP | Input capacitance | – | 20 | – | pF | |
| SIDA106 | A_PSRR | Power supply rejection ratio | – | 60 | – | dB | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA107 | A_TACQ | Sample acquisition time | – | 1 | – | µs | |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 21.3 | µs | Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 85.3 | µs | Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time. |

**Table 15. 10-bit CapSense ADC Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SIDA109 | A_SND | Signal-to-noise and Distortion ratio (SINAD) | – | 61 | – | dB | With 10-Hz input sine wave, external 2.4-V reference, $V_{REF}$ (2.4 V) mode |
| SIDA110 | A_BW | Input bandwidth without aliasing | – | – | 22.4 | KHz | 8-bit resolution |
| SIDA111 | A_INL | Integral Non Linearity. 1 ksps | – | – | 2 | LSB | $V_{REF}$ = 2.4 V or greater |
| SIDA112 | A_DNL | Differential Non Linearity. 1 ksps | – | – | 1 | LSB | |

## Digital Peripherals

*Timer Counter Pulse-Width Modulator (TCPWM)*

**Table 16. TCPWM Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | µA | All modes (TCPWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | – | – | 155 | | All modes (TCPWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | – | – | 650 | | All modes (TCPWM) |
| SID.TCPWM.3 | $TCPWM_{FREQ}$ | Operating frequency | – | – | Fc | MHz | Fc max = CLK_SYS Maximum = 48 MHz |
| SID.TCPWM.4 | $TPWM_{ENEXT}$ | Input trigger pulse width | 2/Fc | – | – | ns | For all trigger events[7] |
| SID.TCPWM.5 | $TPWM_{EXT}$ | Output trigger pulse widths | 2/Fc | – | – | | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | $TC_{RES}$ | Resolution of counter | 1/Fc | – | – | | Minimum time between successive counts |
| SID.TCPWM.5B | $PWM_{RES}$ | PWM resolution | 1/Fc | – | – | | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | $Q_{RES}$ | Quadrature inputs resolution | 1/Fc | – | – | | Minimum pulse width between Quadrature phase inputs |

*$I^2C$*

**Table 17. Fixed $I^2C$ DC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID149 | $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 50 | µA | – |
| SID150 | $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 135 | | – |
| SID151 | $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 310 | | – |
| SID152 | $I_{I2C4}$ | $I^2C$ enabled in Deep Sleep mode | – | – | 1.4 | | |

**Table 18. Fixed $I^2C$ AC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Msps | – |

**Notes**
7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

**Note**
8. Guaranteed by characterization.

**Table 21. UART DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbps | – | – | 55 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbps | – | – | 312 | µA | – |

**Table 22. UART AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 23. LCD Direct Drive DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID154 | $I_{LCDLOW}$ | Operating current in low power mode | – | 5 | – | µA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | $I_{LCDOP1}$ | LCD system operating current Vbias = 5 V | – | 2 | – | mA | 32 × 4 segments. 50 Hz. 25 °C |
| SID158 | $I_{LCDOP2}$ | LCD system operating current Vbias = 3.3 V | – | 2 | – | | 32 × 4 segments. 50 Hz. 25 °C |

**Table 24. LCD Direct Drive AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID159 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

**Note**
9. Guaranteed by characterization.

**Table 34. Watch Crystal Oscillator (WCO) Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID398 | FWCO | Crystal Frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | µW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal Load Capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal Shunt Capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating Current (high power mode) | – | – | 8 | uA | |
| SID406 | IWCO2 | Operating Current (low power mode) | – | – | 1 | uA | |

**Table 35. External Clock Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID305[13] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306[13] | ExtClkDuty | Duty cycle; measured at $V_{DD/2}$ | 45 | – | 55 | % | – |

**Table 36. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID262[13] | $T_{CLKSWITCH}$ | System clock source switching time | 3 | – | 4 | Periods | – |

**Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

**Note**
13. Guaranteed by characterization.

## Packaging

The PSoC 4100S will be offered in 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball WLCSP packages. Package dimensions and Cypress drawing numbers are in the following table.

**Table 38. Package List**

| Spec ID# | Package | Description | Package Dwg |
|---|---|---|---|
| BID20 | 48-pin TQFP | 7 × 7 × 1.4-mm height with 0.5-mm pitch | 51-85135 |
| BID20A | 44-pin TQFP | 10 × 10 × 1.6-mm height with 0.8-mm pitch | 51-85064 |
| BID27 | 40-pin QFN | 6 × 6 × 0.6-mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32-pin QFN | 5 × 5 × 0.6-mm height with 0.5-mm pitch | 001-42168 |
| BID34D | 35-ball WLCSP | 2.6 × 2.1 × 0.48-mm height with 0.35-mm pitch | 002-09958 |

**Table 39. Package Thermal Characteristics**

| Parameter | Description | Package | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating Ambient temperature | | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ | 48-pin TQFP | – | 74.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 48-pin TQFP | – | 35.7 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 44-pin TQFP | – | 57.2 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 44-pin TQFP | – | 17.5 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 40-pin QFN | – | 17.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 40-pin QFN | – | 2.8 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 32-pin QFN | – | 19.9 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 32-pin QFN | – | 4.3 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 35-ball WLCSP | – | 43 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 35-ball WLCSP | – | 0.3 | – | °C/Watt |

**Table 40. Solder Reflow Peak Temperature**

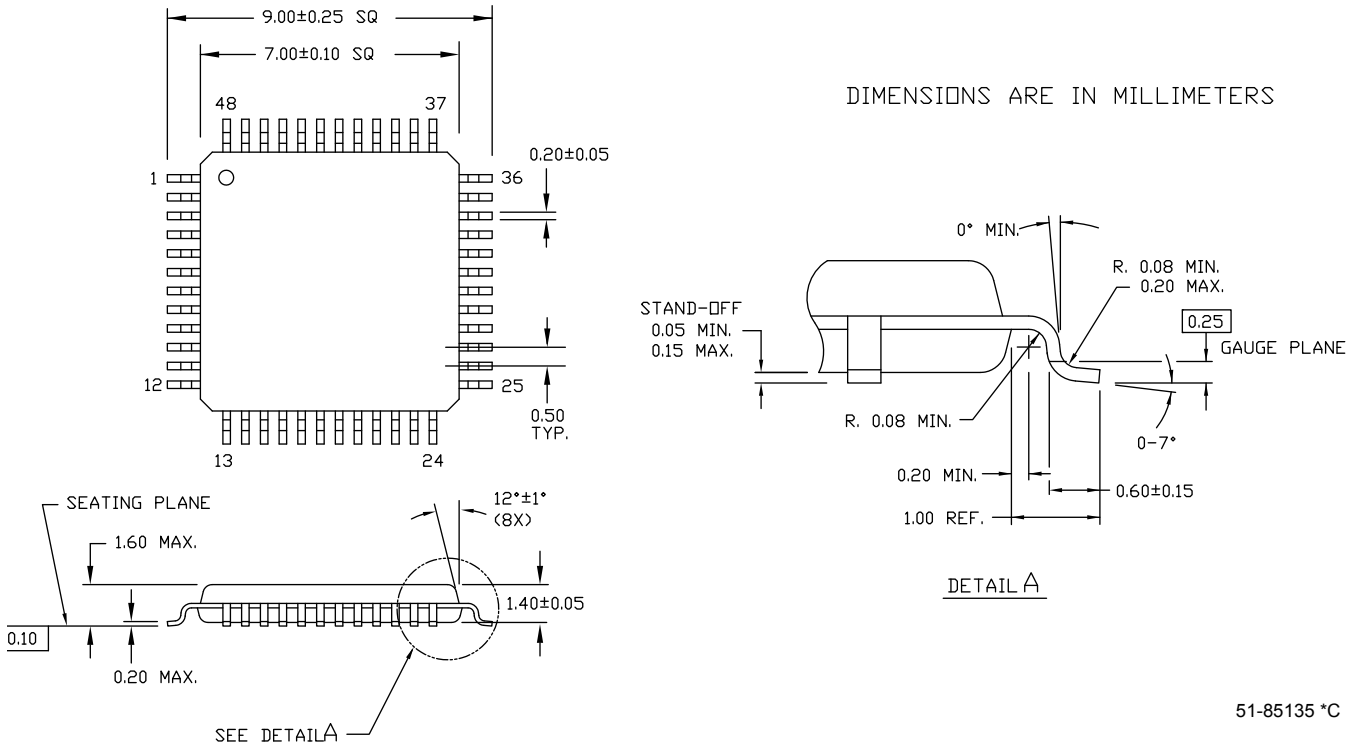
| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| All | 260 °C | 30 seconds |

**Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020**

| Package | MSL |
|---|---|
| All except WLCSP | MSL 3 |
| 35-ball WLCSP | MSL 1 |

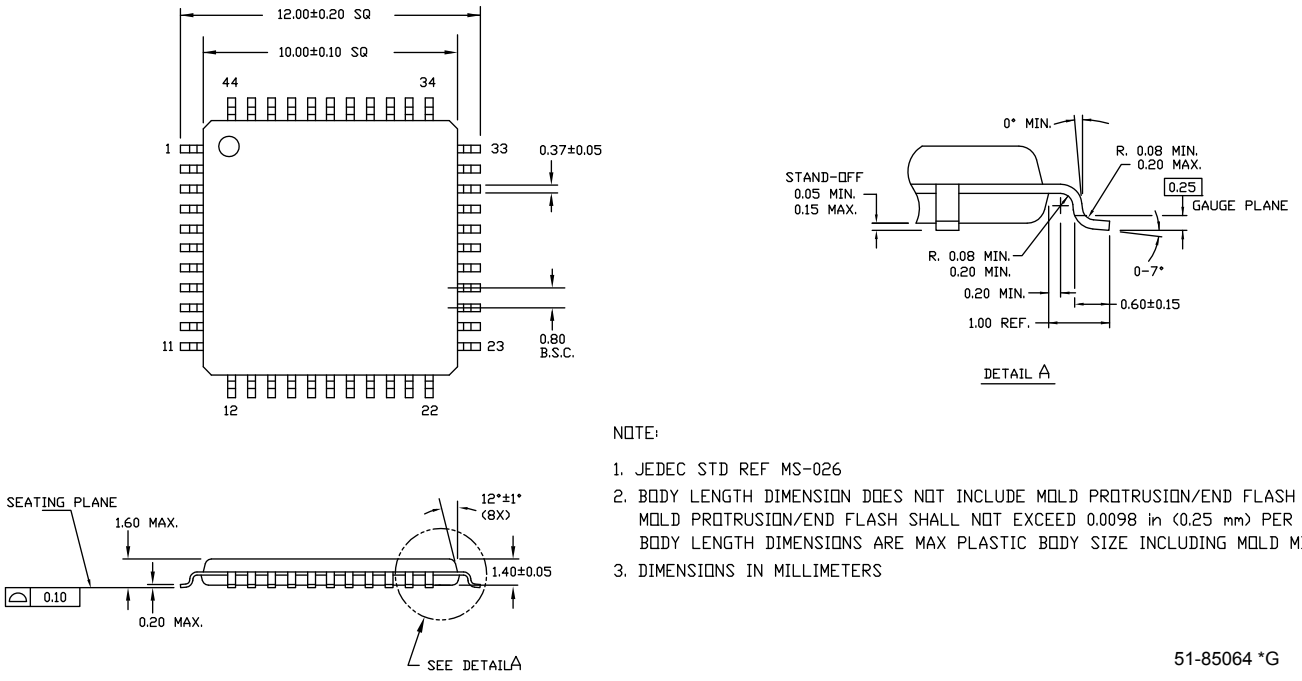
## Package Diagrams

**Figure 6. 48-pin TQFP Package Outline**




51-85135 *C

**Figure 7. 44-pin TQFP Package Outline**

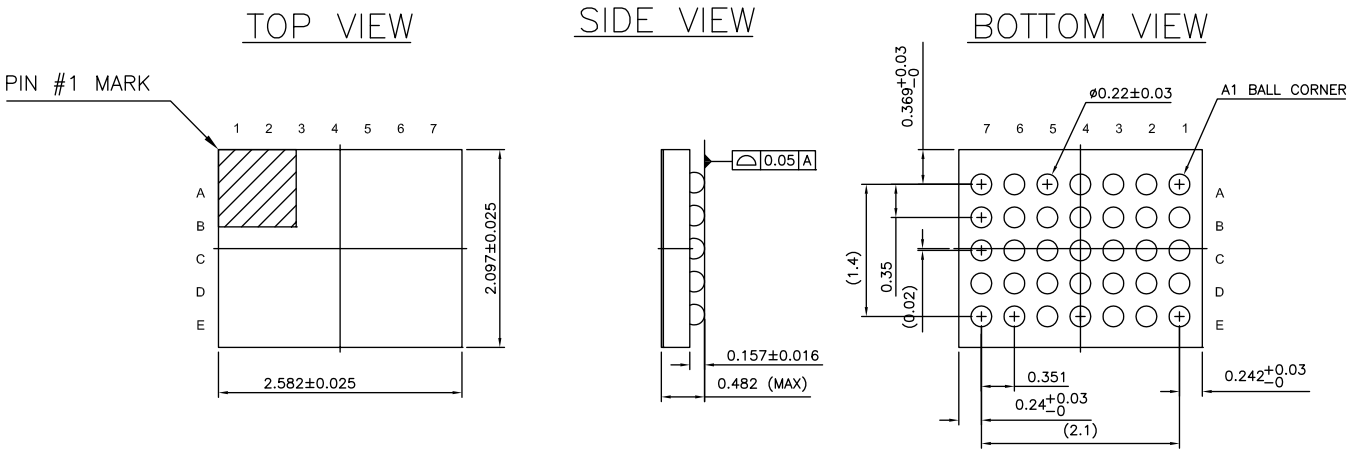



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

**Figure 10. 35-Ball WLCSP Package Outline**




ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-09958 *C

## Acronyms

**Table 42. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 42. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

**Table 42. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

**Table 42. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |