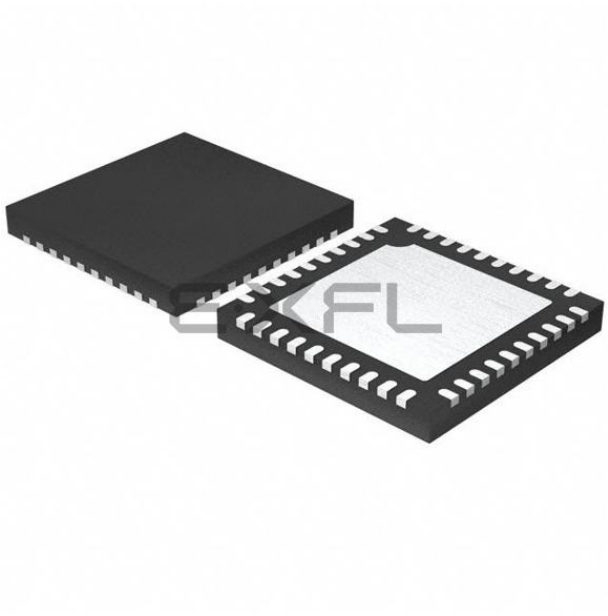

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125lqi-s413

Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1. Pin List

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				

Alternate Pin Functions

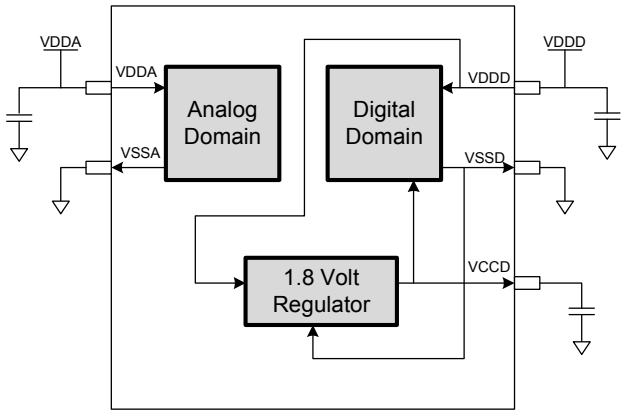
Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 4. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4100S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100S supplies the internal logic and its output is connected to the V_{CCD} pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

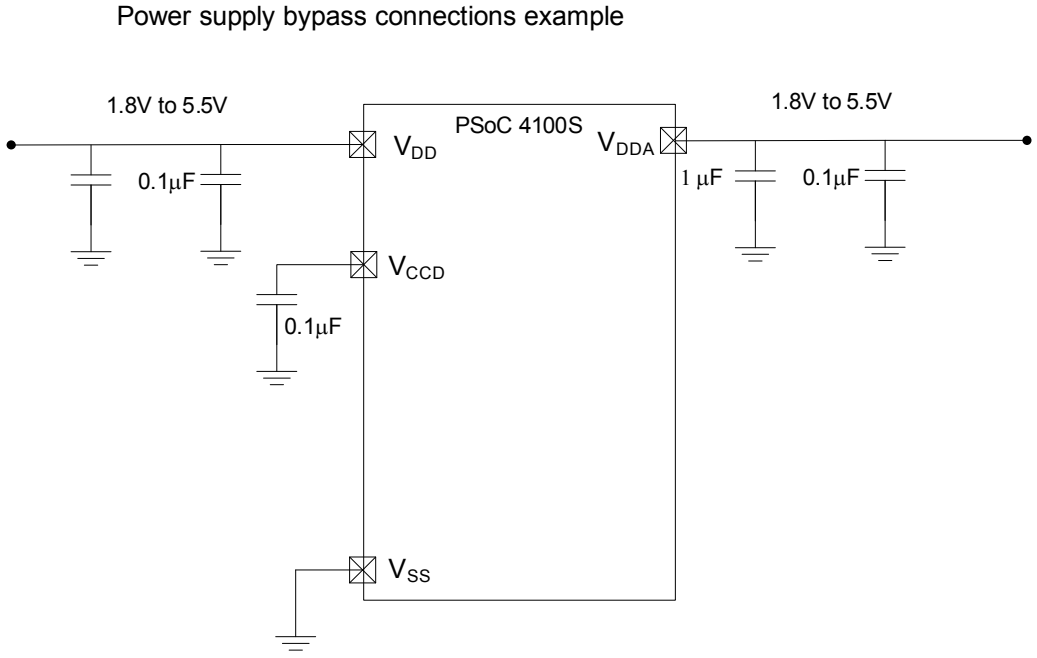
Mode 2: 1.8 V ±5% External Supply

In this mode, the PSoC 4100S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active



GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[3]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		CMOS Input
SID241	V_{IH}[3]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[3]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDD} ≥ 2.7 V
SID68[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF

Notes
3. V_{IH} must not exceed V_{DDD} + 0.2 V.
4. Guaranteed by characterization.

Table 6. GPIO AC Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DDD}≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48		90/10% V_{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81[5]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[5]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note
5. Guaranteed by characterization.

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	power=hi, Iload=10 mA	0.5	–	V_{DDA} -0.5	V	–
SID284	V_{OUT_2}	power=hi, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID285	V_{OUT_3}	power=med, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID286	V_{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V_{DDA} -0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA}-0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA}-0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA}-0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA}-0.2 V, Output is 0.2 V to V_{DDA}-0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA}-0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, T_{rise}=T_{fall} (approx.)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–		25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–		25 °C

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_9	$G_{BW\_LOW\_M!}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V_{DDA}-0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_19	$I_{OUT\_HI\_M!}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

Note
6. Guaranteed by characterization.

Table 10. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD}-0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD}-1.15		V_{DDD} ≥ 2.2 V at –40 °C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	
SID248	I_{CMP2}	Block current, low power mode	–	–	100		
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	6		V_{DDD} ≥ 2.2 V at –40 °C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	

Table 11. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V_{DDD} ≥ 2.2 V at –40 °C

Table 12. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 13. SAR Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.

CSD

Table 14. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25 °C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5-nA typ.

Table 15. 10-bit CapSense ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 16. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[7]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

I^2C

Table 17. Fixed I^2C DC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4		

Table 18. Fixed I^2C AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

Notes
7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

Note
8. Guaranteed by characterization.

Table 19. SPI DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 20. SPI AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

Memory

Table 25. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[10]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (64 KB)	–	–	35		–
SID180[11]	$T_{DEVPROG}$[10]	Total device program time	–	–	7	Seconds	–
SID181[11]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[11]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A[11]	–	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[11]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 28. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[11]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes
10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

SWD Interface

Table 29. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T		–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Internal Main Oscillator

Table 30. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 31. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 32. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[12]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 33. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[12]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note
12. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC 4100S family are listed in the following table.

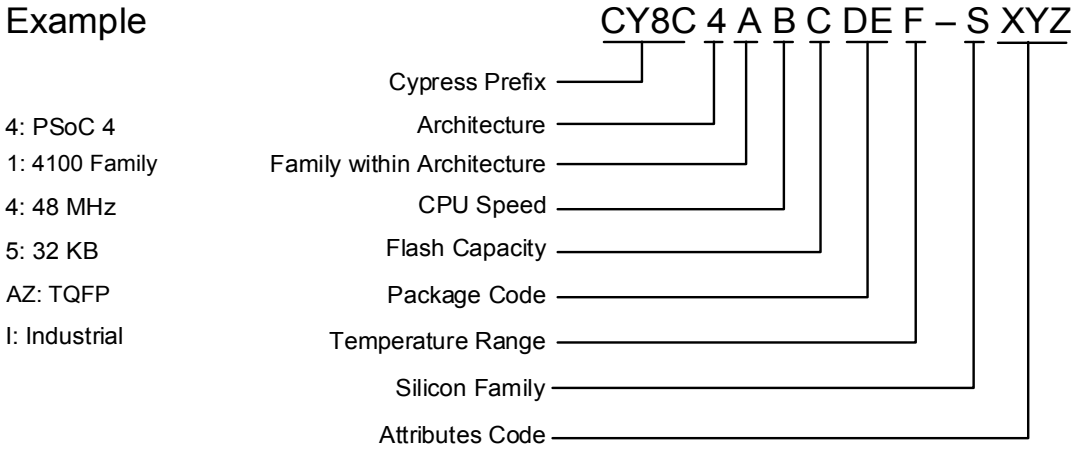
Category	MPN	Features													Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-WLCSP (0.35mm pitch)	32-QFN	40-QFN	48-TQFP	44-TQFP
4124	CY8C4124FNI-S403	24	16	4	2	0	1	0		2	5	2	8	31	X				
	CY8C4124FNI-S413	24	16	4	2	1	1	0		2	5	2	16	31	X				
	CY8C4124LQI-S412	24	16	4	2	1	1	0		2	5	2	16	27		X			
	CY8C4124LQI-S413	24	16	4	2	1	1	0		2	5	2	16	34			X		
	CY8C4124AZI-S413	24	16	4	2	1	1	0		2	5	2	16	36				X	
	CY8C4124FNI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4124LQI-S432	24	16	4	2	1	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4124LQI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4124AZI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	36				X	
4125	CY8C4125FNI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4125LQI-S422	24	32	4	2	0	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4125LQI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4125AZI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36				X	
	CY8C4125AXI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36					X
	CY8C4125FNI-S413	24	32	4	2	1	1	0		2	5	2	16	31	X				
	CY8C4125LQI-S412	24	32	4	2	1	1	0		2	5	2	16	27		X			
	CY8C4125LQI-S413	24	32	4	2	1	1	0		2	5	2	16	34			X		
	CY8C4125AZI-S413	24	32	4	2	1	1	0		2	5	2	16	36				X	
	CY8C4125FNI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4125LQI-S432	24	32	4	2	1	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4125LQI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4125AZI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36				X	
	CY8C4125AXI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36					X
4126	CY8C4126AZI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36				X	
	CY8C4126AXI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36					X
	CY8C4126AZI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36				X	
	CY8C4126AXI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36					X
4145	CY8C4145AZI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36				X	
	CY8C4145AXI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36					X
	CY8C4145AXI-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36					X
4146	CY8C4146FNI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	31	X				
	CY8C4146LQI-S422	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27		X			
	CY8C4146LQI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	34			X		
	CY8C4146AZI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36				X	
	CY8C4146AXI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36					X
	CY8C4146FNI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X				
	CY8C4146LQI-S432	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27		X			
	CY8C4146LQI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	34			X		
	CY8C4146AZI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36				X	
	CY8C4146AXI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36					X

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

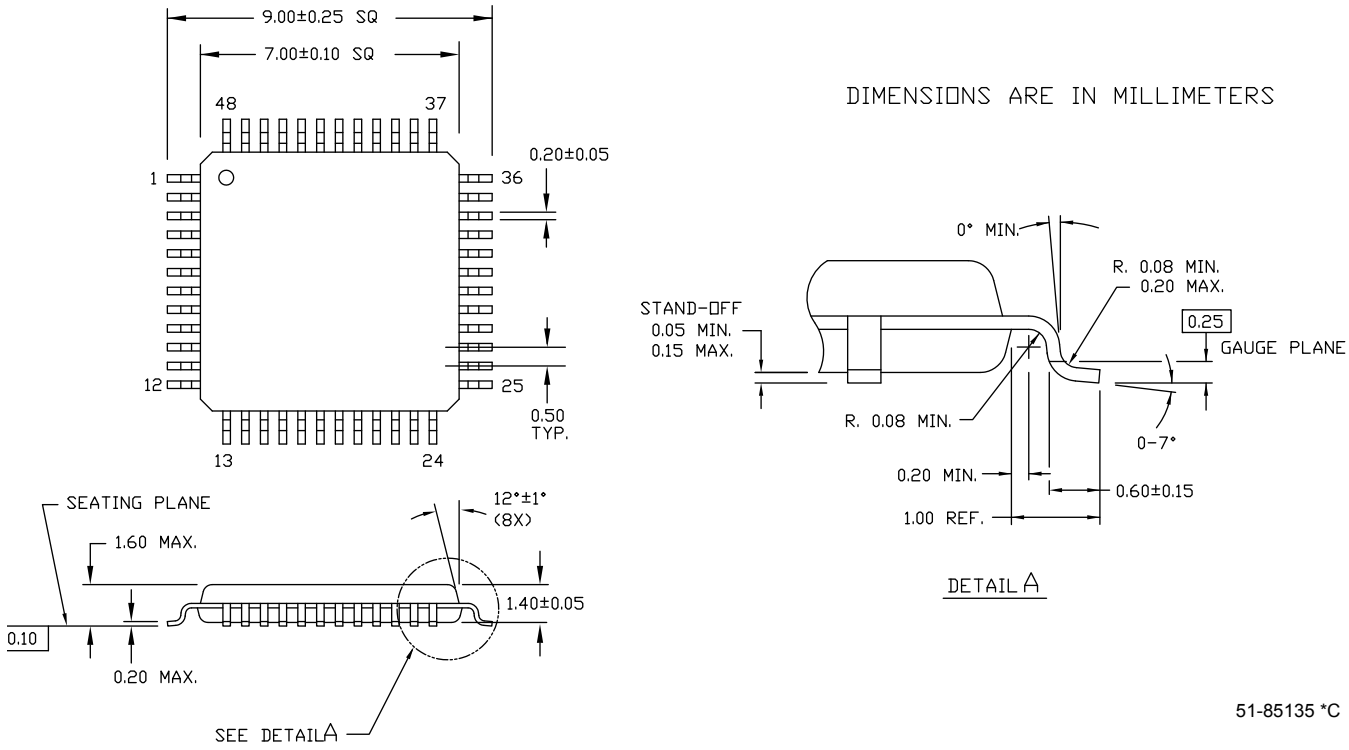
The following is an example of a part number:

Example



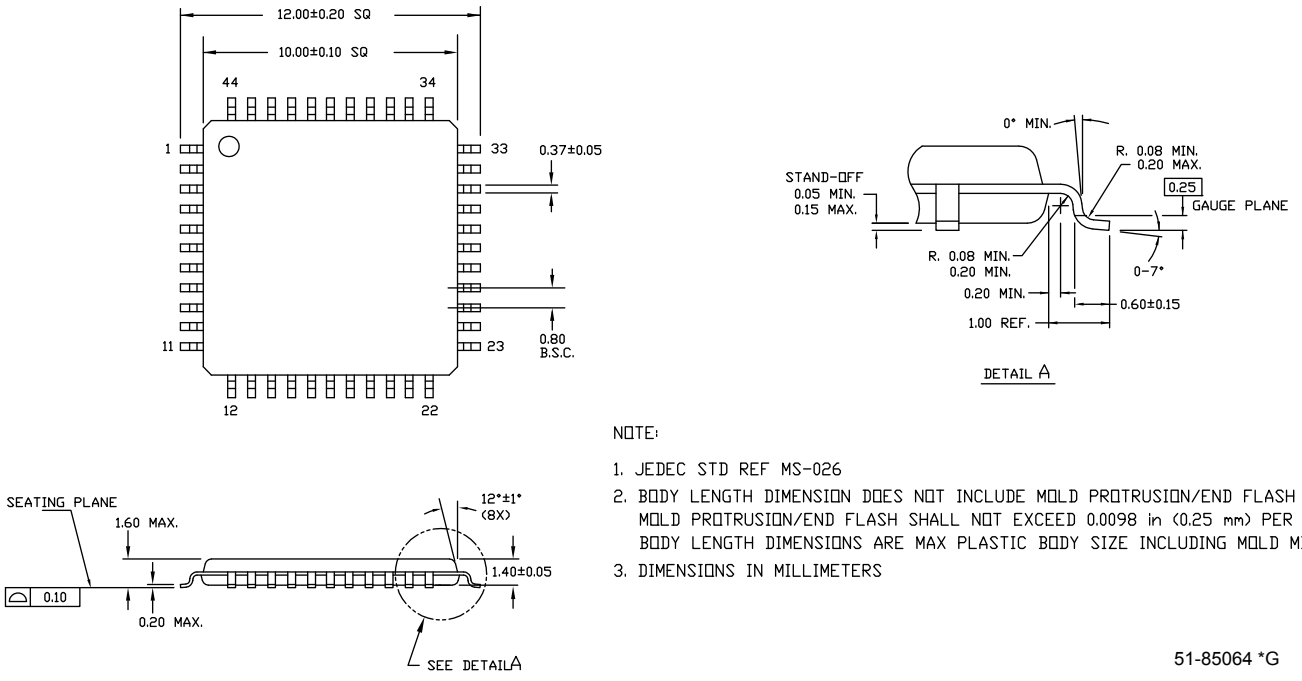
Package Diagrams

Figure 6. 48-pin TQFP Package Outline



51-85135 *C

Figure 7. 44-pin TQFP Package Outline

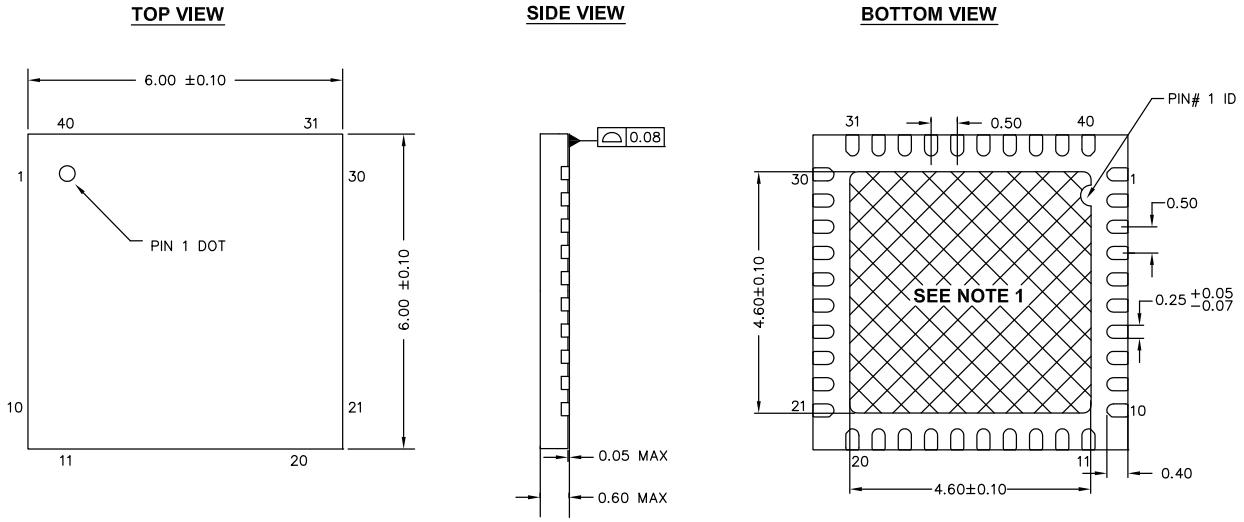


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Figure 8. 40-pin QFN Package Outline

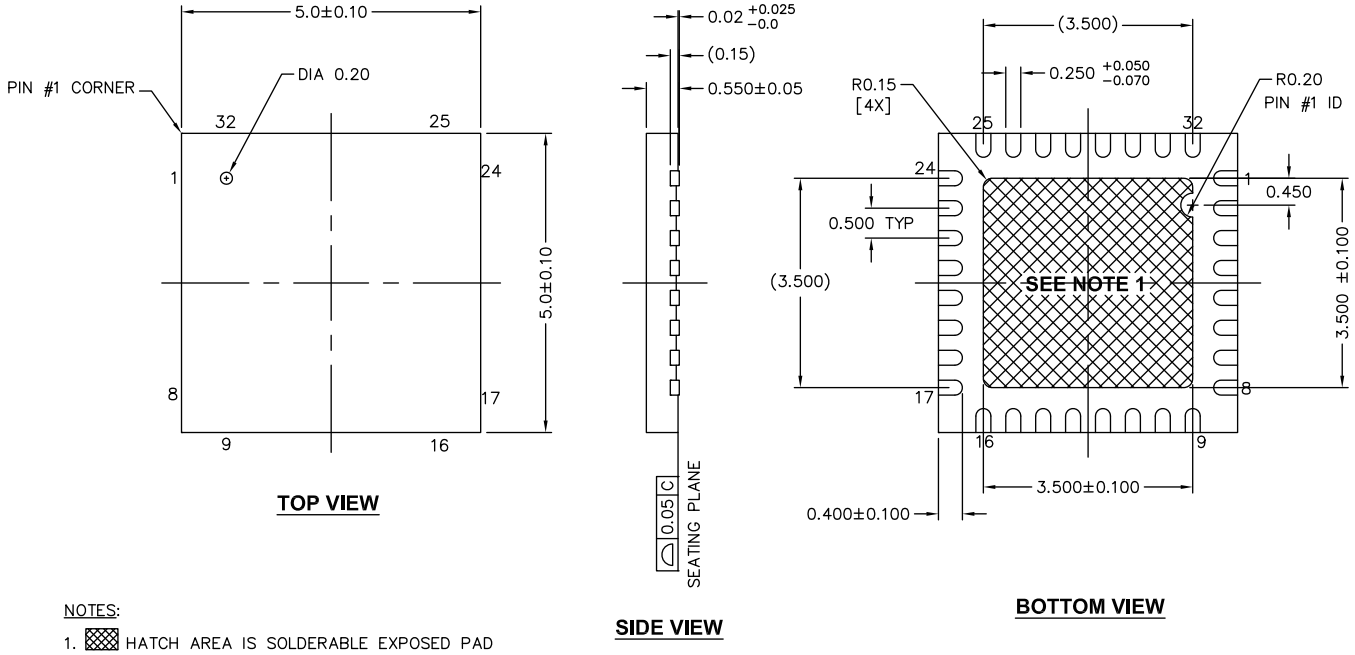


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 9. 32-pin QFN Package Outline



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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