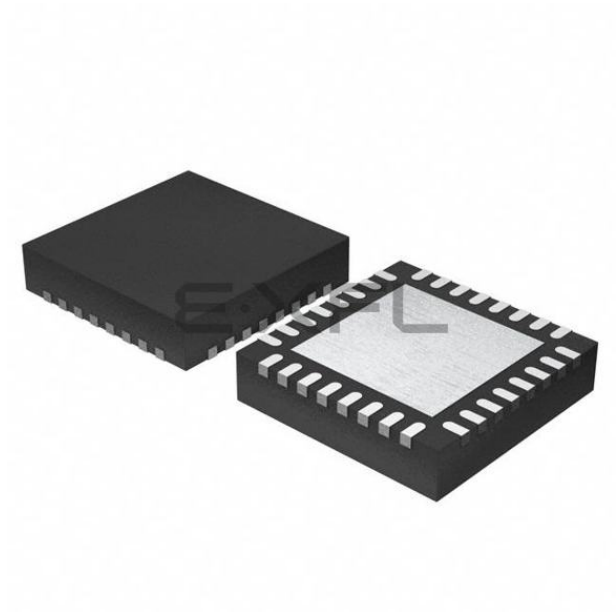

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125lqi-s432 |

# Functional Definition

## CPU and Memory Subsystem

### *CPU*

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

### *Flash*

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

### *SRAM*

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

### *SROM*

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### *Power System*

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

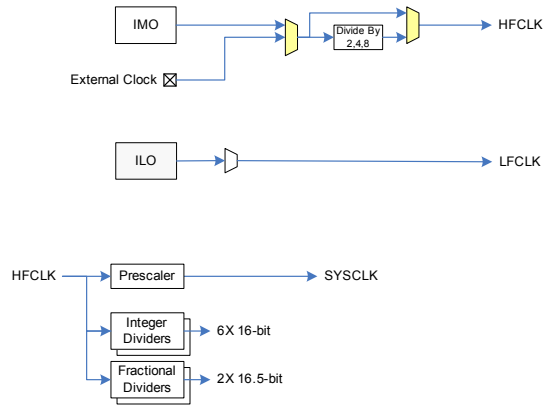
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

### *Clock System*

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

**Figure 2. PSoC 4100S MCU Clocking Architecture**




The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

### *IMO Clock Source*

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

### *ILO Clock Source*

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### *Watch Crystal Oscillator (WCO)*

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

### *Watchdog Timer*

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

## Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

**Table 1. Pin List**

| 48-TQFP | | 44-TQFP | | 40-QFN | | 32-QFN | | 35-CSP | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 28 | P0.0 | 24 | P0.0 | 22 | P0.0 | 17 | P0.0 | C3 | P0.0 |
| 29 | P0.1 | 25 | P0.1 | 23 | P0.1 | 18 | P0.1 | A5 | P0.1 |
| 30 | P0.2 | 26 | P0.2 | 24 | P0.2 | 19 | P0.2 | A4 | P0.2 |
| 31 | P0.3 | 27 | P0.3 | 25 | P0.3 | 20 | P0.3 | A3 | P0.3 |
| 32 | P0.4 | 28 | P0.4 | 26 | P0.4 | 21 | P0.4 | B3 | P0.4 |
| 33 | P0.5 | 29 | P0.5 | 27 | P0.5 | 22 | P0.5 | A6 | P0.5 |
| 34 | P0.6 | 30 | P0.6 | 28 | P0.6 | 23 | P0.6 | B4 | P0.6 |
| 35 | P0.7 | 31 | P0.7 | 29 | P0.7 | | | B5 | P0.7 |
| 36 | XRES | 32 | XRES | 30 | XRES | 24 | XRES | B6 | XRES |
| 37 | VCCD | 33 | VCCD | 31 | VCCD | 25 | VCCD | A7 | VCCD |
| 38 | VSSD | | | DN | VSSD | 26 | VSSD | B7 | VSS |
| 39 | VDDD | 34 | VDDD | 32 | VDDD | | | C7 | VDD |
| 40 | VDDA | 35 | VDDA | 33 | VDDA | 27 | VDD | C7 | VDD |
| 41 | VSSA | 36 | VSSA | 34 | VSSA | 28 | VSSA | B7 | VSS |
| 42 | P1.0 | 37 | P1.0 | 35 | P1.0 | 29 | P1.0 | C4 | P1.0 |
| 43 | P1.1 | 38 | P1.1 | 36 | P1.1 | 30 | P1.1 | C5 | P1.1 |
| 44 | P1.2 | 39 | P1.2 | 37 | P1.2 | 31 | P1.2 | C6 | P1.2 |
| 45 | P1.3 | 40 | P1.3 | 38 | P1.3 | 32 | P1.3 | D7 | P1.3 |
| 46 | P1.4 | 41 | P1.4 | 39 | P1.4 | | | D4 | P1.4 |
| 47 | P1.5 | 42 | P1.5 | | | | | D5 | P1.5 |
| 48 | P1.6 | 43 | P1.6 | | | | | D6 | P1.6 |
| 1 | P1.7/VREF | 44 | P1.7/VREF | 40 | P1.7/VREF | 1 | P1.7/VREF | E7 | P1.7/VREF |
| | | 1 | VSSD | | | | | | |
| 2 | P2.0 | 2 | P2.0 | 1 | P2.0 | 2 | P2.0 | | |
| 3 | P2.1 | 3 | P2.1 | 2 | P2.1 | 3 | P2.1 | | |
| 4 | P2.2 | 4 | P2.2 | 3 | P2.2 | 4 | P2.2 | D3 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | 4 | P2.3 | 5 | P2.3 | E4 | P2.3 |
| 6 | P2.4 | 6 | P2.4 | 5 | P2.4 | | | E5 | P2.4 |
| 7 | P2.5 | 7 | P2.5 | 6 | P2.5 | 6 | P2.5 | E6 | P2.5 |
| 8 | P2.6 | 8 | P2.6 | 7 | P2.6 | 7 | P2.6 | E3 | P2.6 |
| 9 | P2.7 | 9 | P2.7 | 8 | P2.7 | 8 | P2.7 | E2 | P2.7 |
| 10 | VSSD | 10 | VSSD | 9 | VSSD | | | | |
| 12 | P3.0 | 11 | P3.0 | 10 | P3.0 | 9 | P3.0 | E1 | P3.0 |
| 13 | P3.1 | 12 | P3.1 | 11 | P3.1 | 10 | P3.1 | D2 | P3.1 |
| 14 | P3.2 | 13 | P3.2 | 12 | P3.2 | 11 | P3.2 | D1 | P3.2 |
| 16 | P3.3 | 14 | P3.3 | 13 | P3.3 | 12 | P3.3 | C1 | P3.3 |
| 17 | P3.4 | 15 | P3.4 | 14 | P3.4 | | | C2 | P3.4 |
| 18 | P3.5 | 16 | P3.5 | 15 | P3.5 | | | | |

**Table 1. Pin List** *(continued)*

| 48-TQFP | | 44-TQFP | | 40-QFN | | 32-QFN | | 35-CSP | |
|---|---|---|---|---|---|---|---|---|---|
| **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** |
| 19 | P3.6 | 17 | P3.6 | 16 | P3.6 | | | | |
| 20 | P3.7 | 18 | P3.7 | 17 | P3.7 | | | | |
| 21 | VDDD | 19 | VDDD | | | | | | |
| 22 | P4.0 | 20 | P4.0 | 18 | P4.0 | 13 | P4.0 | B1 | P4.0 |
| 23 | P4.1 | 21 | P4.1 | 19 | P4.1 | 14 | P4.1 | B2 | P4.1 |
| 24 | P4.2 | 22 | P4.2 | 20 | P4.2 | 15 | P4.2 | A2 | P4.2 |
| 25 | P4.3 | 23 | P4.3 | 21 | P4.3 | 16 | P4.3 | A1 | P4.3 |

**Notes:** Pins 11, 15, 26, and 27 are No Connects (NC) on the 48-pin TQFP.

**Descriptions of the Power pins are as follows:**

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

### Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

| Port/Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|---|---|---|---|---|---|---|---|
| P0.0 | lpcomp.in_p[0] | | | | tcpwm.tr_in[0] | scb[2].i2c_scl:0 | scb[0].spi_select1:0 |
| P0.1 | lpcomp.in_n[0] | | | | tcpwm.tr_in[1] | scb[2].i2c_sda:0 | scb[0].spi_select2:0 |
| P0.2 | lpcomp.in_p[1] | | | | | | scb[0].spi_select3:0 |
| P0.3 | lpcomp.in_n[1] | | | | | | scb[2].spi_select0 |
| P0.4 | wco.wco_in | | | scb[1].uart_rx:0 | scb[2].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:1 |
| P0.5 | wco.wco_out | | | scb[1].uart_tx:0 | scb[2].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:1 |
| P0.6 | | | srss.ext_clk | scb[1].uart_cts:0 | scb[2].uart_tx:1 | | scb[1].spi_clk:1 |
| P0.7 | | | tcpwm.line[0]:2 | scb[1].uart_rts:0 | | | scb[1].spi_select0:1 |
| P1.0 | ctb0_oa0+ | | tcpwm.line[2]:1 | scb[0].uart_rx:1 | | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | ctb0_oa0- | | tcpwm.line_compl[2]:1 | scb[0].uart_tx:1 | | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | ctb0_oa0_out | | tcpwm.line[3]:1 | scb[0].uart_cts:1 | tcpwm.tr_in[2] | scb[2].i2c_scl:1 | scb[0].spi_clk:1 |
| P1.3 | ctb0_oa1_out | | tcpwm.line_compl[3]:1 | scb[0].uart_rts:1 | tcpwm.tr_in[3] | scb[2].i2c_sda:1 | scb[0].spi_select0:1 |
| P1.4 | ctb0_oa1- | | | | | | scb[0].spi_select1:1 |
| P1.5 | ctb0_oa1+ | | | | | | scb[0].spi_select2:1 |
| P1.6 | ctb0_oa0+ | | | | | | scb[0].spi_select3:1 |
| P1.7 | ctb0_oa1+<br>sar_ext_vref0<br>sar_ext_vref1 | | | | | | scb[2].spi_clk |
| P2.0 | sarmux[0] | prgio[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | sarmux[1] | prgio[0].io[1] | tcpwm.line_compl[4]:0 | | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | sarmux[2] | prgio[0].io[2] | | | | | scb[1].spi_clk:2 |
| P2.3 | sarmux[3] | prgio[0].io[3] | | | | | scb[1].spi_select0:2 |

## Development Support

The PSoC 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

*GPIO*

**Table 5. GPIO DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID57 | $V_{IH}$[3] | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID58 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | | CMOS Input |
| SID241 | $V_{IH}$[3] | LVTTL input, $V_{DDD}$ < 2.7 V | 0.7 × $V_{DDD}$ | – | – | | – |
| SID242 | $V_{IL}$ | LVTTL input, $V_{DDD}$ < 2.7 V | – | – | 0.3 × $V_{DDD}$ | | – |
| SID243 | $V_{IH}$[3] | LVTTL input, $V_{DDD}$ ≥ 2.7 V | 2.0 | – | – | | – |
| SID244 | $V_{IL}$ | LVTTL input, $V_{DDD}$ ≥ 2.7 V | – | – | 0.8 | | – |
| SID59 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.6 | – | – | | $I_{OH}$ = 4 mA at 3 V $V_{DDD}$ |
| SID60 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.5 | – | – | | $I_{OH}$ = 1 mA at 1.8 V $V_{DDD}$ |
| SID61 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | | $I_{OL}$ = 4 mA at 1.8 V $V_{DDD}$ |
| SID62 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | | $I_{OL}$ = 10 mA at 3 V $V_{DDD}$ |
| SID62A | $V_{OL}$ | Output voltage low level | – | – | 0.4 | | $I_{OL}$ = 3 mA at 3 V $V_{DDD}$ |
| SID63 | $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | | – |
| SID65 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DDD}$ = 3.0 V |
| SID66 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID67[4] | $V_{HYSTTL}$ | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DDD}$ ≥ 2.7 V |
| SID68[4] | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DDD}$ | – | – | | $V_{DD}$ < 4.5 V |
| SID68A[4] | $V_{HYSCMOS5V5}$ | Input hysteresis CMOS | 200 | – | – | | $V_{DD}$ > 4.5 V |
| SID69[4] | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | – |
| SID69A[4] | $I_{TOT\_GPIO}$ | Maximum total source or sink chip current | – | – | 200 | mA | – |

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID70 | $T_{RISEF}$ | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID71 | $T_{FALLF}$ | Fall time in fast strong mode | 2 | – | 12 | | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID72 | $T_{RISES}$ | Rise time in slow strong mode | 10 | – | 60 | – | 3.3 V $V_{DDD}$, Cload = 25 pF |

**Notes**
3. $V_{IH}$ must not exceed $V_{DDD}$ + 0.2 V.
4. Guaranteed by characterization.

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID73 | $T_{FALLS}$ | Fall time in slow strong mode | 10 | – | 60 | – | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID74 | $F_{GPIOUT1}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Fast strong mode | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO $F_{OUT}$; 1.71 V≤ $V_{DDD}$≤ 3.3 V Fast strong mode | – | – | 16.7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Slow strong mode | – | – | 7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO $F_{OUT}$; 1.71 V ≤ $V_{DDD}$ ≤ 3.3 V Slow strong mode. | – | – | 3.5 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | $F_{GPIOIN}$ | GPIO input operating frequency; 1.71 V ≤ $V_{DDD}$ ≤ 5.5 V | – | – | 48 | | 90/10% $V_{IO}$ |

*XRES*

**Table 7. XRES DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID77 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID78 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | | |
| SID79 | $R_{PULLUP}$ | Pull-up resistor | – | 60 | – | kΩ | – |
| SID80 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID81[5] | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Typical hysteresis is 200 mV for $V_{DD}$ > 4.5 V |
| SID82 | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | |

**Table 8. XRES AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID83[5] | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | µs | – |
| BID194[5] | $T_{RESETWAKE}$ | Wake-up time from reset release | – | – | 2.7 | ms | – |

**Note**
5. Guaranteed by characterization.

**Table 9. CTBm Opamp Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID299 | T_OP_WAKE | From disable to enable, no external RC dominating | – | – | 25 | µs | – |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | |
| | COMP_MODE | Comparator mode; 50 mV drive, $T_{rise}$=$T_{fall}$ (approx.) | | | | | |
| SID300 | TPD1 | Response time; power=hi | – | 150 | – | ns | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID301 | TPD2 | Response time; power=med | – | 500 | – | | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID302 | TPD3 | Response time; power=lo | – | 2500 | – | | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID303 | VHYST_OP | Hysteresis | – | 10 | – | mV | – |
| SID304 | WUP_CTB | Wake-up time from Enabled to Usable | – | – | 25 | µs | – |
| | Deep Sleep Mode | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | |
| SID_DS_1 | $I_{DD\_HI\_M1}$ | Mode 1, High current | – | 1400 | – | µA | 25 °C |
| SID_DS_2 | $I_{DD\_MED\_M1}$ | Mode 1, Medium current | – | 700 | – | | 25 °C |
| SID_DS_3 | $I_{DD\_LOW\_M1}$ | Mode 1, Low current | – | 200 | – | | 25 °C |
| SID_DS_4 | $I_{DD\_HI\_M2}$ | Mode 2, High current | – | 120 | – | | 25 °C |
| SID_DS_5 | $I_{DD\_MED\_M2}$ | Mode 2, Medium current | – | 60 | – | | 25 °C |
| SID_DS_6 | $I_{DD\_LOW\_M2}$ | Mode 2, Low current | – | 15 | – | | 25 °C |

**Table 10. Comparator DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID84 | $V_{OFFSET1}$ | Input offset voltage, Factory trim | – | – | ±10 | mV | |
| SID85 | $V_{OFFSET2}$ | Input offset voltage, Custom trim | – | – | ±4 | | |
| SID86 | $V_{HYST}$ | Hysteresis when enabled | – | 10 | 35 | | |
| SID87 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$-0.1 | V | Modes 1 and 2 |
| SID247 | $V_{ICM2}$ | Input common mode voltage in low power mode | 0 | – | $V_{DDD}$ | | |
| SID247A | $V_{ICM3}$ | Input common mode voltage in ultra low power mode | 0 | – | $V_{DDD}$-1.15 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID88 | $C_{MRR}$ | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD}$ ≥ 2.7V |
| SID88A | $C_{MRR}$ | Common mode rejection ratio | 42 | – | – | | $V_{DDD}$ ≤ 2.7V |
| SID89 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | |
| SID248 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | | |
| SID259 | $I_{CMP3}$ | Block current in ultra low-power mode | – | – | 6 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID90 | $Z_{CMP}$ | DC Input impedance of comparator | 35 | – | – | MΩ | |

**Table 11. Comparator AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID91 | TRESP1 | Response time, normal mode, 50 mV overdrive | – | 38 | 110 | ns | |
| SID258 | TRESP2 | Response time, low power mode, 50 mV overdrive | – | 70 | 200 | | |
| SID92 | TRESP3 | Response time, ultra-low power mode, 200 mV overdrive | – | 2.3 | 15 | µs | $V_{DDD}$ ≥ 2.2 V at –40 °C |

**Table 12. Temperature Sensor Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID93 | TSENSACC | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

**Table 13. SAR Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| **SAR ADC DC Specifications** | | | | | | | |
| SID94 | A_RES | Resolution | – | – | 12 | bits | |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 4 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | | Yes. |
| SID98 | A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference. |

*CSD*

**Table 14. CSD and IDAC Specifications**

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD}$ > 2 V (with ripple), 25 °C $T_A$, Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD}$ > 1.75V (with ripple), 25 °C $T_A$, Parasitic Capacitance ($C_P$) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | µA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator. |
| SID.CSD#15 | $V_{REF}$ | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#15A | VREF_EXT | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | µA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | µA | |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA}$ –0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA}$ > 2 V. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID314A | IDAC1CRT2 | Output current of IDAC1(7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID314B | IDAC1CRT3 | Output current of IDAC1(7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID314D | IDAC1CRT22 | Output current of IDAC1(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID314E | IDAC1CRT32 | Output current of IDAC1(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID315D | IDAC2CRT22 | Output current of IDAC2(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID315E | IDAC2CRT32 | Output current of IDAC2(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | µA | LSB = 37.5-nA typ. |

**Table 14. CSD and IDAC Specifications** *(continued)*

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID315G | IDAC3CRT23 | Output current of IDAC in 8-bit mode in medium range | 69 | – | 82 | µA | LSB = 300-nA typ. |
| SID315H | IDAC3CRT33 | Output current of IDAC in 8-bit mode in high range | 540 | – | 660 | µA | LSB = 2.4-µA typ. |
| SID320 | IDACOFFSET | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode |
| SID321 | IDACGAIN | Full-scale error less offset | – | – | ±10 | % | |
| SID322 | IDACMISMATCH1 | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | IDACMISMATCH2 | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 5.6 | LSB | LSB = 300-nA typ. |
| SID322B | IDACMISMATCH3 | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 6.8 | LSB | LSB = 2.4-µA typ. |
| SID323 | IDACSET8 | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | IDACSET7 | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

**Table 15. 10-bit CapSense ADC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SIDA95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | Defined by AMUX Bus. |
| SIDA97 | A-MONO | Monotonicity | – | – | – | Yes | |
| SIDA98 | A_GAINERR | Gain error | – | – | ±2 | % | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA99 | A_OFFSET | Input offset voltage | – | – | 3 | mV | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA100 | A_ISAR | Current consumption | – | – | 0.25 | mA | |
| SIDA101 | A_VINS | Input voltage range - single ended | $V_{SSA}$ | – | $V_{DDA}$ | V | |
| SIDA103 | A_INRES | Input resistance | – | 2.2 | – | KΩ | |
| SIDA104 | A_INCAP | Input capacitance | – | 20 | – | pF | |
| SIDA106 | A_PSRR | Power supply rejection ratio | – | 60 | – | dB | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA107 | A_TACQ | Sample acquisition time | – | 1 | – | µs | |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 21.3 | µs | Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 85.3 | µs | Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time. |

**Table 21. UART DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbps | – | – | 55 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbps | – | – | 312 | µA | – |

**Table 22. UART AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 23. LCD Direct Drive DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID154 | $I_{LCDLOW}$ | Operating current in low power mode | – | 5 | – | µA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | $I_{LCDOP1}$ | LCD system operating current Vbias = 5 V | – | 2 | – | mA | 32 × 4 segments. 50 Hz. 25 °C |
| SID158 | $I_{LCDOP2}$ | LCD system operating current Vbias = 3.3 V | – | 2 | – | | 32 × 4 segments. 50 Hz. 25 °C |

**Table 24. LCD Direct Drive AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID159 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

**Note**
9. Guaranteed by characterization.

## Memory

**Table 25. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID173 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | – |

**Table 26. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$[10] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | $T_{ROWERASE}$[10] | Row erase time | – | – | 16 | | – |
| SID176 | $T_{ROWPROGRAM}$[10] | Row program time after erase | – | – | 4 | | – |
| SID178 | $T_{BULKERASE}$[10] | Bulk erase time (64 KB) | – | – | 35 | | – |
| SID180[11] | $T_{DEVPROG}$[10] | Total device program time | – | – | 7 | Seconds | – |
| SID181[11] | $F_{END}$ | Flash endurance | 100 K | – | – | Cycles | – |
| SID182[11] | $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles | 20 | – | – | Years | – |
| SID182A[11] | – | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles | 10 | – | – | | – |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |

## System Resources

*Power-on Reset (POR)*

**Table 27. Power On Reset (PRES)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185[11] | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186[11] | $V_{FALLIPOR}$ | Falling trip voltage | 0.70 | – | 1.4 | | – |

**Table 28. Brown-out Detect (BOD) for $V_{CCD}$**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190[11] | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192[11] | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

**Notes**
10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

*SWD Interface*

**Table 29. SWD Interface Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID213 | F_SWDCLK1 | 3.3 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | 1.71 V ≤ $V_{DD}$ ≤ 3.3 V | – | – | 7 | | SWDCLK ≤ 1/3 CPU clock frequency |
| SID215[12] | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25*T | – | – | ns | – |
| SID216[12] | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25*T | – | – | | – |
| SID217[12] | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5*T | | – |
| SID217A[12] | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | | – |

*Internal Main Oscillator*

**Table 30. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 250 | µA | – |
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 180 | µA | – |

**Table 31. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2 | % | |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 7 | µs | – |
| SID228 | $T_{JITRMSIMO2}$ | RMS jitter at 24 MHz | – | 145 | – | ps | – |

*Internal Low-Speed Oscillator*

**Table 32. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231[12] | $I_{ILO1}$ | ILO operating current | – | 0.3 | 1.05 | µA | – |

**Table 33. ILO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234[12] | $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | – |
| SID236[12] | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | $F_{ILOTRIM1}$ | ILO frequency range | 20 | 40 | 80 | kHz | – |

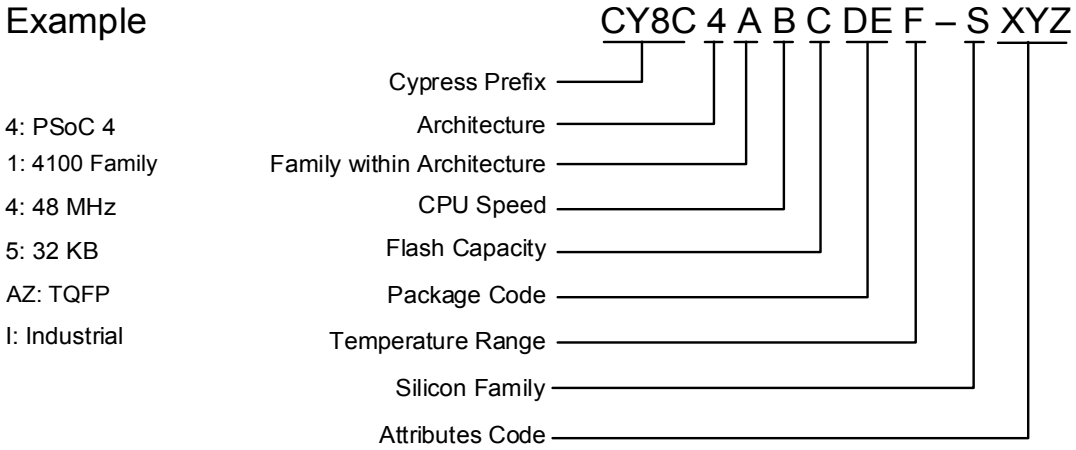
**Note**
12. Guaranteed by characterization.

The nomenclature used in the preceding table is based on the following part numbering convention:

| Field | Description | Values | Meaning |
|---|---|---|---|
| CY8C | Cypress Prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family | 1 | 4100 Family |
| B | CPU Speed | 2 | 24 MHz |
| | | 4 | 48 MHz |
| C | Flash Capacity | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package Code | AX | TQFP (0.8mm pitch) |
| | | AZ | TQFP (0.5mm pitch) |
| | | LQ | QFN |
| | | PV | SSOP |
| | | FN | CSP |
| F | Temperature Range | I | Industrial |
| S | Silicon Family | S | PSoC 4A-S1, PSoC 4A-S2 |
| | | M | PSoC 4A-M |
| | | L | PSoC 4A-L |
| | | BL | PSoC 4A-BLE |
| XYZ | Attributes Code | 000-999 | Code of feature set in the specific family |

The following is an example of a part number:

Example



## Packaging

The PSoC 4100S will be offered in 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball WLCSP packages. Package dimensions and Cypress drawing numbers are in the following table.

**Table 38. Package List**

| Spec ID# | Package | Description | Package Dwg |
|---|---|---|---|
| BID20 | 48-pin TQFP | 7 × 7 × 1.4-mm height with 0.5-mm pitch | 51-85135 |
| BID20A | 44-pin TQFP | 10 × 10 × 1.6-mm height with 0.8-mm pitch | 51-85064 |
| BID27 | 40-pin QFN | 6 × 6 × 0.6-mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32-pin QFN | 5 × 5 × 0.6-mm height with 0.5-mm pitch | 001-42168 |
| BID34D | 35-ball WLCSP | 2.6 × 2.1 × 0.48-mm height with 0.35-mm pitch | 002-09958 |

**Table 39. Package Thermal Characteristics**

| Parameter | Description | Package | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating Ambient temperature | | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ | 48-pin TQFP | – | 74.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 48-pin TQFP | – | 35.7 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 44-pin TQFP | – | 57.2 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 44-pin TQFP | – | 17.5 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 40-pin QFN | – | 17.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 40-pin QFN | – | 2.8 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 32-pin QFN | – | 19.9 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 32-pin QFN | – | 4.3 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 35-ball WLCSP | – | 43 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 35-ball WLCSP | – | 0.3 | – | °C/Watt |

**Table 40. Solder Reflow Peak Temperature**

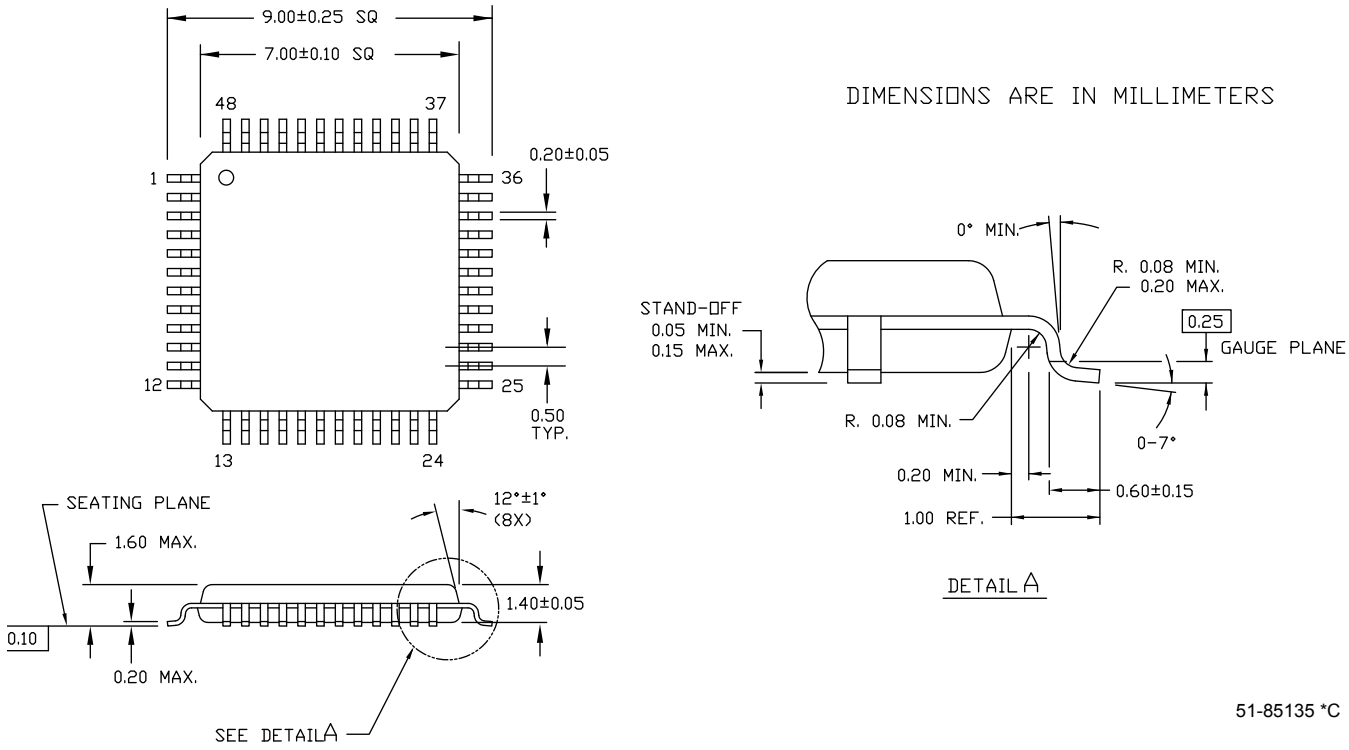
| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| All | 260 °C | 30 seconds |

**Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020**

| Package | MSL |
|---|---|
| All except WLCSP | MSL 3 |
| 35-ball WLCSP | MSL 1 |

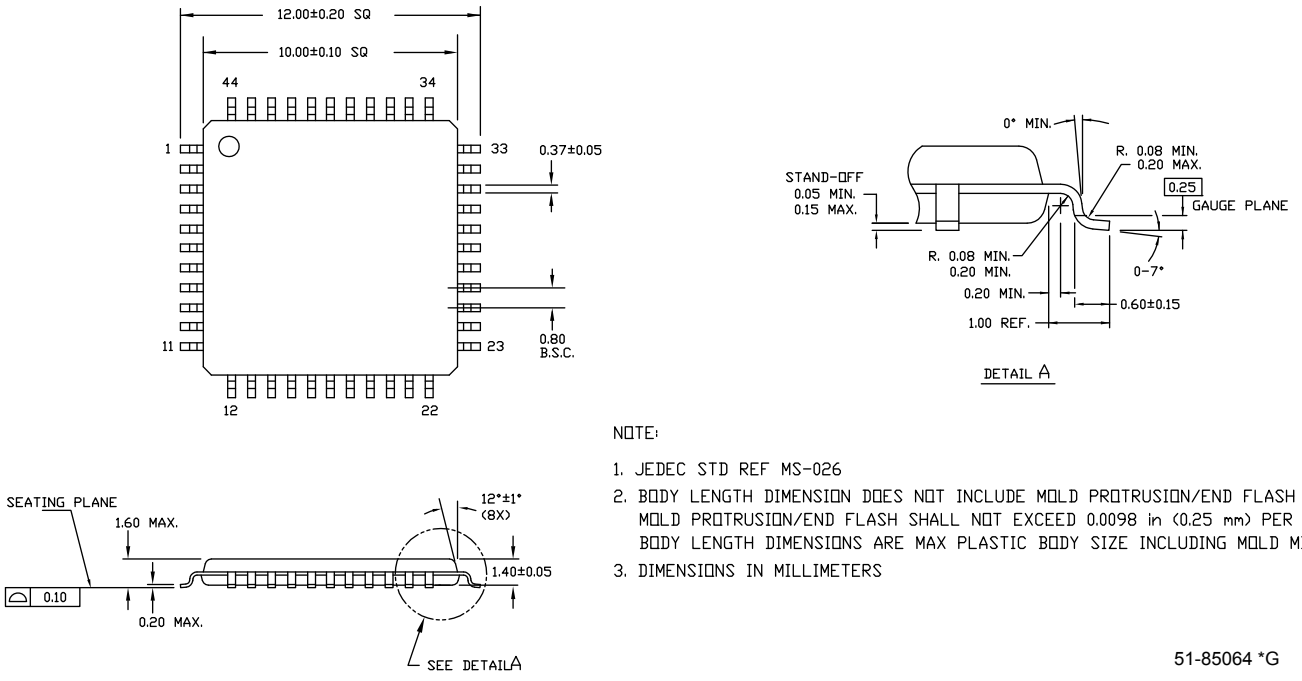
## Package Diagrams

**Figure 6. 48-pin TQFP Package Outline**




51-85135 *C

**Figure 7. 44-pin TQFP Package Outline**

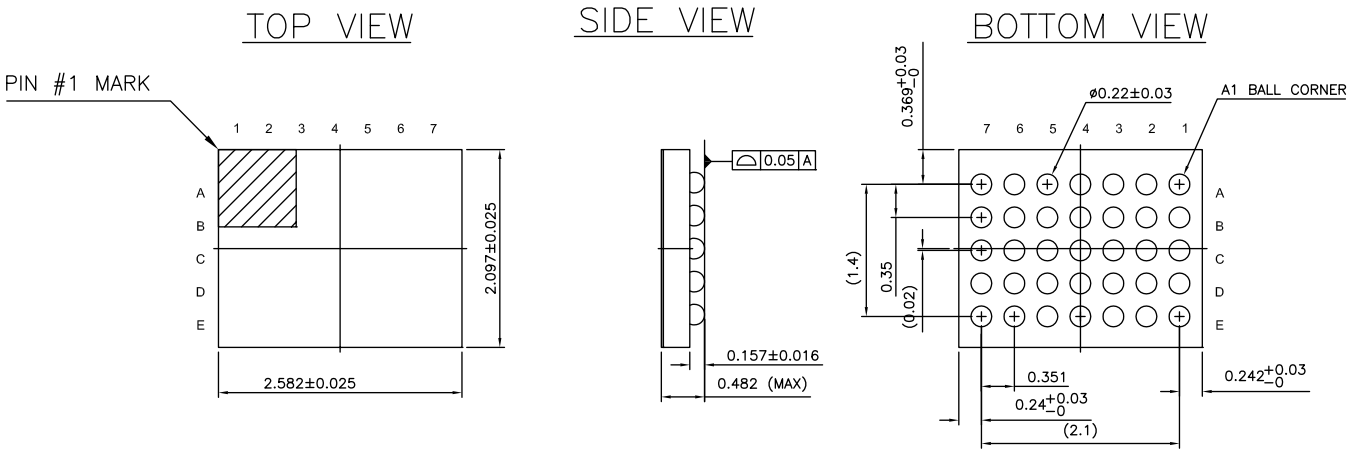



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

**Figure 10. 35-Ball WLCSP Package Outline**




ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-09958 *C

## Document Conventions

### Units of Measure

**Table 43. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Revision History

| Description Title: PSoC® 4: PSoC 4100S Family Datasheet Programmable System-on-Chip (PSoC)<br>Document Number: 002-00122 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 4883809 | WKA | 08/28/2015 | New datasheet |
| *A | 4992376 | WKA | 10/30/2015 | Updated Pinouts.<br>Added $V_{DDD}$ ≥ 2.2V at –40 °C under Conditions for specs SID247A, SID90, SID92.<br>Updated Table 15.<br>Updated Ordering Information. |
| *B | 5037826 | SLAN | 12/08/2015 | Changed datasheet status to Preliminary |
| *C | 5060691 | WKA | 12/22/2015 | Updated SCBs from 2 to 3.<br>Updated SRAM size to 8 KB.<br>Changed WLCSP package to 35-ball WLCSP.<br>Updated Pin List and Alternate Pin Functions.<br>Updated Ordering Information. |
| *D | 5139206 | WKA | 02/16/2016 | Added Errata.<br>Added 35 WLCSP package details.<br>Updated theta $J_A$ and $J_C$ values for all packages.<br>Updated copyright information at the end of the document. |
| *E | 5173961 | WKA | 03/15/2016 | Updated values for SID79, BID194. SID175, and SID176.<br>Updated CSD and IDAC Specifications.<br>Updated 10-bit CapSense ADC Specifications. |
| *F | 5330930 | WKA | 07/27/2016 | Updated CSD and IDAC Specifications.<br>Updated 10-bit CapSense ADC Specifications.<br>Removed errata. |
| *G | 5473409 | WKA | 10/13/2016 | Added 44 TQFP pin and package details. |
| *H | 5561833 | WKA | 01/09/2017 | Updated Figure 3.<br>Changed PRGIO references to Smart I/O.<br>Updated DC Specifications.<br>Updated Ordering Information. |