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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125lqi-s433t

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Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V $\pm 5\%$ (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

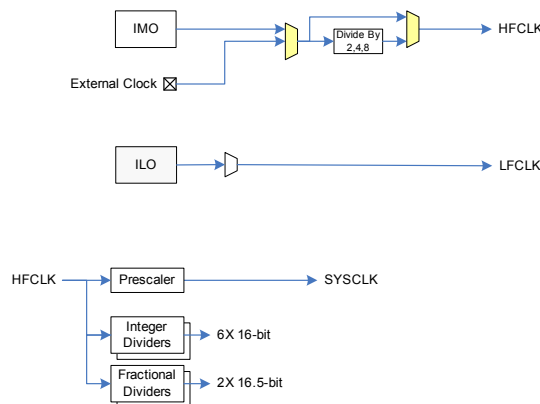
Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is $\pm 2\%$.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

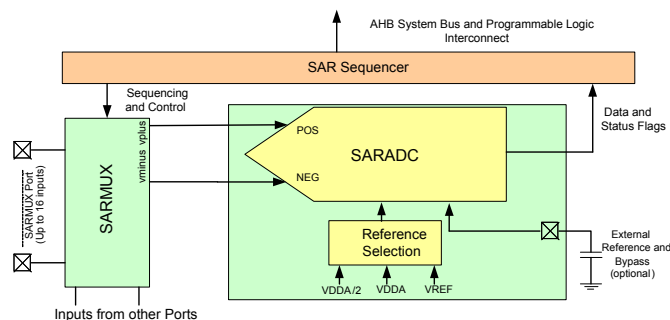
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 3. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

The PSoC 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage

Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

The PSoC 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4100S.

Serial Communication Block (SCB)

The PSoC 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also

Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1. Pin List

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

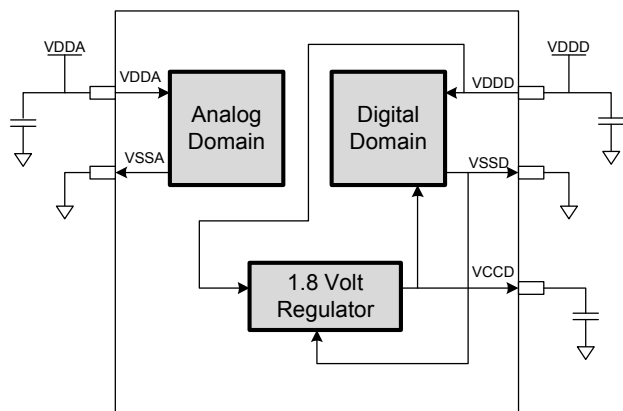
Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_miso:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 4. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V \pm 5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4100S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100S supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better) and must not be connected to anything else.

Mode 2: 1.8 V \pm 5% External Supply

In this mode, the PSoC 4100S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active

Power supply bypass connections example

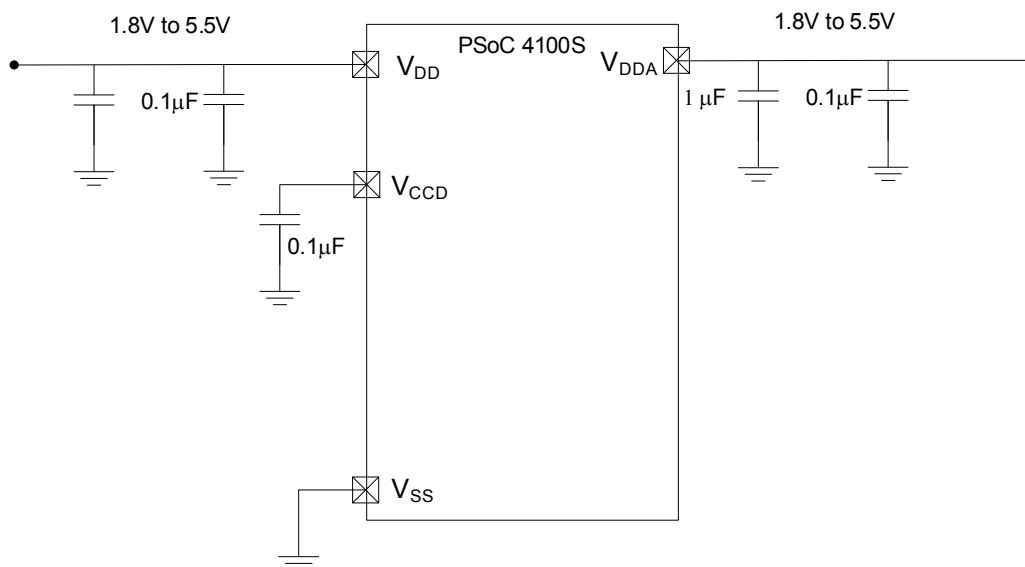


Table 6. GPIO AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Load = 25 pF
SID74	$F_{GPIOOUT1}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOOUT2}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOOUT3}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOOUT4}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5$ V	–	–	48		90/10% V_{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	k Ω	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81 ^[5]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for $V_{DD} > 4.5$ V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 ^[5]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	–
BID194 ^[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note

5. Guaranteed by characterization.

Analog Peripherals

Table 9. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current, External load					
SID269	I _{DD_HI}	power=hi	–	1100	1850	μA	–
SID270	I _{DD_MED}	power=med	–	550	950		–
SID271	I _{DD_LOW}	power=lo	–	150	350		–
	G _{BW}	Load = 20 pF, 0.1 mA V _{D_{DDA}} = 2.7 V					
SID272	G _{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
SID273	G _{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
SID274	G _{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
	I _{OUT_MAX}	V _{D_{DDA}} = 2.7 V, 500 mV from rail					
SID275	I _{OUT_MAX_HI}	power=hi	10	–	–	mA	Output is 0.5 V V _{D_{DDA}} -0.5 V
SID276	I _{OUT_MAX_MID}	power=mid	10	–	–		Output is 0.5 V V _{D_{DDA}} -0.5 V
SID277	I _{OUT_MAX_LO}	power=lo	–	5	–		Output is 0.5 V V _{D_{DDA}} -0.5 V
	I _{OUT}	V _{D_{DDA}} = 1.71 V, 500 mV from rail					
SID278	I _{OUT_MAX_HI}	power=hi	4	–	–	mA	Output is 0.5 V V _{D_{DDA}} -0.5 V
SID279	I _{OUT_MAX_MID}	power=mid	4	–	–		Output is 0.5 V V _{D_{DDA}} -0.5 V
SID280	I _{OUT_MAX_LO}	power=lo	–	2	–		Output is 0.5 V V _{D_{DDA}} -0.5 V
	I _{DD_Int}	Opamp block current Internal Load					
SID269_I	I _{DD_HI_Int}	power=hi	–	1500	1700	μA	–
SID270_I	I _{DD_MED_Int}	power=med	–	700	900		–
SID271_I	I _{DD_LOW_Int}	power=lo	–	–	–		–
	G _{BW}	V _{D_{DDA}} = 2.7 V	–	–	–		–
SID272_I	G _{BW_HI_Int}	power=hi	8	–	–	MHz	Output is 0.25 V to V _{D_{DDA}} -0.25 V

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V _{IN}	Charge-pump on, V _{DDA} = 2.7 V	−0.05	−	V _{DDA} -0.2	V	−
SID282	V _{CM}	Charge-pump on, V _{DDA} = 2.7 V	−0.05	−	V _{DDA} -0.2		−
	V _{OUT}	V _{DDA} = 2.7 V					
SID283	V _{OUT_1}	power=hi, Iload=10 mA	0.5	−	V _{DDA} -0.5	V	−
SID284	V _{OUT_2}	power=hi, Iload=1 mA	0.2	−	V _{DDA} -0.2		−
SID285	V _{OUT_3}	power=med, Iload=1 mA	0.2	−	V _{DDA} -0.2		−
SID286	V _{OUT_4}	power=lo, Iload=0.1 mA	0.2	−	V _{DDA} -0.2		−
SID288	V _{OS_TR}	Offset voltage, trimmed	−1.0	±0.5	1.0	mV	High mode, input 0 V to V _{DDA} -0.2 V
SID288A	V _{OS_TR}	Offset voltage, trimmed	−	±1	−		Medium mode, input 0 V to V _{DDA} -0.2 V
SID288B	V _{OS_TR}	Offset voltage, trimmed	−	±2	−		Low mode, input 0 V to V _{DDA} -0.2 V
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	−10	±3	10	µV/C	High mode
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	−	±10	−	µV/C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	−	±10	−		Low mode
SID291	CMRR	DC	70	80	−	dB	Input is 0 V to V _{DDA} -0.2 V, Output is 0.2 V to V _{DDA} -0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	−		V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} -0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	−	72	−	nV/rHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	−	28	−		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	−	15	−		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID297	C _{LOAD}	Stable up to max. load. Performance specs at 50 pF.	−	−	125	pF	−
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V _{DDA} = 2.7 V	6	−	−	V/µs	−

Table 14. CSD and IDAC Specifications (continued)

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 15. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V _{SSA}	–	V _{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = F _{clk} /(2 ^{N+2}). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksp/s including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = F _{clk} /(2 ^{N+2}). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time.

Table 15. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V _{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 16. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

²C

Table 17. Fixed I²C DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4		

Table 18. Fixed I²C AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Mbps	–

Notes

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

Note

8. Guaranteed by characterization.

Table 21. UART DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	I _{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	–

Table 22. UART AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	–

Table 23. LCD Direct Drive DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I _{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD _{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I _{LCDOP1}	LCD system operating current V _{bias} = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I _{LCDOP2}	LCD system operating current V _{bias} = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25 °C

Table 24. LCD Direct Drive AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	–

Note

9. Guaranteed by characterization.

Table 34. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

Table 35. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 ^[13]	ExtClkDuty	Duty cycle; measured at V _{DD/2}	45	–	55	%	–

Table 36. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[13]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

Note

13. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC 4100S family are listed in the following table.

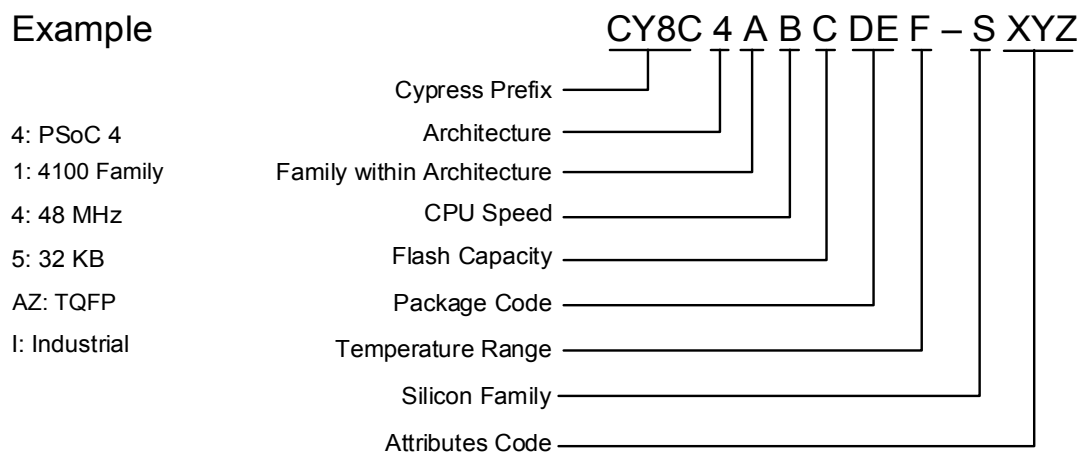
Category	MPN	Features														Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-WLCSP (0.35mm pitch)	32-QFN	40-QFN	48-TQFP	44-TQFP	
4124	CY8C4124FNI-S403	24	16	4	2	0	1	0		2	5	2	8	31	X					
	CY8C4124FNI-S413	24	16	4	2	1	1	0		2	5	2	16	31	X					
	CY8C4124LQI-S412	24	16	4	2	1	1	0		2	5	2	16	27		X				
	CY8C4124LQI-S413	24	16	4	2	1	1	0		2	5	2	16	34			X			
	CY8C4124AZI-S413	24	16	4	2	1	1	0		2	5	2	16	36				X		
	CY8C4124FNI-S433	24	16	4	2	1	1	1	806 ksp/s	2	5	2	16	31	X					
	CY8C4124LQI-S432	24	16	4	2	1	1	1	806 ksp/s	2	5	2	16	27		X				
	CY8C4124LQI-S433	24	16	4	2	1	1	1	806 ksp/s	2	5	2	16	34			X			
4125	CY8C4124AZI-S433	24	16	4	2	1	1	1	806 ksp/s	2	5	2	16	36				X		
	CY8C4125FNI-S423	24	32	4	2	0	1	1	806 ksp/s	2	5	2	16	31	X					
	CY8C4125LQI-S422	24	32	4	2	0	1	1	806 ksp/s	2	5	2	16	27		X				
	CY8C4125LQI-S423	24	32	4	2	0	1	1	806 ksp/s	2	5	2	16	34			X			
	CY8C4125AZI-S423	24	32	4	2	0	1	1	806 ksp/s	2	5	2	16	36				X		
	CY8C4125AXI-S423	24	32	4	2	0	1	1	806 ksp/s	2	5	2	16	36					X	
	CY8C4125FNI-S413	24	32	4	2	1	1	0		2	5	2	16	31	X					
	CY8C4125LQI-S412	24	32	4	2	1	1	0		2	5	2	16	27		X				
	CY8C4125LQI-S413	24	32	4	2	1	1	0		2	5	2	16	34			X			
	CY8C4125AZI-S413	24	32	4	2	1	1	0		2	5	2	16	36				X		
	CY8C4125FNI-S433	24	32	4	2	1	1	1	806 ksp/s	2	5	2	16	31	X					
	CY8C4125LQI-S432	24	32	4	2	1	1	1	806 ksp/s	2	5	2	16	27		X				
	CY8C4125LQI-S433	24	32	4	2	1	1	1	806 ksp/s	2	5	2	16	34			X			
	CY8C4125AZI-S433	24	32	4	2	1	1	1	806 ksp/s	2	5	2	16	36				X		
4126	CY8C4125AXI-S433	24	32	4	2	1	1	1	806 ksp/s	2	5	2	16	36					X	
	CY8C4126AZI-S423	24	64	8	2	0	1	1	806 ksp/s	2	5	3	16	36				X		
	CY8C4126AXI-S423	24	64	8	2	0	1	1	806 ksp/s	2	5	3	16	36					X	
	CY8C4126AZI-S433	24	64	8	2	1	1	1	806 ksp/s	2	5	3	16	36				X		
4145	CY8C4126AXI-S433	24	64	8	2	1	1	1	806 ksp/s	2	5	3	16	36					X	
	CY8C4145AZI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36				X		
	CY8C4145AXI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36					X	
4146	CY8C4145AXI-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36					X	
	CY8C4146FNI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	31	X					
	CY8C4146LQI-S422	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27		X				
	CY8C4146LQI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	34			X			
	CY8C4146AZI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36				X		
	CY8C4146AXI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36					X	
	CY8C4146FNI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X					
	CY8C4146LQI-S432	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27		X				
	CY8C4146LQI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	34			X			
	CY8C4146AZI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36				X		
CY8C4146AXI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36					X		

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

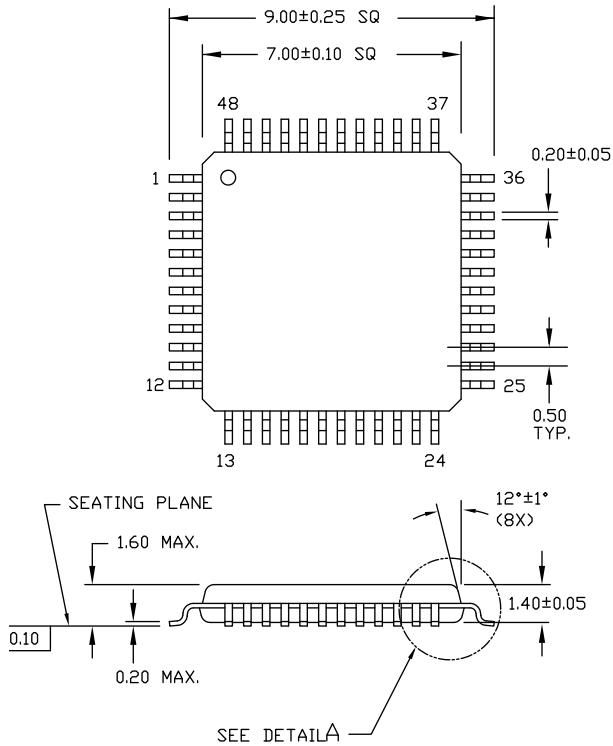
The following is an example of a part number:

Example

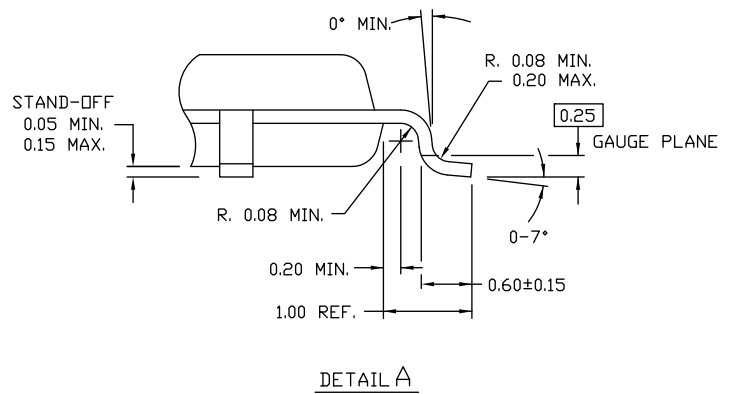


Package Diagrams

Figure 6. 48-pin TQFP Package Outline

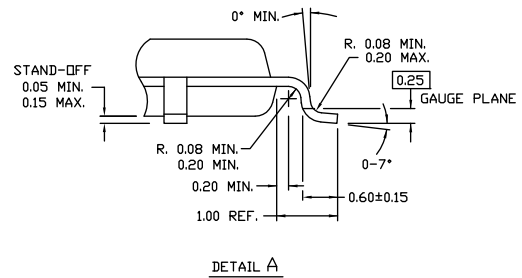
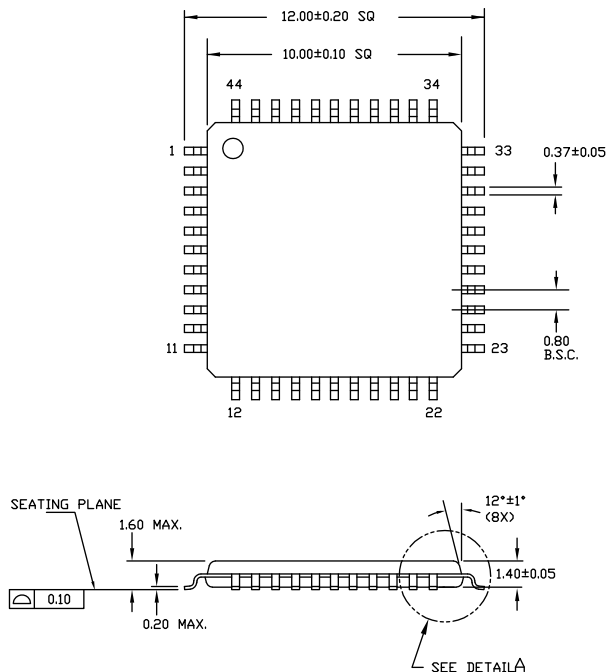


DIMENSIONS ARE IN MILLIMETERS



51-85135 *C

Figure 7. 44-pin TQFP Package Outline

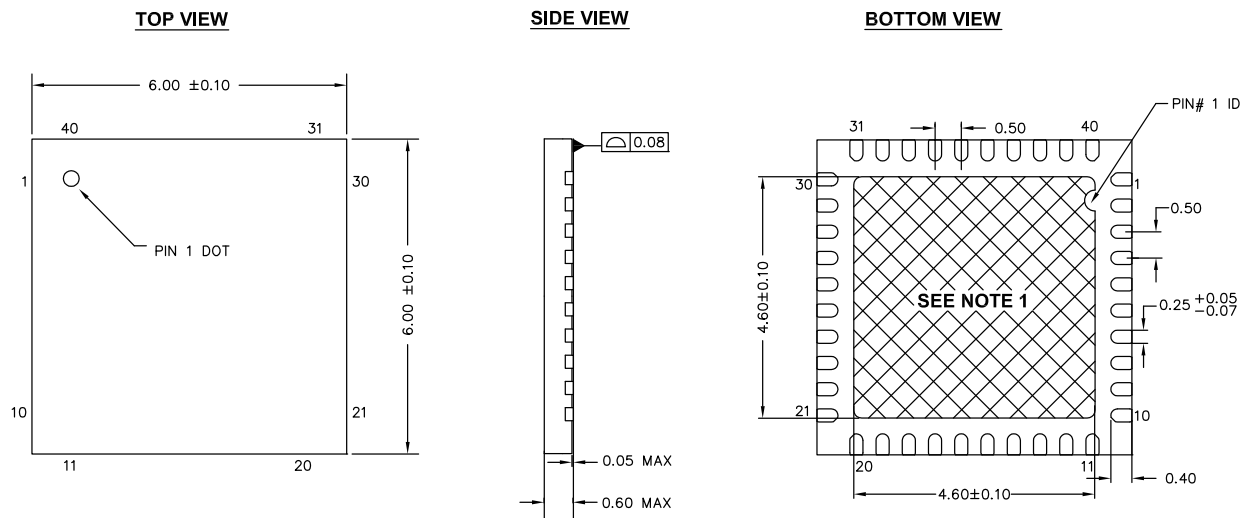


NOTE:


1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Figure 8. 40-pin QFN Package Outline

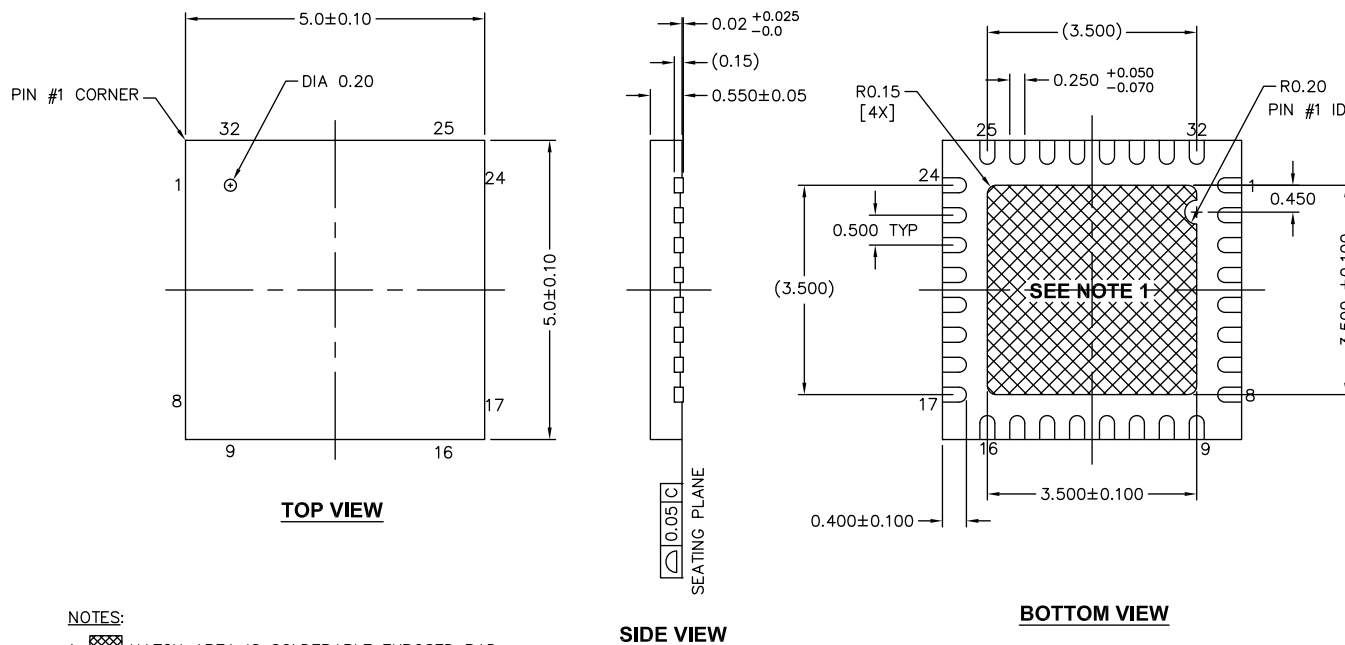


NOTES:


1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 9. 32-pin QFN Package Outline

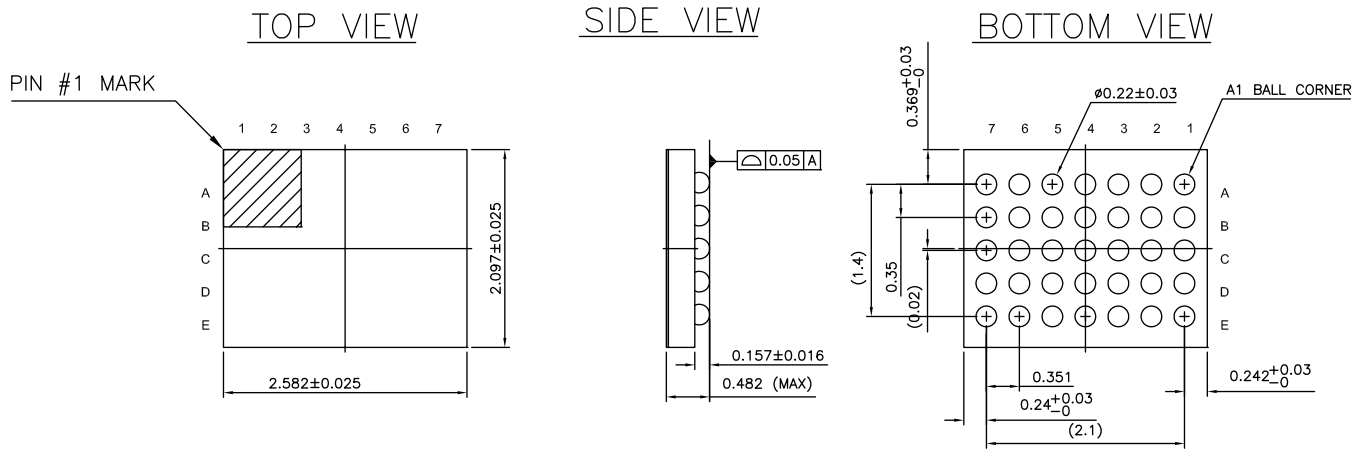


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 10. 35-Ball WLCSP Package Outline



ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-09958 *C

Revision History

Description Title: PSoC® 4: PSoC 4100S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00122				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4883809	WKA	08/28/2015	New datasheet
*A	4992376	WKA	10/30/2015	Updated Pinouts . Added $V_{DDD} \geq 2.2V$ at $-40^{\circ}C$ under Conditions for specs SID247A, SID90, SID92. Updated Table 15 . Updated Ordering Information .
*B	5037826	SLAN	12/08/2015	Changed datasheet status to Preliminary
*C	5060691	WKA	12/22/2015	Updated SCBs from 2 to 3. Updated SRAM size to 8 KB. Changed WLCSP package to 35-ball WLCSP. Updated Pin List and Alternate Pin Functions. Updated Ordering Information .
*D	5139206	WKA	02/16/2016	Added Errata. Added 35 WLCSP package details. Updated θ_{JA} and J_C values for all packages. Updated copyright information at the end of the document.
*E	5173961	WKA	03/15/2016	Updated values for SID79, BID194, SID175, and SID176. Updated CSD and IDAC Specifications . Updated 10-bit CapSense ADC Specifications .
*F	5330930	WKA	07/27/2016	Updated CSD and IDAC Specifications . Updated 10-bit CapSense ADC Specifications . Removed errata.
*G	5473409	WKA	10/13/2016	Added 44 TQFP pin and package details.
*H	5561833	WKA	01/09/2017	Updated Figure 3 . Changed PRGIO references to Smart I/O. Updated DC Specifications . Updated Ordering Information .