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What is "Embedded - Microcontrollers"?

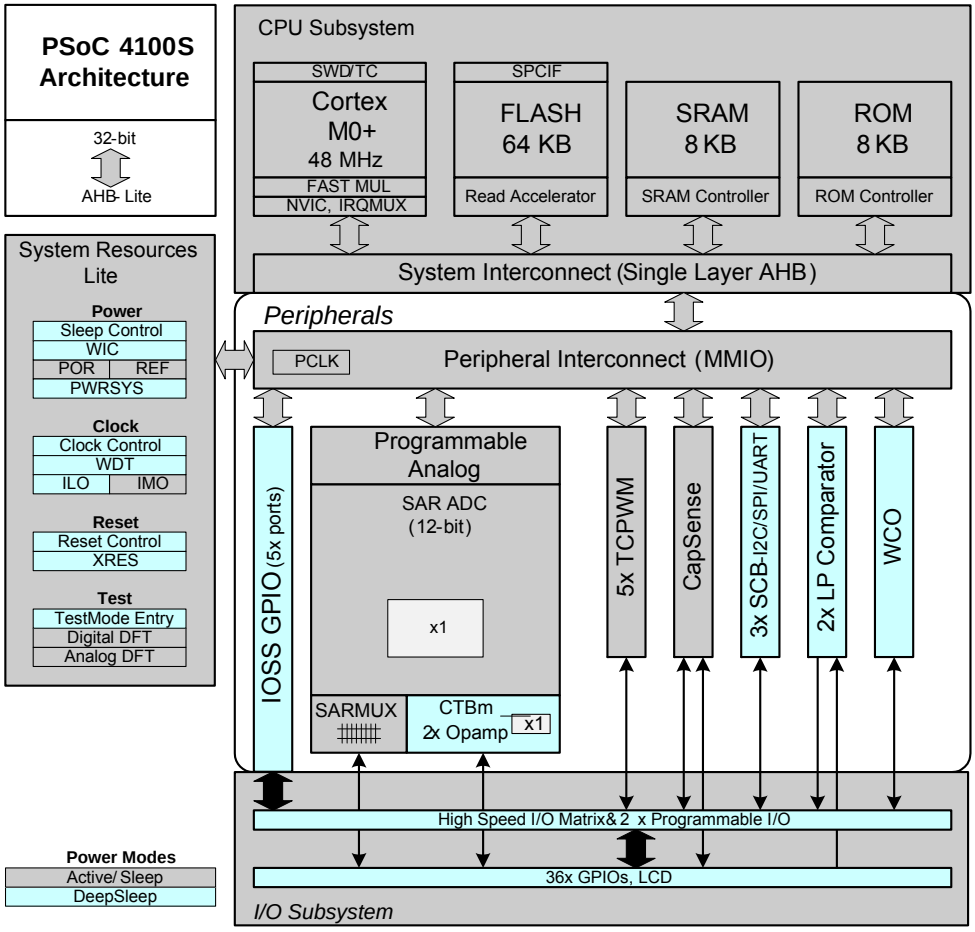
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4126azi-s423t

Contents

Figure 1. Block Diagram



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

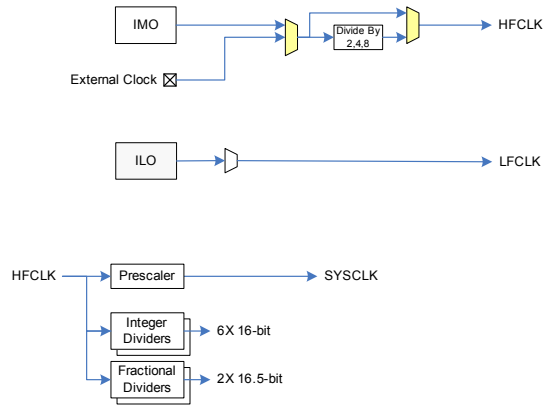
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Table 1. Pin List *(continued)*

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
19	P3.6	17	P3.6	16	P3.6				
20	P3.7	18	P3.7	17	P3.7				
21	VDDD	19	VDDD						
22	P4.0	20	P4.0	18	P4.0	13	P4.0	B1	P4.0
23	P4.1	21	P4.1	19	P4.1	14	P4.1	B2	P4.1
24	P4.2	22	P4.2	20	P4.2	15	P4.2	A2	P4.2
25	P4.3	23	P4.3	21	P4.3	16	P4.3	A1	P4.3

Notes: Pins 11, 15, 26, and 27 are No Connects (NC) on the 48-pin TQFP.

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: Power supply to all sections of the chip

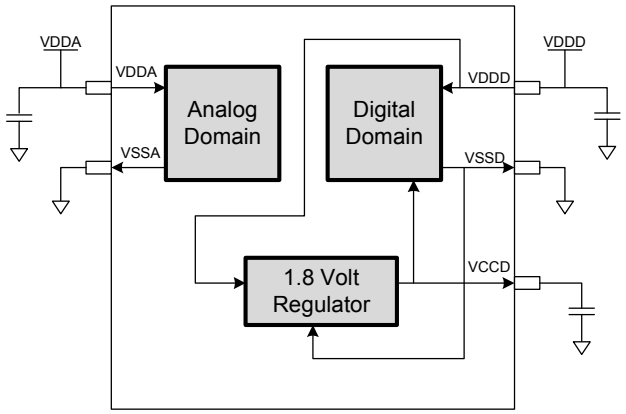
VSS: Ground for all sections of the chip

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 4. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4100S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100S supplies the internal logic and its output is connected to the V_{CCD} pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

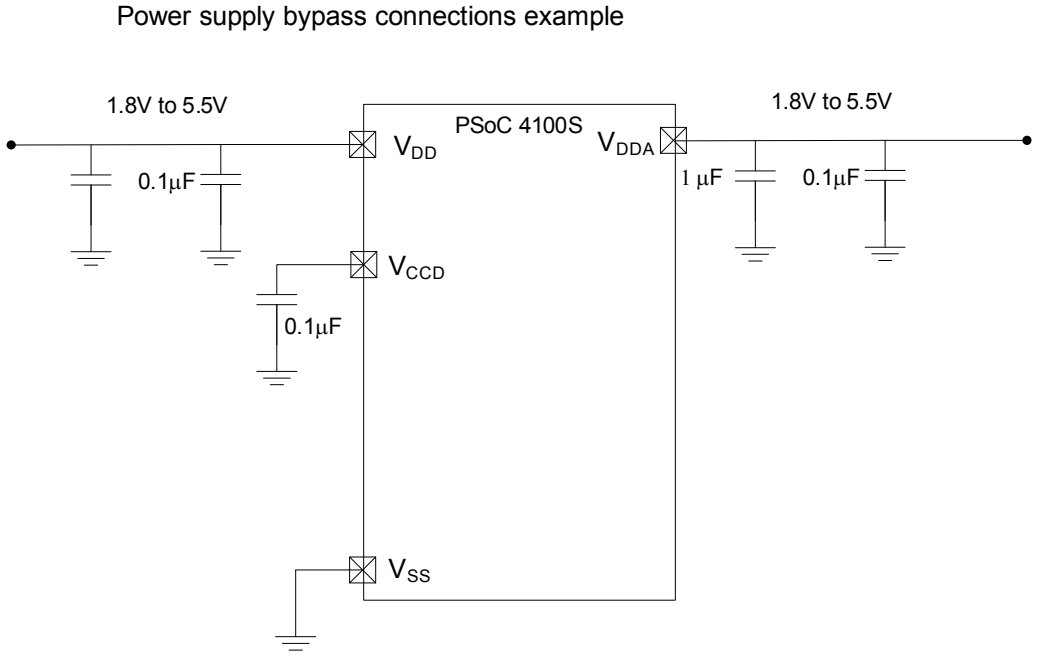
Mode 2: 1.8 V ±5% External Supply

In this mode, the PSoC 4100S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active



Development Support

The PSoC 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DDD} = V_{DDA})	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Max is at 85 °C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	4.75		Max is at 85 °C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	6.85		Max is at 85 °C and 5.5 V

Note
1. Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I^2C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID25	IDD20	I^2C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHZ. Max is at 85 °C and 5.5 V.
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I^2C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID28A	IDD23A	I^2C wakeup, WDT, and Comparators on	–	1	1.2	mA	12 MHZ. Max is at 85 °C and 5.5 V.
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 3.6 V and 85 °C.
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 5.5 V and 85 °C.
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	65	µA	Max is at 1.89 V and 85 °C.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[3]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[3]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

Note
2. Guaranteed by characterization.

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[3]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		CMOS Input
SID241	V_{IH}[3]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[3]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDD} ≥ 2.7 V
SID68[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF

Notes
3. V_{IH} must not exceed V_{DDD} + 0.2 V.
4. Guaranteed by characterization.

Analog Peripherals

Table 9. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current, External load					
SID269	I_{DD_HI}	power=hi	–	1100	1850	µA	–
SID270	I_{DD_MED}	power=med	–	550	950		–
SID271	I_{DD_LOW}	power=lo	–	150	350		–
	G_{BW}	Load = 20 pF, 0.1 mA V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V_{DDA}-0.2 V
SID273	G_{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V_{DDA}-0.2 V
SID274	G_{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V_{DDA}-0.2 V
	I_{OUT_MAX}	V_{DDA} = 2.7 V, 500 mV from rail					
SID275	$I_{OUT\_MAX\_HI}$	power=hi	10	–	–	mA	Output is 0.5 V V_{DDA}-0.5 V
SID276	$I_{OUT\_MAX\_MID}$	power=mid	10	–	–		Output is 0.5 V V_{DDA}-0.5 V
SID277	$I_{OUT\_MAX\_LO}$	power=lo	–	5	–		Output is 0.5 V V_{DDA}-0.5 V
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT\_MAX\_HI}$	power=hi	4	–	–	mA	Output is 0.5 V V_{DDA}-0.5 V
SID279	$I_{OUT\_MAX\_MID}$	power=mid	4	–	–		Output is 0.5 V V_{DDA}-0.5 V
SID280	$I_{OUT\_MAX\_LO}$	power=lo	–	2	–		Output is 0.5 V V_{DDA}-0.5 V
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD\_HI\_Int}$	power=hi	–	1500	1700	µA	–
SID270_I	$I_{DD\_MED\_Int}$	power=med	–	700	900		–
SID271_I	$I_{DD\_LOW\_Int}$	power=lo	–	–	–		–
	G_{BW}	V_{DDA} = 2.7 V	–	–	–		–
SID272_I	$G_{BW\_HI\_Int}$	power=hi	8	–	–	MHz	Output is 0.25 V to V_{DDA}-0.25 V

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	power=hi, Iload=10 mA	0.5	–	V_{DDA} -0.5	V	–
SID284	V_{OUT_2}	power=hi, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID285	V_{OUT_3}	power=med, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID286	V_{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V_{DDA} -0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA}-0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA}-0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA}-0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA}-0.2 V, Output is 0.2 V to V_{DDA}-0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA}-0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–

Table 9. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_9	$G_{BW\_LOW\_M!}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V_{DDA}-0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_19	$I_{OUT\_HI\_M!}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

Note
6. Guaranteed by characterization.

CSD

Table 14. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25 °C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5-nA typ.

Table 14. CSD and IDAC Specifications *(continued)*

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 15. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.

Table 21. UART DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 22. UART AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 23. LCD Direct Drive DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25 °C

Table 24. LCD Direct Drive AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note
9. Guaranteed by characterization.

Memory

Table 25. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[10]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (64 KB)	–	–	35		–
SID180[11]	$T_{DEVPROG}$[10]	Total device program time	–	–	7	Seconds	–
SID181[11]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[11]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A[11]	–	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[11]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 28. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[11]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes
10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

SWD Interface

Table 29. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T		–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Internal Main Oscillator

Table 30. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 31. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 32. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[12]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 33. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[12]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note
12. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC 4100S family are listed in the following table.

Category	MPN	Features													Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-WLCSP (0.35mm pitch)	32-QFN	40-QFN	48-TQFP	44-TQFP
4124	CY8C4124FNI-S403	24	16	4	2	0	1	0		2	5	2	8	31	X				
	CY8C4124FNI-S413	24	16	4	2	1	1	0		2	5	2	16	31	X				
	CY8C4124LQI-S412	24	16	4	2	1	1	0		2	5	2	16	27		X			
	CY8C4124LQI-S413	24	16	4	2	1	1	0		2	5	2	16	34			X		
	CY8C4124AZI-S413	24	16	4	2	1	1	0		2	5	2	16	36				X	
	CY8C4124FNI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4124LQI-S432	24	16	4	2	1	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4124LQI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4124AZI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	36				X	
4125	CY8C4125FNI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4125LQI-S422	24	32	4	2	0	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4125LQI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4125AZI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36				X	
	CY8C4125AXI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36					X
	CY8C4125FNI-S413	24	32	4	2	1	1	0		2	5	2	16	31	X				
	CY8C4125LQI-S412	24	32	4	2	1	1	0		2	5	2	16	27		X			
	CY8C4125LQI-S413	24	32	4	2	1	1	0		2	5	2	16	34			X		
	CY8C4125AZI-S413	24	32	4	2	1	1	0		2	5	2	16	36				X	
	CY8C4125FNI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	31	X				
	CY8C4125LQI-S432	24	32	4	2	1	1	1	806 ksps	2	5	2	16	27		X			
	CY8C4125LQI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	34			X		
	CY8C4125AZI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36				X	
	CY8C4125AXI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36					X
4126	CY8C4126AZI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36				X	
	CY8C4126AXI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36					X
	CY8C4126AZI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36				X	
	CY8C4126AXI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36					X
4145	CY8C4145AZI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36				X	
	CY8C4145AXI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36					X
	CY8C4145AXI-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36					X
4146	CY8C4146FNI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	31	X				
	CY8C4146LQI-S422	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27		X			
	CY8C4146LQI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	34			X		
	CY8C4146AZI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36				X	
	CY8C4146AXI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36					X
	CY8C4146FNI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X				
	CY8C4146LQI-S432	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27		X			
	CY8C4146LQI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	34			X		
	CY8C4146AZI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36				X	
	CY8C4146AXI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36					X

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PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support