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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4126azi-s433 |

## Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

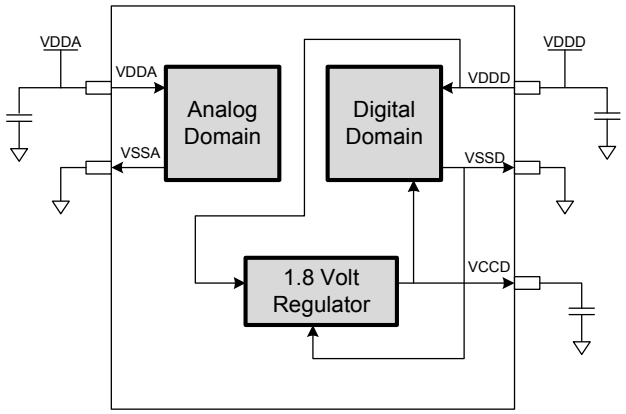
**Table 1. Pin List**

| 48-TQFP | | 44-TQFP | | 40-QFN | | 32-QFN | | 35-CSP | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 28 | P0.0 | 24 | P0.0 | 22 | P0.0 | 17 | P0.0 | C3 | P0.0 |
| 29 | P0.1 | 25 | P0.1 | 23 | P0.1 | 18 | P0.1 | A5 | P0.1 |
| 30 | P0.2 | 26 | P0.2 | 24 | P0.2 | 19 | P0.2 | A4 | P0.2 |
| 31 | P0.3 | 27 | P0.3 | 25 | P0.3 | 20 | P0.3 | A3 | P0.3 |
| 32 | P0.4 | 28 | P0.4 | 26 | P0.4 | 21 | P0.4 | B3 | P0.4 |
| 33 | P0.5 | 29 | P0.5 | 27 | P0.5 | 22 | P0.5 | A6 | P0.5 |
| 34 | P0.6 | 30 | P0.6 | 28 | P0.6 | 23 | P0.6 | B4 | P0.6 |
| 35 | P0.7 | 31 | P0.7 | 29 | P0.7 | | | B5 | P0.7 |
| 36 | XRES | 32 | XRES | 30 | XRES | 24 | XRES | B6 | XRES |
| 37 | VCCD | 33 | VCCD | 31 | VCCD | 25 | VCCD | A7 | VCCD |
| 38 | VSSD | | | DN | VSSD | 26 | VSSD | B7 | VSS |
| 39 | VDDD | 34 | VDDD | 32 | VDDD | | | C7 | VDD |
| 40 | VDDA | 35 | VDDA | 33 | VDDA | 27 | VDD | C7 | VDD |
| 41 | VSSA | 36 | VSSA | 34 | VSSA | 28 | VSSA | B7 | VSS |
| 42 | P1.0 | 37 | P1.0 | 35 | P1.0 | 29 | P1.0 | C4 | P1.0 |
| 43 | P1.1 | 38 | P1.1 | 36 | P1.1 | 30 | P1.1 | C5 | P1.1 |
| 44 | P1.2 | 39 | P1.2 | 37 | P1.2 | 31 | P1.2 | C6 | P1.2 |
| 45 | P1.3 | 40 | P1.3 | 38 | P1.3 | 32 | P1.3 | D7 | P1.3 |
| 46 | P1.4 | 41 | P1.4 | 39 | P1.4 | | | D4 | P1.4 |
| 47 | P1.5 | 42 | P1.5 | | | | | D5 | P1.5 |
| 48 | P1.6 | 43 | P1.6 | | | | | D6 | P1.6 |
| 1 | P1.7/VREF | 44 | P1.7/VREF | 40 | P1.7/VREF | 1 | P1.7/VREF | E7 | P1.7/VREF |
| | | 1 | VSSD | | | | | | |
| 2 | P2.0 | 2 | P2.0 | 1 | P2.0 | 2 | P2.0 | | |
| 3 | P2.1 | 3 | P2.1 | 2 | P2.1 | 3 | P2.1 | | |
| 4 | P2.2 | 4 | P2.2 | 3 | P2.2 | 4 | P2.2 | D3 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | 4 | P2.3 | 5 | P2.3 | E4 | P2.3 |
| 6 | P2.4 | 6 | P2.4 | 5 | P2.4 | | | E5 | P2.4 |
| 7 | P2.5 | 7 | P2.5 | 6 | P2.5 | 6 | P2.5 | E6 | P2.5 |
| 8 | P2.6 | 8 | P2.6 | 7 | P2.6 | 7 | P2.6 | E3 | P2.6 |
| 9 | P2.7 | 9 | P2.7 | 8 | P2.7 | 8 | P2.7 | E2 | P2.7 |
| 10 | VSSD | 10 | VSSD | 9 | VSSD | | | | |
| 12 | P3.0 | 11 | P3.0 | 10 | P3.0 | 9 | P3.0 | E1 | P3.0 |
| 13 | P3.1 | 12 | P3.1 | 11 | P3.1 | 10 | P3.1 | D2 | P3.1 |
| 14 | P3.2 | 13 | P3.2 | 12 | P3.2 | 11 | P3.2 | D1 | P3.2 |
| 16 | P3.3 | 14 | P3.3 | 13 | P3.3 | 12 | P3.3 | C1 | P3.3 |
| 17 | P3.4 | 15 | P3.4 | 14 | P3.4 | | | C2 | P3.4 |
| 18 | P3.5 | 16 | P3.5 | 15 | P3.5 | | | | |

## Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the $V_{DD}$ input.

**Figure 4. Power Supply Connections**




There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

### Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4100S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100S supplies the internal logic and its output is connected to the $V_{CCD}$ pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

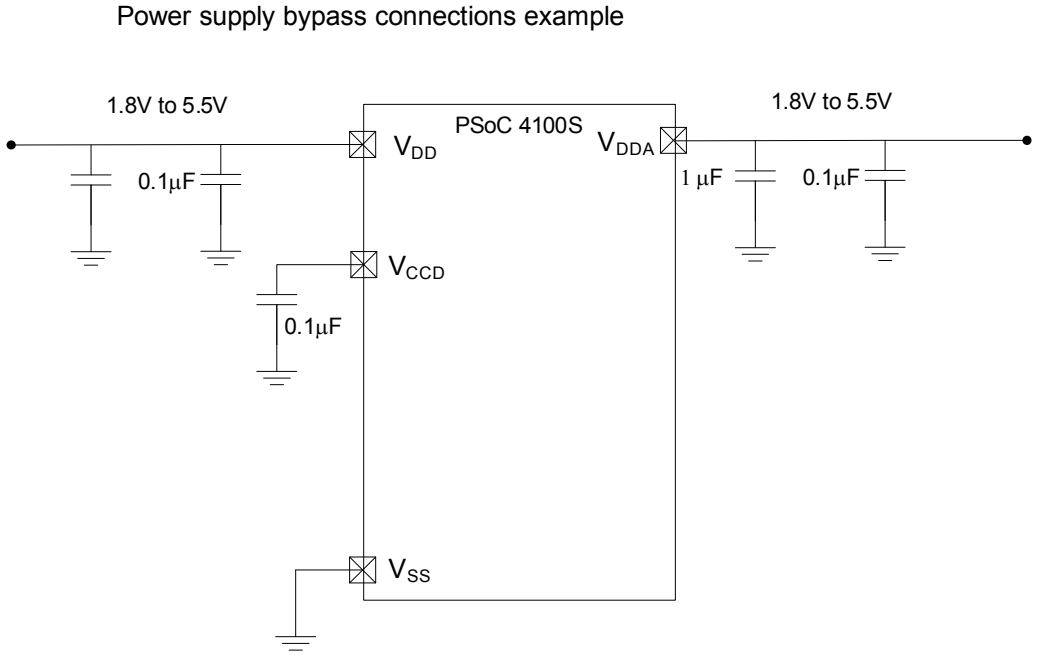
### Mode 2: 1.8 V ±5% External Supply

In this mode, the PSoC 4100S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

**Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active**



# Electrical Specifications

## Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings**[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID1 | $V_{DDD\_ABS}$ | Digital supply relative to $V_{SS}$ | –0.5 | – | 6 | V | – |
| SID2 | $V_{CCD\_ABS}$ | Direct digital core voltage input relative to $V_{SS}$ | –0.5 | – | 1.95 | | – |
| SID3 | $V_{GPIO\_ABS}$ | GPIO voltage | –0.5 | – | $V_{DD}$+0.5 | | – |
| SID4 | $I_{GPIO\_ABS}$ | Maximum current per GPIO | –25 | – | 25 | mA | – |
| SID5 | $I_{GPIO\_injection}$ | GPIO injection current, Max for $V_{IH}$ > $V_{DDD}$, and Min for $V_{IL}$ < $V_{SS}$ | –0.5 | – | 0.5 | | Current injected per pin |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | – |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | | – |
| BID46 | LU | Pin current for latch-up | –140 | – | 140 | mA | – |

## Device Level Specifications

All specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 3. DC Specifications**

Typical values measured at $V_{DD}$ = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID53 | $V_{DD}$ | Power supply input voltage | 1.8 | – | 5.5 | V | Internally regulated supply |
| SID255 | $V_{DD}$ | Power supply input voltage ($V_{CCD}$ = $V_{DDD}$ = $V_{DDA}$) | 1.71 | – | 1.89 | | Internally unregulated supply |
| SID54 | $V_{CCD}$ | Output voltage (for core logic) | – | 1.8 | – | | – |
| SID55 | $C_{EFC}$ | External regulator voltage bypass | – | 0.1 | – | µF | X5R ceramic or better |
| SID56 | $C_{EXC}$ | Power supply bypass capacitor | – | 1 | – | | X5R ceramic or better |
| **Active Mode, $V_{DD}$ = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C.** | | | | | | | |
| SID10 | $I_{DD5}$ | Execute from flash; CPU at 6 MHz | – | 1.8 | 2.7 | mA | Max is at 85 °C and 5.5 V |
| SID16 | $I_{DD8}$ | Execute from flash; CPU at 24 MHz | – | 3.0 | 4.75 | | Max is at 85 °C and 5.5 V |
| SID19 | $I_{DD11}$ | Execute from flash; CPU at 48 MHz | – | 5.4 | 6.85 | | Max is at 85 °C and 5.5 V |

**Note**
1. Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 3. DC Specifications** *(continued)*

Typical values measured at $V_{DD}$ = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| **Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)** | | | | | | | |
| SID22 | IDD17 | $I^2C$ wakeup WDT, and Comparators on | – | 1.7 | 2.2 | mA | 6 MHZ. Max is at 85 °C and 5.5 V. |
| SID25 | IDD20 | $I^2C$ wakeup, WDT, and Comparators on. | – | 2.2 | 2.5 | | 12 MHZ. Max is at 85 °C and 5.5 V. |
| **Sleep Mode, $V_{DDD}$ = 1.71 V to 1.89 V (Regulator bypassed)** | | | | | | | |
| SID28 | IDD23 | $I^2C$ wakeup, WDT, and Comparators on | – | 0.7 | 0.9 | mA | 6 MHZ. Max is at 85 °C and 5.5 V. |
| SID28A | IDD23A | $I^2C$ wakeup, WDT, and Comparators on | – | 1 | 1.2 | mA | 12 MHZ. Max is at 85 °C and 5.5 V. |
| **Deep Sleep Mode, $V_{DD}$ = 1.8 V to 3.6 V (Regulator on)** | | | | | | | |
| SID31 | $I_{DD26}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 60 | µA | Max is at 3.6 V and 85 °C. |
| **Deep Sleep Mode, $V_{DD}$ = 3.6 V to 5.5 V (Regulator on)** | | | | | | | |
| SID34 | $I_{DD29}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 60 | µA | Max is at 5.5 V and 85 °C. |
| **Deep Sleep Mode, $V_{DD}$ = $V_{CCD}$ = 1.71 V to 1.89 V (Regulator bypassed)** | | | | | | | |
| SID37 | $I_{DD32}$ | $I^2C$ wakeup and WDT on | – | 2.5 | 65 | µA | Max is at 1.89 V and 85 °C. |
| **XRES Current** | | | | | | | |
| SID307 | $I_{DD\_XR}$ | Supply current while XRES asserted | – | 2 | 5 | mA | – |

**Table 4. AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID48 | $F_{CPU}$ | CPU frequency | DC | – | 48 | MHz | $1.71 \le V_{DD} \le 5.5$ |
| SID49[3] | $T_{SLEEP}$ | Wakeup from Sleep mode | – | 0 | – | µs | |
| SID50[3] | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | | |

**Note**
2. Guaranteed by characterization.

*GPIO*

**Table 5. GPIO DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID57 | $V_{IH}$[3] | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID58 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | | CMOS Input |
| SID241 | $V_{IH}$[3] | LVTTL input, $V_{DDD}$ < 2.7 V | 0.7 × $V_{DDD}$ | – | – | | – |
| SID242 | $V_{IL}$ | LVTTL input, $V_{DDD}$ < 2.7 V | – | – | 0.3 × $V_{DDD}$ | | – |
| SID243 | $V_{IH}$[3] | LVTTL input, $V_{DDD}$ ≥ 2.7 V | 2.0 | – | – | | – |
| SID244 | $V_{IL}$ | LVTTL input, $V_{DDD}$ ≥ 2.7 V | – | – | 0.8 | | – |
| SID59 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.6 | – | – | | $I_{OH}$ = 4 mA at 3 V $V_{DDD}$ |
| SID60 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.5 | – | – | | $I_{OH}$ = 1 mA at 1.8 V $V_{DDD}$ |
| SID61 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | | $I_{OL}$ = 4 mA at 1.8 V $V_{DDD}$ |
| SID62 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | | $I_{OL}$ = 10 mA at 3 V $V_{DDD}$ |
| SID62A | $V_{OL}$ | Output voltage low level | – | – | 0.4 | | $I_{OL}$ = 3 mA at 3 V $V_{DDD}$ |
| SID63 | $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | | – |
| SID65 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DDD}$ = 3.0 V |
| SID66 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID67[4] | $V_{HYSTTL}$ | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DDD}$ ≥ 2.7 V |
| SID68[4] | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DDD}$ | – | – | | $V_{DD}$ < 4.5 V |
| SID68A[4] | $V_{HYSCMOS5V5}$ | Input hysteresis CMOS | 200 | – | – | | $V_{DD}$ > 4.5 V |
| SID69[4] | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | – |
| SID69A[4] | $I_{TOT\_GPIO}$ | Maximum total source or sink chip current | – | – | 200 | mA | – |

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID70 | $T_{RISEF}$ | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID71 | $T_{FALLF}$ | Fall time in fast strong mode | 2 | – | 12 | | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID72 | $T_{RISES}$ | Rise time in slow strong mode | 10 | – | 60 | – | 3.3 V $V_{DDD}$, Cload = 25 pF |

**Notes**
3. $V_{IH}$ must not exceed $V_{DDD}$ + 0.2 V.
4. Guaranteed by characterization.

## Analog Peripherals

**Table 9. CTBm Opamp Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| | $I_{DD}$ | Opamp block current, External load | | | | | |
| SID269 | $I_{DD\_HI}$ | power=hi | – | 1100 | 1850 | µA | – |
| SID270 | $I_{DD\_MED}$ | power=med | – | 550 | 950 | | – |
| SID271 | $I_{DD\_LOW}$ | power=lo | – | 150 | 350 | | – |
| | $G_{BW}$ | Load = 20 pF, 0.1 mA $V_{DDA}$ = 2.7 V | | | | | |
| SID272 | $G_{BW\_HI}$ | power=hi | 6 | – | – | MHz | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| SID273 | $G_{BW\_MED}$ | power=med | 3 | – | – | | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| SID274 | $G_{BW\_LO}$ | power=lo | – | 1 | – | | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| | $I_{OUT\_MAX}$ | $V_{DDA}$ = 2.7 V, 500 mV from rail | | | | | |
| SID275 | $I_{OUT\_MAX\_HI}$ | power=hi | 10 | – | – | mA | Output is 0.5 V $V_{DDA}$-0.5 V |
| SID276 | $I_{OUT\_MAX\_MID}$ | power=mid | 10 | – | – | | Output is 0.5 V $V_{DDA}$-0.5 V |
| SID277 | $I_{OUT\_MAX\_LO}$ | power=lo | – | 5 | – | | Output is 0.5 V $V_{DDA}$-0.5 V |
| | $I_{OUT}$ | $V_{DDA}$ = 1.71 V, 500 mV from rail | | | | | |
| SID278 | $I_{OUT\_MAX\_HI}$ | power=hi | 4 | – | – | mA | Output is 0.5 V $V_{DDA}$-0.5 V |
| SID279 | $I_{OUT\_MAX\_MID}$ | power=mid | 4 | – | – | | Output is 0.5 V $V_{DDA}$-0.5 V |
| SID280 | $I_{OUT\_MAX\_LO}$ | power=lo | – | 2 | – | | Output is 0.5 V $V_{DDA}$-0.5 V |
| | $I_{DD\_Int}$ | Opamp block current Internal Load | | | | | |
| SID269_I | $I_{DD\_HI\_Int}$ | power=hi | – | 1500 | 1700 | µA | – |
| SID270_I | $I_{DD\_MED\_Int}$ | power=med | – | 700 | 900 | | – |
| SID271_I | $I_{DD\_LOW\_Int}$ | power=lo | – | – | – | | – |
| | $G_{BW}$ | $V_{DDA}$ = 2.7 V | – | – | – | | – |
| SID272_I | $G_{BW\_HI\_Int}$ | power=hi | 8 | – | – | MHz | Output is 0.25 V to $V_{DDA}$-0.25 V |

**Table 9. CTBm Opamp Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID299 | T_OP_WAKE | From disable to enable, no external RC dominating | – | – | 25 | µs | – |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | |
| | COMP_MODE | Comparator mode; 50 mV drive, $T_{rise}$=$T_{fall}$ (approx.) | | | | | |
| SID300 | TPD1 | Response time; power=hi | – | 150 | – | ns | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID301 | TPD2 | Response time; power=med | – | 500 | – | | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID302 | TPD3 | Response time; power=lo | – | 2500 | – | | Input is 0.2 V to $V_{DDA}$-0.2 V |
| SID303 | VHYST_OP | Hysteresis | – | 10 | – | mV | – |
| SID304 | WUP_CTB | Wake-up time from Enabled to Usable | – | – | 25 | µs | – |
| | Deep Sleep Mode | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | |
| SID_DS_1 | $I_{DD\_HI\_M1}$ | Mode 1, High current | – | 1400 | – | µA | 25 °C |
| SID_DS_2 | $I_{DD\_MED\_M1}$ | Mode 1, Medium current | – | 700 | – | | 25 °C |
| SID_DS_3 | $I_{DD\_LOW\_M1}$ | Mode 1, Low current | – | 200 | – | | 25 °C |
| SID_DS_4 | $I_{DD\_HI\_M2}$ | Mode 2, High current | – | 120 | – | | 25 °C |
| SID_DS_5 | $I_{DD\_MED\_M2}$ | Mode 2, Medium current | – | 60 | – | | 25 °C |
| SID_DS_6 | $I_{DD\_LOW\_M2}$ | Mode 2, Low current | – | 15 | – | | 25 °C |

**Table 10. Comparator DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID84 | $V_{OFFSET1}$ | Input offset voltage, Factory trim | – | – | ±10 | mV | |
| SID85 | $V_{OFFSET2}$ | Input offset voltage, Custom trim | – | – | ±4 | | |
| SID86 | $V_{HYST}$ | Hysteresis when enabled | – | 10 | 35 | | |
| SID87 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$-0.1 | V | Modes 1 and 2 |
| SID247 | $V_{ICM2}$ | Input common mode voltage in low power mode | 0 | – | $V_{DDD}$ | | |
| SID247A | $V_{ICM3}$ | Input common mode voltage in ultra low power mode | 0 | – | $V_{DDD}$-1.15 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID88 | $C_{MRR}$ | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD}$ ≥ 2.7V |
| SID88A | $C_{MRR}$ | Common mode rejection ratio | 42 | – | – | | $V_{DDD}$ ≤ 2.7V |
| SID89 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | |
| SID248 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | | |
| SID259 | $I_{CMP3}$ | Block current in ultra low-power mode | – | – | 6 | | $V_{DDD}$ ≥ 2.2 V at –40 °C |
| SID90 | $Z_{CMP}$ | DC Input impedance of comparator | 35 | – | – | MΩ | |

**Table 11. Comparator AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID91 | TRESP1 | Response time, normal mode, 50 mV overdrive | – | 38 | 110 | ns | |
| SID258 | TRESP2 | Response time, low power mode, 50 mV overdrive | – | 70 | 200 | | |
| SID92 | TRESP3 | Response time, ultra-low power mode, 200 mV overdrive | – | 2.3 | 15 | µs | $V_{DDD}$ ≥ 2.2 V at –40 °C |

**Table 12. Temperature Sensor Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID93 | TSENSACC | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

**Table 13. SAR Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| **SAR ADC DC Specifications** | | | | | | | |
| SID94 | A_RES | Resolution | – | – | 12 | bits | |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 4 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | | Yes. |
| SID98 | A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference. |

**Table 13. SAR Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR | Current consumption | – | – | 1 | mA | |
| SID101 | A_VINS | Input voltage range - single ended | $V_{SS}$ | – | $V_{DDA}$ | V | |
| SID102 | A_VIND | Input voltage range - differential[ | $V_{SS}$ | – | $V_{DDA}$ | V | |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | KΩ | |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | |
| SID260 | VREFSAR | Trimmed internal reference to SAR | – | – | TBD | V | |
| **SAR ADC AC Specifications** | | | | | | | |
| SID106 | A_PSRR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| SID108 | A_SAMP | Sample rate | – | – | 1 | Msps | |
| SID109 | A_SNR | Signal-to-noise and distortion ratio (SINAD) | 65 | – | – | dB | $F_{IN}$ = 10 kHz |
| SID110 | A_BW | Input bandwidth without aliasing | – | – | A_samp/2 | kHz | |
| SID111 | A_INL | Integral non linearity. $V_{DD}$ = 1.71 to 5.5, 1 Msps | –1.7 | – | 2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID111A | A_INL | Integral non linearity. $V_{DDD}$ = 1.71 to 3.6, 1 Msps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1.71 to $V_{DD}$ |
| SID111B | A_INL | Integral non linearity. $V_{DD}$ = 1.71 to 5.5, 500 ksps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID112 | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 5.5, 1 Msps | –1 | _ | 2.2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID112A | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 3.6, 1 Msps | –1 | _ | 2 | LSB | $V_{REF}$ = 1.71 to $V_{DD}$ |
| SID112B | A_DNL | Differential non linearity. $V_{DD}$ = 1.71 to 5.5, 500 ksps | –1 | _ | 2.2 | LSB | $V_{REF}$ = 1 to $V_{DD}$ |
| SID113 | A_THD | Total harmonic distortion | – | – | –65 | dB | Fin = 10 kHz |
| SID261 | FSARINTREF | SAR operating speed without external ref. bypass | _ | _ | 100 | ksps | 12-bit resolution |

*CSD*

**Table 14. CSD and IDAC Specifications**

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD}$ > 2 V (with ripple), 25 °C $T_A$, Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD}$ > 1.75V (with ripple), 25 °C $T_A$, Parasitic Capacitance ($C_P$) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | µA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator. |
| SID.CSD#15 | $V_{REF}$ | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#15A | VREF_EXT | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | µA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | µA | |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA}$ –0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA}$ > 2 V. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID314A | IDAC1CRT2 | Output current of IDAC1(7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID314B | IDAC1CRT3 | Output current of IDAC1(7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID314D | IDAC1CRT22 | Output current of IDAC1(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID314E | IDAC1CRT32 | Output current of IDAC1(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID315D | IDAC2CRT22 | Output current of IDAC2(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID315E | IDAC2CRT32 | Output current of IDAC2(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | µA | LSB = 37.5-nA typ. |

**Table 21. UART DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbps | – | – | 55 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbps | – | – | 312 | µA | – |

**Table 22. UART AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 23. LCD Direct Drive DC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID154 | $I_{LCDLOW}$ | Operating current in low power mode | – | 5 | – | µA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | $I_{LCDOP1}$ | LCD system operating current Vbias = 5 V | – | 2 | – | mA | 32 × 4 segments. 50 Hz. 25 °C |
| SID158 | $I_{LCDOP2}$ | LCD system operating current Vbias = 3.3 V | – | 2 | – | | 32 × 4 segments. 50 Hz. 25 °C |

**Table 24. LCD Direct Drive AC Specifications**[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID159 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

**Note**
9. Guaranteed by characterization.

## Memory

**Table 25. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID173 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | – |

**Table 26. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$[10] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | $T_{ROWERASE}$[10] | Row erase time | – | – | 16 | | – |
| SID176 | $T_{ROWPROGRAM}$[10] | Row program time after erase | – | – | 4 | | – |
| SID178 | $T_{BULKERASE}$[10] | Bulk erase time (64 KB) | – | – | 35 | | – |
| SID180[11] | $T_{DEVPROG}$[10] | Total device program time | – | – | 7 | Seconds | – |
| SID181[11] | $F_{END}$ | Flash endurance | 100 K | – | – | Cycles | – |
| SID182[11] | $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles | 20 | – | – | Years | – |
| SID182A[11] | – | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles | 10 | – | – | | – |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |

## System Resources

*Power-on Reset (POR)*

**Table 27. Power On Reset (PRES)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185[11] | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186[11] | $V_{FALLIPOR}$ | Falling trip voltage | 0.70 | – | 1.4 | | – |

**Table 28. Brown-out Detect (BOD) for $V_{CCD}$**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190[11] | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192[11] | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

**Notes**
10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

**Table 34. Watch Crystal Oscillator (WCO) Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID398 | FWCO | Crystal Frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | µW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal Load Capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal Shunt Capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating Current (high power mode) | – | – | 8 | uA | |
| SID406 | IWCO2 | Operating Current (low power mode) | – | – | 1 | uA | |

**Table 35. External Clock Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID305[13] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306[13] | ExtClkDuty | Duty cycle; measured at $V_{DD/2}$ | 45 | – | 55 | % | – |

**Table 36. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID262[13] | $T_{CLKSWITCH}$ | System clock source switching time | 3 | – | 4 | Periods | – |

**Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

**Note**
13. Guaranteed by characterization.

## Ordering Information

The marketing part numbers for the PSoC 4100S family are listed in the following table.

| Category | MPN | Features | | | | | | | | | | | | | Package | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | Opamp (CTBm) | CSD | 10-bit CSD ADC | 12-bit SAR ADC | ADC Sample Rate | LP Comparators | TCPWM Blocks | SCB Blocks | Smart I/Os | GPIO | 35-WLCSP (0.35mm pitch) | 32-QFN | 40-QFN | 48-TQFP | 44-TQFP |
| 4124 | CY8C4124FNI-S403 | 24 | 16 | 4 | 2 | 0 | 1 | 0 | | 2 | 5 | 2 | 8 | 31 | X | | | | |
| | CY8C4124FNI-S413 | 24 | 16 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 31 | X | | | | |
| | CY8C4124LQI-S412 | 24 | 16 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 27 | | X | | | |
| | CY8C4124LQI-S413 | 24 | 16 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 34 | | | X | | |
| | CY8C4124AZI-S413 | 24 | 16 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 36 | | | | X | |
| | CY8C4124FNI-S433 | 24 | 16 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 31 | X | | | | |
| | CY8C4124LQI-S432 | 24 | 16 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 27 | | X | | | |
| | CY8C4124LQI-S433 | 24 | 16 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 34 | | | X | | |
| | CY8C4124AZI-S433 | 24 | 16 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 36 | | | | X | |
| 4125 | CY8C4125FNI-S423 | 24 | 32 | 4 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 31 | X | | | | |
| | CY8C4125LQI-S422 | 24 | 32 | 4 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 27 | | X | | | |
| | CY8C4125LQI-S423 | 24 | 32 | 4 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 34 | | | X | | |
| | CY8C4125AZI-S423 | 24 | 32 | 4 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 36 | | | | X | |
| | CY8C4125AXI-S423 | 24 | 32 | 4 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 36 | | | | | X |
| | CY8C4125FNI-S413 | 24 | 32 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 31 | X | | | | |
| | CY8C4125LQI-S412 | 24 | 32 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 27 | | X | | | |
| | CY8C4125LQI-S413 | 24 | 32 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 34 | | | X | | |
| | CY8C4125AZI-S413 | 24 | 32 | 4 | 2 | 1 | 1 | 0 | | 2 | 5 | 2 | 16 | 36 | | | | X | |
| | CY8C4125FNI-S433 | 24 | 32 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 31 | X | | | | |
| | CY8C4125LQI-S432 | 24 | 32 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 27 | | X | | | |
| | CY8C4125LQI-S433 | 24 | 32 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 34 | | | X | | |
| | CY8C4125AZI-S433 | 24 | 32 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 36 | | | | X | |
| | CY8C4125AXI-S433 | 24 | 32 | 4 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 2 | 16 | 36 | | | | | X |
| 4126 | CY8C4126AZI-S423 | 24 | 64 | 8 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 3 | 16 | 36 | | | | X | |
| | CY8C4126AXI-S423 | 24 | 64 | 8 | 2 | 0 | 1 | 1 | 806 ksps | 2 | 5 | 3 | 16 | 36 | | | | | X |
| | CY8C4126AZI-S433 | 24 | 64 | 8 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 3 | 16 | 36 | | | | X | |
| | CY8C4126AXI-S433 | 24 | 64 | 8 | 2 | 1 | 1 | 1 | 806 ksps | 2 | 5 | 3 | 16 | 36 | | | | | X |
| 4145 | CY8C4145AZI-S423 | 48 | 32 | 4 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 2 | 16 | 36 | | | | X | |
| | CY8C4145AXI-S423 | 48 | 32 | 4 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 2 | 16 | 36 | | | | | X |
| | CY8C4145AXI-S433 | 48 | 32 | 4 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 2 | 16 | 36 | | | | | X |
| 4146 | CY8C4146FNI-S423 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 31 | X | | | | |
| | CY8C4146LQI-S422 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 27 | | X | | | |
| | CY8C4146LQI-S423 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 34 | | | X | | |
| | CY8C4146AZI-S423 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 36 | | | | X | |
| | CY8C4146AXI-S423 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 36 | | | | | X |
| | CY8C4146FNI-S433 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 31 | X | | | | |
| | CY8C4146LQI-S432 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 27 | | X | | | |
| | CY8C4146LQI-S433 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 34 | | | X | | |
| | CY8C4146AZI-S433 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 36 | | | | X | |
| | CY8C4146AXI-S433 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 5 | 3 | 16 | 36 | | | | | X |

## Packaging

The PSoC 4100S will be offered in 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball WLCSP packages. Package dimensions and Cypress drawing numbers are in the following table.

**Table 38. Package List**

| Spec ID# | Package | Description | Package Dwg |
|---|---|---|---|
| BID20 | 48-pin TQFP | 7 × 7 × 1.4-mm height with 0.5-mm pitch | 51-85135 |
| BID20A | 44-pin TQFP | 10 × 10 × 1.6-mm height with 0.8-mm pitch | 51-85064 |
| BID27 | 40-pin QFN | 6 × 6 × 0.6-mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32-pin QFN | 5 × 5 × 0.6-mm height with 0.5-mm pitch | 001-42168 |
| BID34D | 35-ball WLCSP | 2.6 × 2.1 × 0.48-mm height with 0.35-mm pitch | 002-09958 |

**Table 39. Package Thermal Characteristics**

| Parameter | Description | Package | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating Ambient temperature | | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ | 48-pin TQFP | – | 74.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 48-pin TQFP | – | 35.7 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 44-pin TQFP | – | 57.2 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 44-pin TQFP | – | 17.5 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 40-pin QFN | – | 17.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 40-pin QFN | – | 2.8 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 32-pin QFN | – | 19.9 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 32-pin QFN | – | 4.3 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 35-ball WLCSP | – | 43 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 35-ball WLCSP | – | 0.3 | – | °C/Watt |

**Table 40. Solder Reflow Peak Temperature**

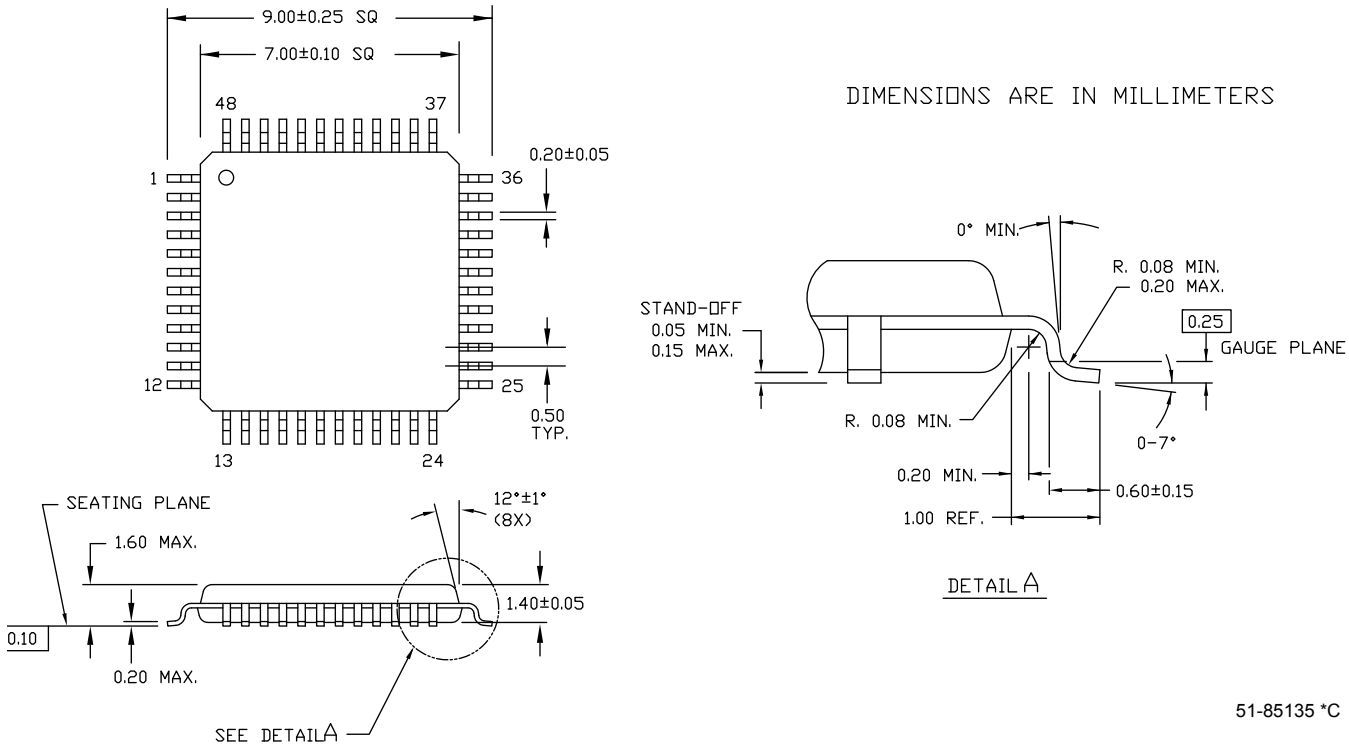
| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| All | 260 °C | 30 seconds |

**Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020**

| Package | MSL |
|---|---|
| All except WLCSP | MSL 3 |
| 35-ball WLCSP | MSL 1 |

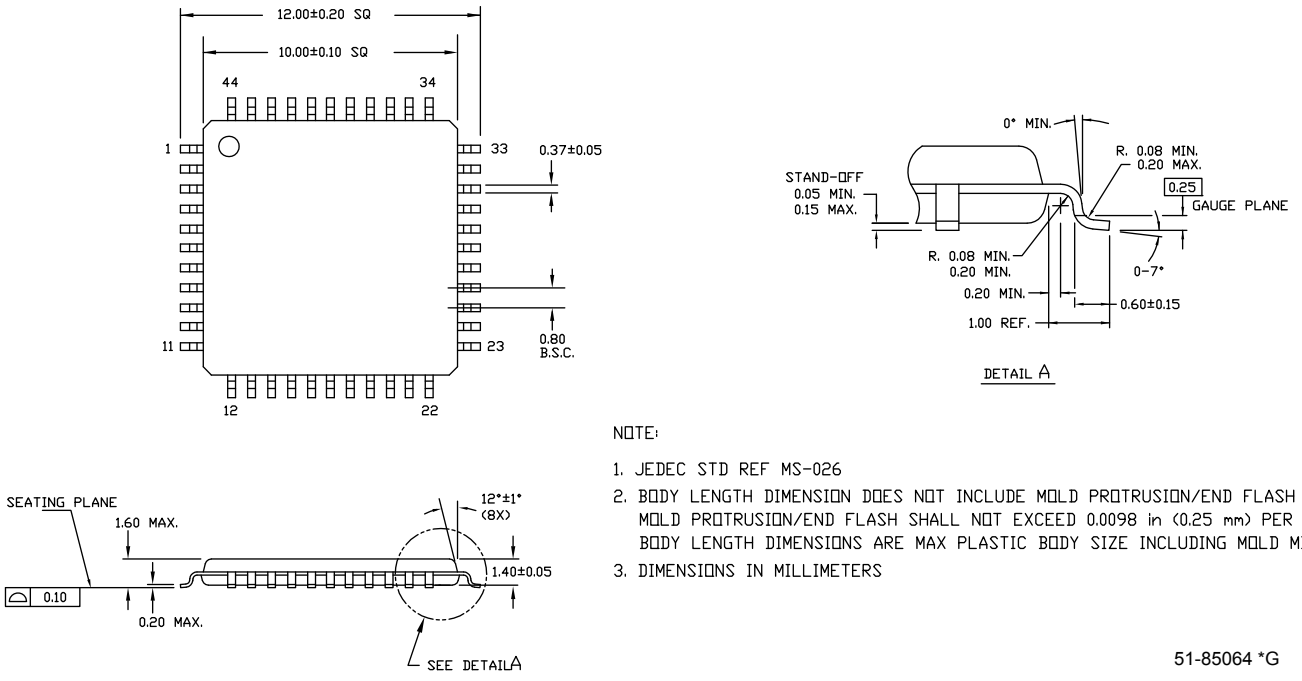
## Package Diagrams

**Figure 6. 48-pin TQFP Package Outline**




51-85135 *C

**Figure 7. 44-pin TQFP Package Outline**

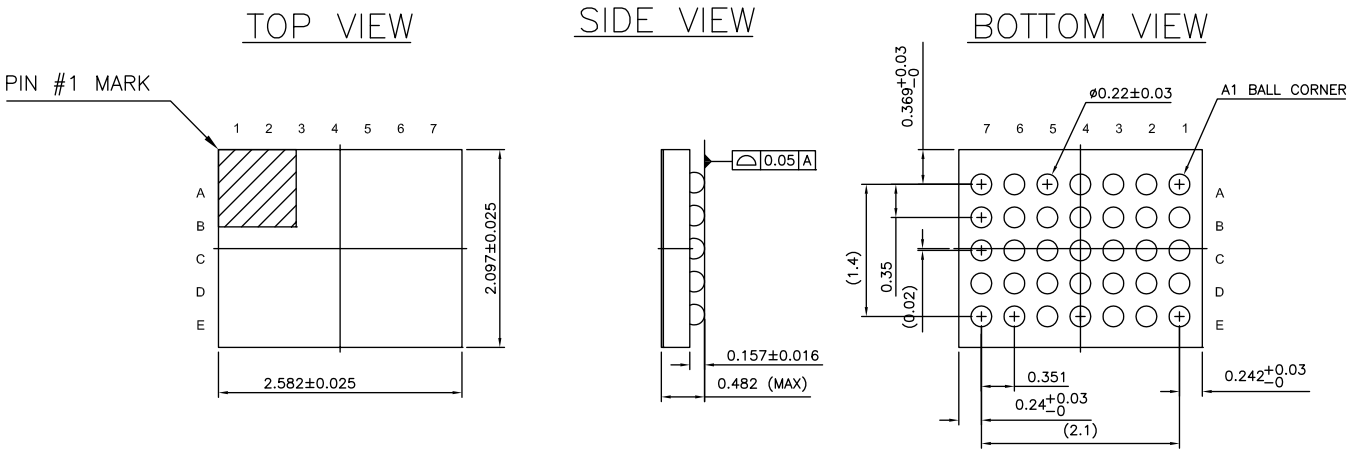



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

**Figure 10. 35-Ball WLCSP Package Outline**




ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-09958 *C

**Table 42. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

**Table 42. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

## Revision History

| Description Title: PSoC® 4: PSoC 4100S Family Datasheet Programmable System-on-Chip (PSoC)<br>Document Number: 002-00122 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 4883809 | WKA | 08/28/2015 | New datasheet |
| *A | 4992376 | WKA | 10/30/2015 | Updated Pinouts.<br>Added $V_{DDD}$ ≥ 2.2V at –40 °C under Conditions for specs SID247A, SID90, SID92.<br>Updated Table 15.<br>Updated Ordering Information. |
| *B | 5037826 | SLAN | 12/08/2015 | Changed datasheet status to Preliminary |
| *C | 5060691 | WKA | 12/22/2015 | Updated SCBs from 2 to 3.<br>Updated SRAM size to 8 KB.<br>Changed WLCSP package to 35-ball WLCSP.<br>Updated Pin List and Alternate Pin Functions.<br>Updated Ordering Information. |
| *D | 5139206 | WKA | 02/16/2016 | Added Errata.<br>Added 35 WLCSP package details.<br>Updated theta $J_A$ and $J_C$ values for all packages.<br>Updated copyright information at the end of the document. |
| *E | 5173961 | WKA | 03/15/2016 | Updated values for SID79, BID194. SID175, and SID176.<br>Updated CSD and IDAC Specifications.<br>Updated 10-bit CapSense ADC Specifications. |
| *F | 5330930 | WKA | 07/27/2016 | Updated CSD and IDAC Specifications.<br>Updated 10-bit CapSense ADC Specifications.<br>Removed errata. |
| *G | 5473409 | WKA | 10/13/2016 | Added 44 TQFP pin and package details. |
| *H | 5561833 | WKA | 01/09/2017 | Updated Figure 3.<br>Changed PRGIO references to Smart I/O.<br>Updated DC Specifications.<br>Updated Ordering Information. |

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