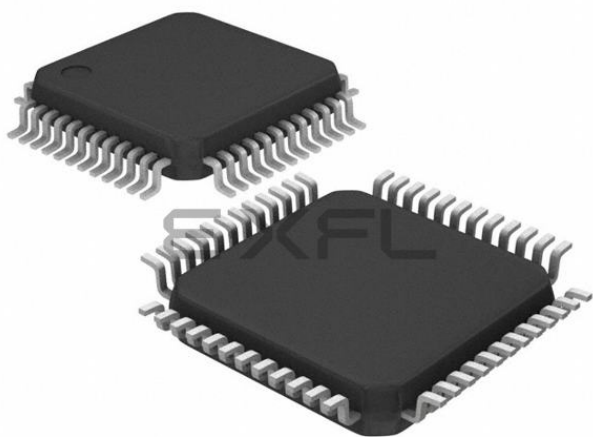




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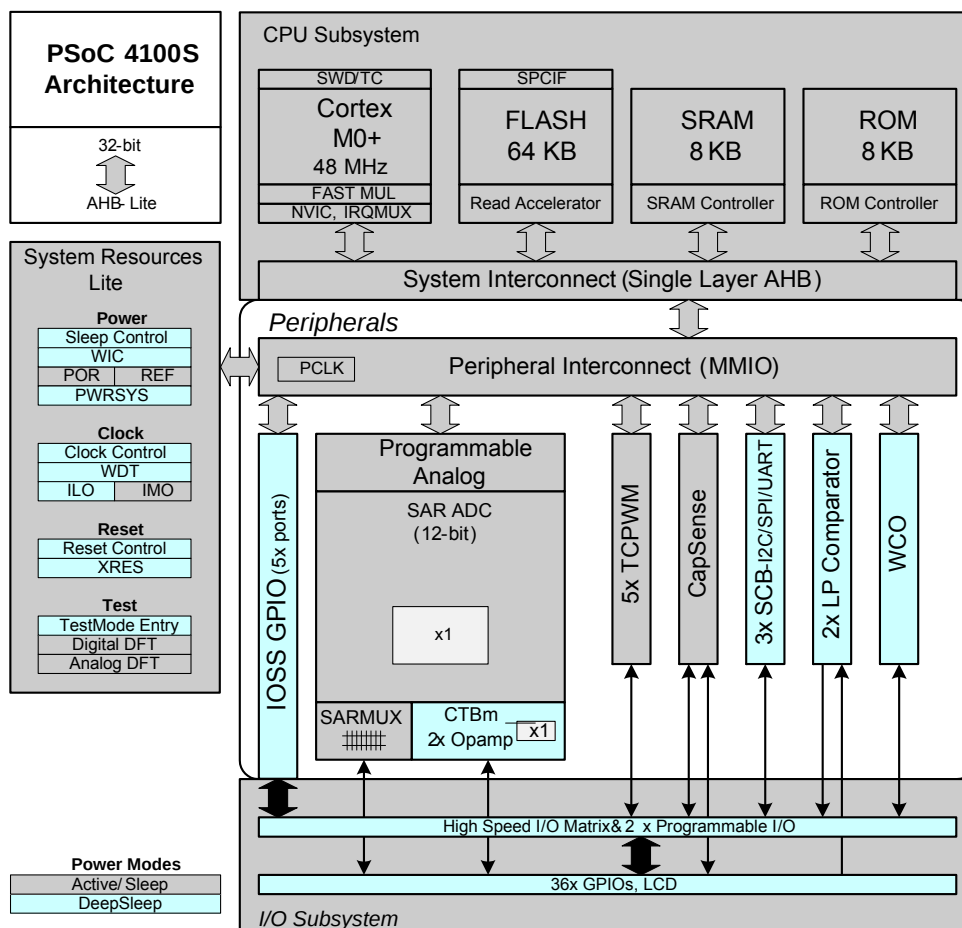
Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4145azi-s423

Contents

Functional Definition	4	Digital Peripherals	25
CPU and Memory Subsystem	4	Memory	28
System Resources	4	System Resources	28
Analog Blocks	5	Ordering Information.....	31
Fixed Function Digital	5	Packaging.....	34
GPIO	6	Package Diagrams	35
Special Function Peripherals.....	6	Acronyms	38
Pinouts	7	Document Conventions	40
Alternate Pin Functions	9	Units of Measure	40
Power	11	Revision History	41
Mode 1: 1.8 V to 5.5 V External Supply	11	Sales, Solutions, and Legal Information	42
Mode 2: 1.8 V ±5% External Supply.....	11	Worldwide Sales and Design Support.....	42
Development Support	12	Products	42
Documentation	12	PSoC® Solutions	42
Online	12	Cypress Developer Community.....	42
Tools.....	12	Technical Support	42
Electrical Specifications	13		
Absolute Maximum Ratings.....	13		
Device Level Specifications.....	13		
Analog Peripherals	17		

Figure 1. Block Diagram



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SRAM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

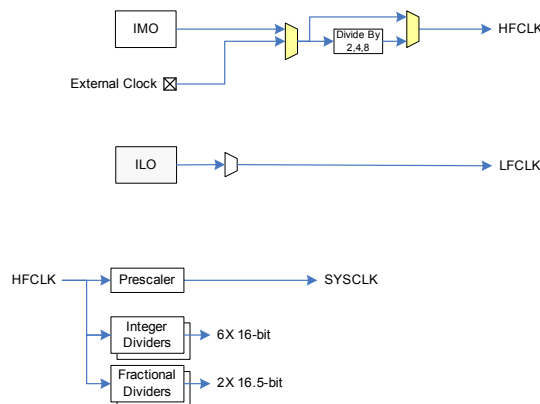
Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is $\pm$ 2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1. Pin List

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Development Support

The PSoC 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	−0.5	−	6	V	−
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	−0.5	−	1.95		−
SID3	V _{GPIO_ABS}	GPIO voltage	−0.5	−	V _{DD} +0.5		−
SID4	I _{GPIO_ABS}	Maximum current per GPIO	−25	−	25	mA	−
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	−0.5	−	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	−	−	V	−
BID45	ESD_CDM	Electrostatic discharge charged device model	500	−	−		−
BID46	LU	Pin current for latch-up	−140	−	140	mA	−

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V _{DD}	Power supply input voltage	1.8	−	5.5	V	Internally regulated supply
SID255	V _{DD}	Power supply input voltage (V _{CCD} = V _{DDD} = V _{DDA})	1.71	−	1.89		Internally unregulated supply
SID54	V _{CCD}	Output voltage (for core logic)	−	1.8	−		−
SID55	C _{EFC}	External regulator voltage bypass	−	0.1	−	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply bypass capacitor	−	1	−		X5R ceramic or better

Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25 °C.

SID10	I _{DD5}	Execute from flash; CPU at 6 MHz	−	1.8	2.7	mA	Max is at 85 °C and 5.5 V
SID16	I _{DD8}	Execute from flash; CPU at 24 MHz	−	3.0	4.75		Max is at 85 °C and 5.5 V
SID19	I _{DD11}	Execute from flash; CPU at 48 MHz	−	5.4	6.85		Max is at 85 °C and 5.5 V

Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} < 2.7$ V	$0.7 \times V_{DDD}$	–	–		–
SID242	V_{IL}	LVTTL input, $V_{DDD} < 2.7$ V	–	–	$0.3 \times V_{DDD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	$V_{DDD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	$V_{DDD} - 0.5$	–	–		$I_{OH} = 1$ mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DDD} = 3.0$ V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD} , Load = 25 pF

Notes

- V_{IH} must not exceed $V_{DDD} + 0.2$ V.
- Guaranteed by characterization.

Table 13. SAR Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	
SID102	A_VIND	Input voltage range - differential[	V _{SS}	–	V _{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F _{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A _{samp} /2	kHz	
SID111	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V _{REF} = 1 to V _{DD}
SID111A	A_INL	Integral non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V _{REF} = 1.71 to V _{DD}
SID111B	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V _{REF} = 1 to V _{DD}
SID112	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID112A	A_DNL	Differential non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V _{REF} = 1.71 to V _{DD}
SID112B	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F _{in} = 10 kHz
SID261	FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

CSD

Table 14. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), 25°C T_A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	$V_{DD} > 1.75\text{V}$ (with ripple), 25°C T_A , Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V _{REF}	Voltage reference for CSD and Comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	μA	LSB = 37.5-nA typ.

Table 15. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksp	–	–	2	LSB	V _{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksp	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 16. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

I²C

Table 17. Fixed I²C DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4		

Table 18. Fixed I²C AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Msp	–

Notes

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

Note

8. Guaranteed by characterization.

Table 19. SPI DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	μA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 20. SPI AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		T _{CPU} = 1/F _{CPU}
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

Table 21. UART DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	I _{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	–

Table 22. UART AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	–

Table 23. LCD Direct Drive DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I _{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD _{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I _{LCDOP1}	LCD system operating current V _{bias} = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I _{LCDOP2}	LCD system operating current V _{bias} = 3.3 V	–	2	–		32 × 4 segments. 50 Hz. 25 °C

Table 24. LCD Direct Drive AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	–

Note

9. Guaranteed by characterization.

Memory

Table 25. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[10]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[10]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[10]	Bulk erase time (64 KB)	–	–	35		–
SID180 ^[11]	T _{DEVPROG} ^[10]	Total device program time	–	–	7	Seconds	–
SID181 ^[11]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[11]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[11]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[11]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[11]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 28. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[11]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[11]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

11. Guaranteed by characterization.

SWD Interface

Table 29. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCCLK $\leq$ 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCCLK $\leq$ 1/3 CPU clock frequency
SID215 ^[12]	T_SWDI_SETUP	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–	ns	–
SID216 ^[12]	T_SWDI_HOLD	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–		–
SID217 ^[12]	T_SWDO_VALID	$T = 1/f_{\text{SWDCCLK}}$	–	–	$0.5 \cdot T$		–
SID217A ^[12]	T_SWDO_HOLD	$T = 1/f_{\text{SWDCCLK}}$	1	–	–		–

Internal Main Oscillator

Table 30. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

Table 31. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	–
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 32. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[12]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	–

Table 33. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[12]	T _{STARTILO1}	ILO startup time	–	–	2	ms	–
SID236 ^[12]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	–
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	–

Note

12. Guaranteed by characterization.

Table 34. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

Table 35. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 ^[13]	ExtClkDuty	Duty cycle; measured at V _{DD/2}	45	–	55	%	–

Table 36. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[13]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

Table 37. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

Note

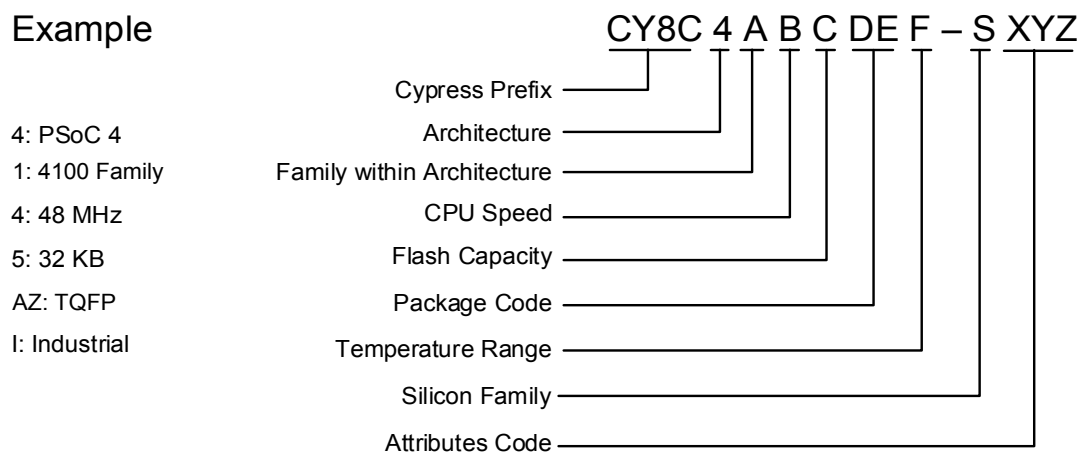
13. Guaranteed by characterization.

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

Example



TOP VIEW

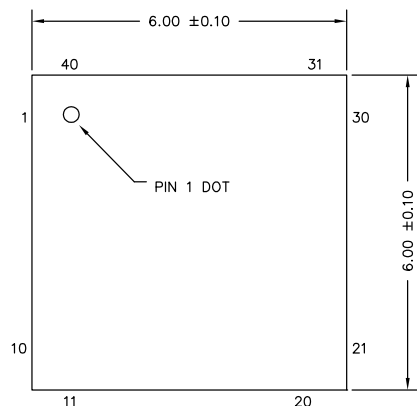


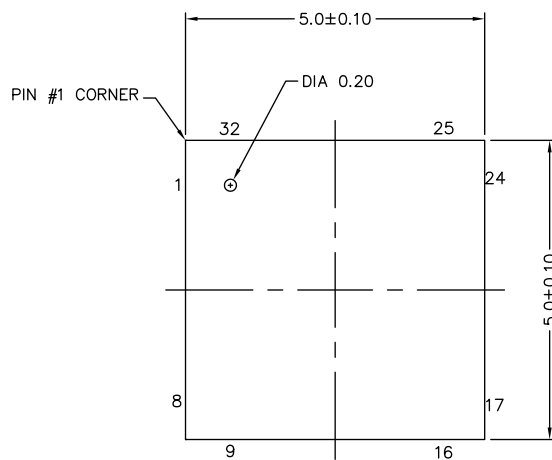
Figure 1 shows a vertical pipe with a series of rectangular slots. The slots are labeled "0.05 MAX" and "0.60 MAX". A small inset shows a semi-circular cross-section with a radius of "0.08".

[illegible]

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

TOP VIEW



Technical drawing of a square component with a central cross-hatched area. The drawing includes dimensions: overall width (3.500), overall height (3.500), central width (3.500 ± 0.100), and central height (3.500 ± 0.100). It also shows fillet radii (R0.15 [4X] and R0.20), a central hole (PIN #1 ID), and various other dimensions like 0.250, 0.450, 0.500 TYP, and 0.400 ± 0.100. A note "SEE NOTE 1" is present in the center.

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

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