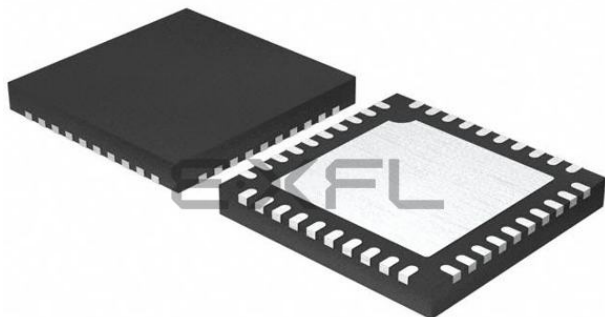




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

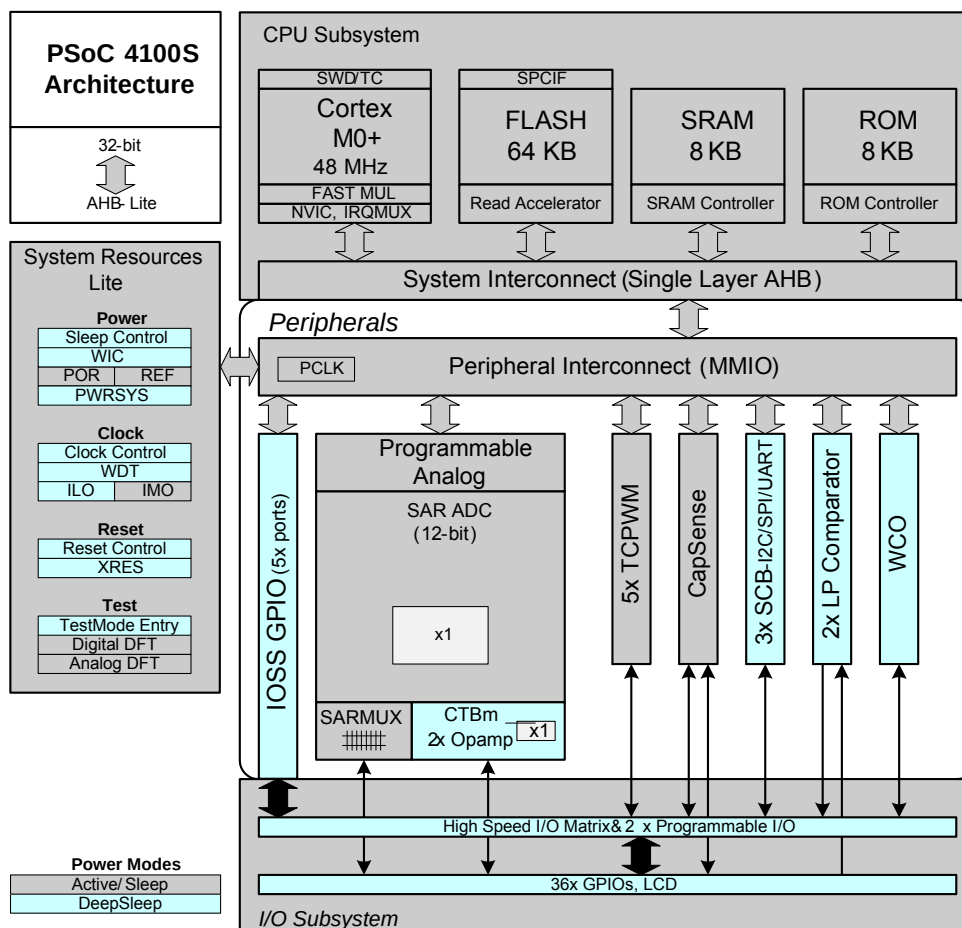
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4146lqi-s433

Figure 1. Block Diagram



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SRAM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

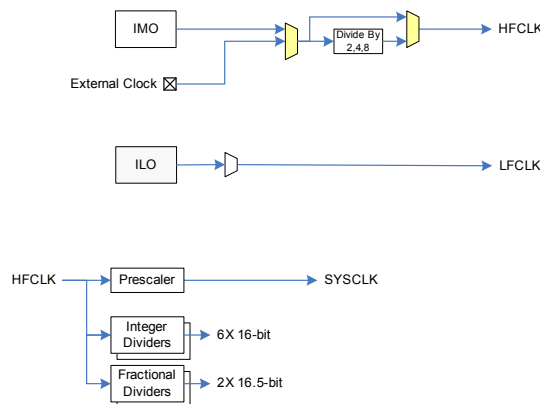
Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC 4100S MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is $\pm$ 2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

Table 1. Pin List

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				

Table 1. Pin List *(continued)*

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
19	P3.6	17	P3.6	16	P3.6				
20	P3.7	18	P3.7	17	P3.7				
21	VDDD	19	VDDD						
22	P4.0	20	P4.0	18	P4.0	13	P4.0	B1	P4.0
23	P4.1	21	P4.1	19	P4.1	14	P4.1	B2	P4.1
24	P4.2	22	P4.2	20	P4.2	15	P4.2	A2	P4.2
25	P4.3	23	P4.3	21	P4.3	16	P4.3	A1	P4.3

Notes: Pins 11, 15, 26, and 27 are No Connects (NC) on the 48-pin TQFP.

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V $\pm$ 5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_miso:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Development Support

The PSoC 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	−0.5	−	6	V	−
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	−0.5	−	1.95		−
SID3	V _{GPIO_ABS}	GPIO voltage	−0.5	−	V _{DD} +0.5		−
SID4	I _{GPIO_ABS}	Maximum current per GPIO	−25	−	25	mA	−
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	−0.5	−	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	−	−	V	−
BID45	ESD_CDM	Electrostatic discharge charged device model	500	−	−		−
BID46	LU	Pin current for latch-up	−140	−	140	mA	−

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V _{DD}	Power supply input voltage	1.8	−	5.5	V	Internally regulated supply
SID255	V _{DD}	Power supply input voltage (V _{CCD} = V _{DDD} = V _{DDA})	1.71	−	1.89		Internally unregulated supply
SID54	V _{CCD}	Output voltage (for core logic)	−	1.8	−		−
SID55	C _{EFC}	External regulator voltage bypass	−	0.1	−	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply bypass capacitor	−	1	−		X5R ceramic or better

Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25 °C.

SID10	I _{DD5}	Execute from flash; CPU at 6 MHz	−	1.8	2.7	mA	Max is at 85 °C and 5.5 V
SID16	I _{DD8}	Execute from flash; CPU at 24 MHz	−	3.0	4.75		Max is at 85 °C and 5.5 V
SID19	I _{DD11}	Execute from flash; CPU at 48 MHz	−	5.4	6.85		Max is at 85 °C and 5.5 V

Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 6. GPIO AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T _{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V _{DD} , Cload = 25 pF
SID74	F _{GPIOOUT1}	GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F _{GPIOOUT2}	GPIO F _{OUT} ; 1.71 V ≤ V _{DD} ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F _{GPIOOUT3}	GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F _{GPIOOUT4}	GPIO F _{OUT} ; 1.71 V ≤ V _{DD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F _{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V _{DD} ≤ 5.5 V	–	–	48		90/10% V _{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V _{IH}	Input voltage high threshold	0.7 × V _{DD}	–	–	V	CMOS Input
SID78	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DD}		
SID79	R _{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C _{IN}	Input capacitance	–	–	7	pF	–
SID81 ^[5]	V _{HYSXRES}	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V _{DD} > 4.5 V
SID82	I _{DIODE}	Current through protection diode to V _{DD} /V _{SS}	–	–	100	μA	

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 ^[5]	T _{RESETWIDTH}	Reset pulse width	1	–	–	μs	–
BID194 ^[5]	T _{RESETWAKE}	Wake-up time from reset release	–	–	2.7	ms	–

Note

5. Guaranteed by characterization.

Table 9. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V _{IN}	Charge-pump on, V _{DDA} = 2.7 V	−0.05	−	V _{DDA} -0.2	V	−
SID282	V _{CM}	Charge-pump on, V _{DDA} = 2.7 V	−0.05	−	V _{DDA} -0.2		−
	V _{OUT}	V _{DDA} = 2.7 V					
SID283	V _{OUT_1}	power=hi, Iload=10 mA	0.5	−	V _{DDA} -0.5	V	−
SID284	V _{OUT_2}	power=hi, Iload=1 mA	0.2	−	V _{DDA} -0.2		−
SID285	V _{OUT_3}	power=med, Iload=1 mA	0.2	−	V _{DDA} -0.2		−
SID286	V _{OUT_4}	power=lo, Iload=0.1 mA	0.2	−	V _{DDA} -0.2		−
SID288	V _{OS_TR}	Offset voltage, trimmed	−1.0	±0.5	1.0	mV	High mode, input 0 V to V _{DDA} -0.2 V
SID288A	V _{OS_TR}	Offset voltage, trimmed	−	±1	−		Medium mode, input 0 V to V _{DDA} -0.2 V
SID288B	V _{OS_TR}	Offset voltage, trimmed	−	±2	−		Low mode, input 0 V to V _{DDA} -0.2 V
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	−10	±3	10	µV/C	High mode
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	−	±10	−	µV/C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	−	±10	−		Low mode
SID291	CMRR	DC	70	80	−	dB	Input is 0 V to V _{DDA} -0.2 V, Output is 0.2 V to V _{DDA} -0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	−		V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} -0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	−	72	−	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	−	28	−		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	−	15	−		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID297	C _{LOAD}	Stable up to max. load. Performance specs at 50 pF.	−	−	125	pF	−
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V _{DDA} = 2.7 V	6	−	−	V/µs	−

Table 9. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, $T_{rise}=T_{fall}$ (approx.)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	I _{DD_MED_M1}	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I _{DD_HI_M2}	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I _{DD_MED_M2}	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, Low current	–	15	–		25 °C

Table 9. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_7	G _{BW_HI_M1}	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_8	G _{BW_MED_M1}	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_9	G _{BW_LOW_M1}	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_10	G _{BW_HI_M2}	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_11	G _{BW_MED_M2}	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_12	G _{BW_LOW_M2}	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V _{DDA} -0.2 V
SID_DS_13	V _{OS_HI_M1}	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_14	V _{OS_MED_M1}	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_15	V _{OS_LOW_M2}	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_16	V _{OS_HI_M2}	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V _{DDA} -0.2 V
SID_DS_17	V _{OS_MED_M2}	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_18	V _{OS_LOW_M2}	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_19	I _{OUT_HI_M1}	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_20	I _{OUT_MED_M1}	Mode 1, Medium current	–	10	–		Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_21	I _{OUT_LOW_M1}	Mode 1, Low current	–	4	–		Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_22	I _{OUT_HI_M2}	Mode 2, High current	–	1	–		
SID_DS_23	I _{OU_MED_M2}	Mode 2, Medium current	–	1	–		
SID_DS_24	I _{OU_LOW_M2}	Mode 2, Low current	–	0.5	–		

Note

6. Guaranteed by characterization.

Table 10. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	V _{OFFSET1}	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	V _{OFFSET2}	Input offset voltage, Custom trim	–	–	±4		
SID86	V _{HYST}	Hysteresis when enabled	–	10	35		
SID87	V _{ICM1}	Input common mode voltage in normal mode	0	–	V _{DDD} -0.1	V	Modes 1 and 2
SID247	V _{ICM2}	Input common mode voltage in low power mode	0	–	V _{DDD}		
SID247A	V _{ICM3}	Input common mode voltage in ultra low power mode	0	–	V _{DDD} -1.15		V _{DDD} ≥ 2.2 V at –40 °C
SID88	C _{MRR}	Common mode rejection ratio	50	–	–	dB	V _{DDD} ≥ 2.7V
SID88A	C _{MRR}	Common mode rejection ratio	42	–	–		V _{DDD} ≤ 2.7V
SID89	I _{CMP1}	Block current, normal mode	–	–	400	μA	
SID248	I _{CMP2}	Block current, low power mode	–	–	100		
SID259	I _{CMP3}	Block current in ultra low-power mode	–	–	6		V _{DDD} ≥ 2.2 V at –40 °C
SID90	Z _{CMP}	DC Input impedance of comparator	35	–	–	MΩ	

Table 11. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	μs	V _{DDD} ≥ 2.2 V at –40 °C

Table 12. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 13. SAR Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.

Table 13. SAR Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	
SID102	A_VIND	Input voltage range - differential[	V _{SS}	–	V _{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F _{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A _{samp} /2	kHz	
SID111	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V _{REF} = 1 to V _{DD}
SID111A	A_INL	Integral non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V _{REF} = 1.71 to V _{DD}
SID111B	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V _{REF} = 1 to V _{DD}
SID112	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID112A	A_DNL	Differential non linearity. V _{DD} = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V _{REF} = 1.71 to V _{DD}
SID112B	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F _{in} = 10 kHz
SID261	FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

CSD

Table 14. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), 25°C T_A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	$V_{DD} > 1.75\text{V}$ (with ripple), 25°C T_A , Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V _{REF}	Voltage reference for CSD and Comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1 (7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1 (7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1 (7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1 (7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	μA	LSB = 37.5-nA typ.

Table 14. CSD and IDAC Specifications (continued)

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 15. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V _{SSA}	–	V _{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSR	Power supply rejection ratio	–	60	–	dB	In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = F _{clk} /(2 ^{N+2}). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksp/s including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = F _{clk} /(2 ^{N+2}). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time.

Memory

Table 25. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[10]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[10]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[10]	Bulk erase time (64 KB)	–	–	35		–
SID180 ^[11]	T _{DEVPROG} ^[10]	Total device program time	–	–	7	Seconds	–
SID181 ^[11]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[11]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[11]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[11]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[11]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 28. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[11]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[11]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

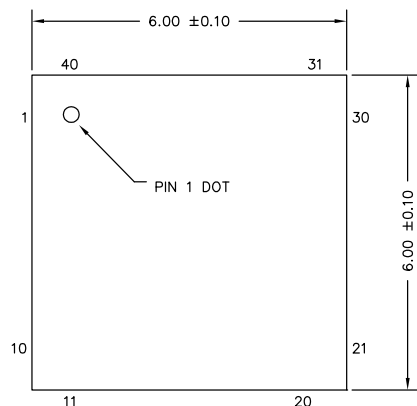
11. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC 4100S family are listed in the following table.

Category	MPN	Features														Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-WLCSP (0.35mm pitch)	32-QFN	40-QFN	48-TQFP	44-TQFP	
4124	CY8C4124FNI-S403	24	16	4	2	0	1	0		2	5	2	8	31	X					
	CY8C4124FNI-S413	24	16	4	2	1	1	0		2	5	2	16	31	X					
	CY8C4124LQI-S412	24	16	4	2	1	1	0		2	5	2	16	27		X				
	CY8C4124LQI-S413	24	16	4	2	1	1	0		2	5	2	16	34			X			
	CY8C4124AZI-S413	24	16	4	2	1	1	0		2	5	2	16	36				X		
	CY8C4124FNI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	31	X					
	CY8C4124LQI-S432	24	16	4	2	1	1	1	806 ksps	2	5	2	16	27		X				
	CY8C4124LQI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	34			X			
4125	CY8C4124AZI-S433	24	16	4	2	1	1	1	806 ksps	2	5	2	16	36				X		
	CY8C4125FNI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	31	X					
	CY8C4125LQI-S422	24	32	4	2	0	1	1	806 ksps	2	5	2	16	27		X				
	CY8C4125LQI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	34			X			
	CY8C4125AZI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36				X		
	CY8C4125AXI-S423	24	32	4	2	0	1	1	806 ksps	2	5	2	16	36					X	
	CY8C4125FNI-S413	24	32	4	2	1	1	0		2	5	2	16	31	X					
	CY8C4125LQI-S412	24	32	4	2	1	1	0		2	5	2	16	27		X				
	CY8C4125LQI-S413	24	32	4	2	1	1	0		2	5	2	16	34			X			
	CY8C4125AZI-S413	24	32	4	2	1	1	0		2	5	2	16	36				X		
	CY8C4125FNI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	31	X					
	CY8C4125LQI-S432	24	32	4	2	1	1	1	806 ksps	2	5	2	16	27		X				
	CY8C4125LQI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	34			X			
	CY8C4125AZI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36				X		
CY8C4125AXI-S433	24	32	4	2	1	1	1	806 ksps	2	5	2	16	36					X		
4126	CY8C4126AZI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36				X		
	CY8C4126AXI-S423	24	64	8	2	0	1	1	806 ksps	2	5	3	16	36					X	
	CY8C4126AZI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36				X		
	CY8C4126AXI-S433	24	64	8	2	1	1	1	806 ksps	2	5	3	16	36					X	
4145	CY8C4145AZI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36				X		
	CY8C4145AXI-S423	48	32	4	2	0	1	1	1 Msps	2	5	2	16	36					X	
	CY8C4145AXI-S433	48	32	4	2	1	1	1	1 Msps	2	5	2	16	36					X	
4146	CY8C4146FNI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	31	X					
	CY8C4146LQI-S422	48	64	8	2	0	1	1	1 Msps	2	5	3	16	27		X				
	CY8C4146LQI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	34			X			
	CY8C4146AZI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36				X		
	CY8C4146AXI-S423	48	64	8	2	0	1	1	1 Msps	2	5	3	16	36					X	
	CY8C4146FNI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	31	X					
	CY8C4146LQI-S432	48	64	8	2	1	1	1	1 Msps	2	5	3	16	27		X				
	CY8C4146LQI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	34			X			
	CY8C4146AZI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36				X		
	CY8C4146AXI-S433	48	64	8	2	1	1	1	1 Msps	2	5	3	16	36					X	

TOP VIEW



Technical drawing of a vertical component. The drawing shows a long vertical section with a series of small rectangular features along its length. At the top, there is a semi-circular feature with a dimension of 0.08. Below this, there are two horizontal lines with dimensions 0.05 MAX and 0.60 MAX. The drawing is labeled with '0.08', '0.05 MAX', and '0.60 MAX'.

[illegible]

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

TOP VIEW

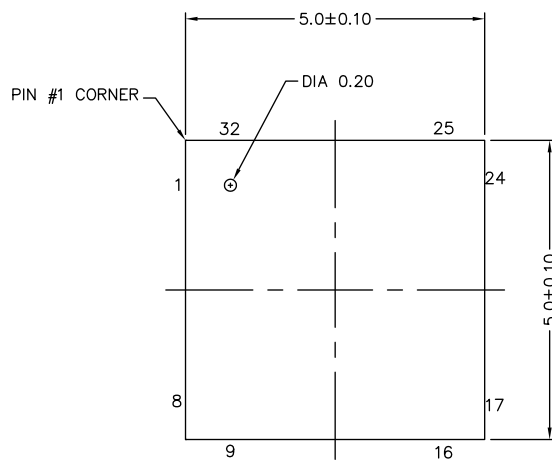


Figure 1 is a dimensional drawing of the test specimen. It shows a vertical rectangular specimen with a horizontal line across its center labeled "SEATING PLANE". Above the seating plane, there are three horizontal dimensions: a top flange with a thickness of $0.02 \begin{smallmatrix} +0.025 \\ -0.0 \end{smallmatrix}$, a middle section with a height of (0.15) , and a lower section with a height of 0.550 ± 0.05 . Below the seating plane, there is a vertical dimension of 3.5 . At the bottom, there is a circular feature with a diameter of $0.05 C$.

Technical drawing of a square component with a central cross-hatched area. The drawing includes dimensions for overall size (3.500), central area (3.500 ± 0.100), and various radii (R0.15, R0.20). It also shows a central area labeled "SEE NOTE 1" and a central area labeled "PIN #1 ID". Dimensions are given in inches, with some values in parentheses indicating typical or nominal values.

Key dimensions and features:

- Overall width: (3.500)
- Overall height: (3.500)
- Central area width: 3.500 ± 0.100
- Central area height: 3.500 ± 0.100
- Top-left corner radius: R0.15 [4X]
- Top-right corner radius: R0.20
- Top edge feature: 0.250 (+0.050 / -0.070)
- Right edge feature: 0.450
- Bottom edge feature: 0.400 ± 0.100
- Left edge feature: 0.500 TYP
- Central area label: SEE NOTE 1
- Central area label: PIN #1 ID

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt