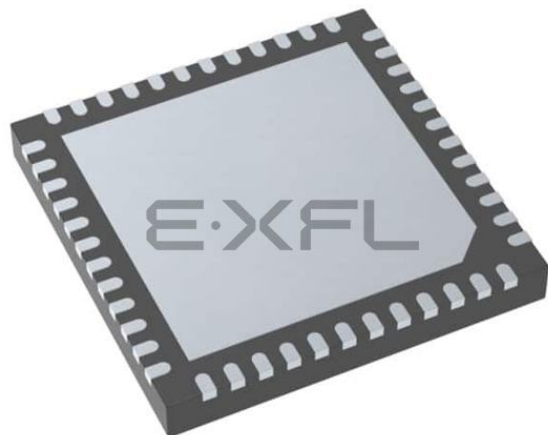




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	39
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431cbu6

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2 Description

The STM32L431xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L431xx devices embed high-speed memories (Flash memory up to 256 Kbyte, 64 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L431xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, two DAC channels, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Three I2Cs
- Three SPIs
- Three USARTs and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L431xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators. A VBAT input allows to backup the RTC and backup registers.

The STM32L431xx family offers nine packages from 32 to 100-pin packages.

Table 2. STM32L431xx family device features and peripheral counts

Peripheral	STM32L431Vx	STM32L431Rx		STM32L431Cx		STM32L431Kx	
Flash memory	256KB	128KB	256KB	128KB	256KB	128KB	256KB
SRAM	64KB						
Quad SPI	Yes						

3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to [Table 6: DMA implementation](#) for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 6. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.22.2 General-purpose timers (TIM2, TIM15, TIM16)

There are up to three synchronizable general-purpose timers embedded in the STM32L431xx (see [Table 9](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
It is a full-featured general-purpose timer:
TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler.
This timer features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. It can work with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.
The counter can be frozen in debug mode.
It has independent DMA request generation and support quadrature encoder.
- TIM15 and 16
They are general-purpose timers with mid-range features:
They have 16-bit auto-reload upcounters and 16-bit prescalers.
 - TIM15 has 2 channels and 1 complementary channel
 - TIM16 has 1 channel and 1 complementary channelAll channels can be used for input capture/output compare, PWM or one-pulse mode output.
The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.
The counters can be frozen in debug mode.

3.22.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.22.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

Table 16. Alternate function AF8 to AF15 (for AF0 to AF7 see [Table 15](#)) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	QUADSPI		SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_ BK1_IO1		COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS_ _DE	-	QUADSPI_ BK1_IO0		-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-		-	-	-	EVENTOUT
	PB3	-	-	-		-	SAI1_SCK_B	-	EVENTOUT
	PB4	-	TSC_G2_IO1	-		-	SAI1_MCLK_B	-	EVENTOUT
	PB5	-	TSC_G2_IO2	-		COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	-	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	-	TSC_G2_IO4	-		-	-	-	EVENTOUT
	PB8	-	CAN1_RX	-		SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-		SDMMC1_D5	SAI1_FS_A	-	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK		COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_ BK1_NCS		COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_ _DE	TSC_G1_IO1	-		SWPMI1_IO	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	-		SWPMI1_TX	SAI1_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-		SWPMI1_RX	SAI1_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-		SWPMI1_ SUSPEND	SAI1_SD_A	TIM15_CH2	EVENTOUT

Table 17. STM32L431xx memory map and peripheral register boundary addresses

Bus	Boundary address	Size(bytes)	Peripheral
APB1	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 1800 - 0x4000 27FF	4 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0400 - 0x4000 0FFF	3 KB	Reserved
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	140	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	100	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	100	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0 ⁽⁴⁾	
	Injected current on PA4, PA5	-5/0	
$\Sigma I_{INJ(PIN)} $	Total injected current (sum of all I/Os and control pins) ⁽⁵⁾	25	

1. All main power (V_{DD} , V_{DDA} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 18: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma |I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

Figure 19. V_{REFINT} versus temperature

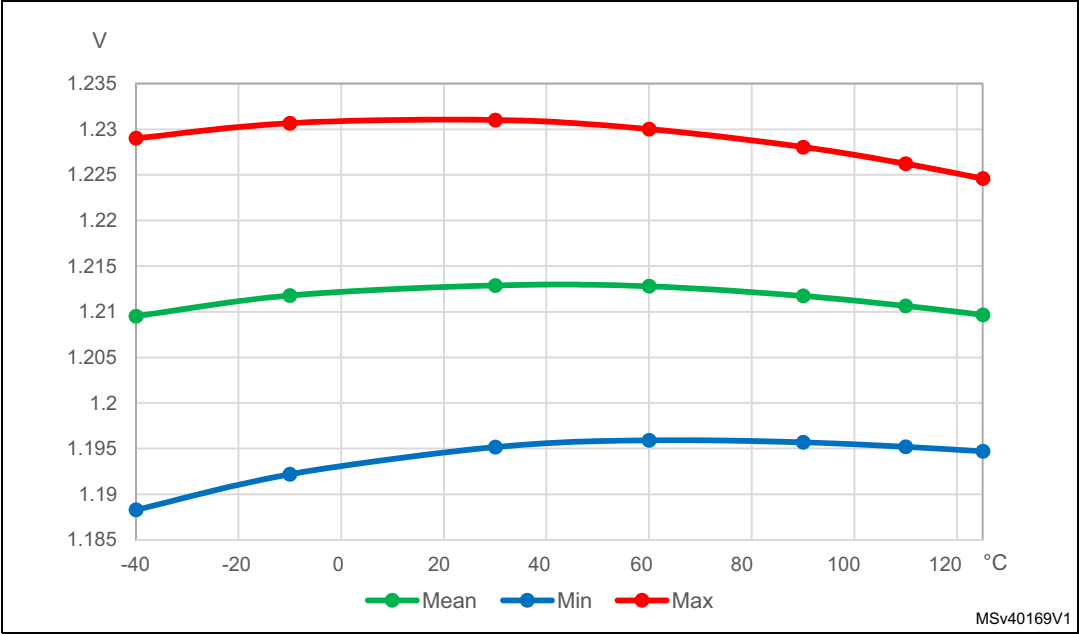


Table 31. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX ⁽¹⁾					Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD} (Sleep)	Supply current in sleep mode, pll ON above 48 MHz all peripherals disable	f _{HCLK} = f _{HSE} up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	0.8	0.9	1.0	1.3	mA
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	0.2	0.3	0.4	0.7	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	0.2	0.3	0.4	0.7	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	2.5	2.6	2.8	3.1	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	2.3	2.4	2.5	2.9	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.1	2.3	2.6	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	1.6	1.7	1.8	2.2	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	1.1	1.2	1.4	1.7	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	0.9	1.0	1.1	1.4	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	0.6	0.7	0.9	1.2	
I _{DD} (LPSleep)	Supply current in low-power sleep mode	f _{HCLK} = f _{MSI} all peripherals disable	2 MHz	71.8	80.7	125	200	350	91.1	122.7	191.3	341.5	653.5	μA	
			1 MHz	45.0	57.3	101	176	325	63.2	95.4	165.4	316.5	628.7		
			400 kHz	27.0	40.7	84.6	158	308	43.9	75.8	147.2	297.6	609.2		
			100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	67.9	140.9	290.8	602.4		

1. Guaranteed by characterization results, unless otherwise specified.

Table 38. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD} (VBAT)	Backup domain supply current	RTC disabled	1.8 V	2	12	66	193	540	5	30	165	482	1350	nA
			2.4 V	1	12	73	217	600	6	30	182	542	1500	
			3 V	5	16	92	266	731	12.5	40	230	665	1928	
			3.6 V	6	30	161	459	1 269	15	75	402	1147	3173	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	154	175	247	430	-	-	-	-	-	-	
			2.4 V	228	246	335	542	-	-	-	-	-	-	
			3 V	316	340	459	714	-	-	-	-	-	-	
			3.6 V	419	462	684	1 140	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz ⁽²⁾	1.8 V	256	297	385	558	823	-	-	-	-	-	
			2.4 V	345	381	477	673	906	-	-	-	-	-	
			3 V	455	495	603	836	1 085	-	-	-	-	-	
			3.6 V	591	642	824	1 207	1 733	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 40. Low-power mode wakeup timings⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.02	9.24	μs
			Wakeup clock HSI16 = 16 MHz	7.66	8.95	
		Range 2	Wakeup clock MSI = 24 MHz	8.5	9.54	
			Wakeup clock HSI16 = 16 MHz	7.75	8.95	
			Wakeup clock MSI = 4 MHz	12.06	13.16	
			Wakeup clock MSI = 4 MHz	12.06	13.16	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.45	6.79	
			Wakeup clock HSI16 = 16 MHz	6.9	7.98	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	7.36	
			Wakeup clock HSI16 = 16 MHz	6.9	7.9	
			Wakeup clock MSI = 4 MHz	13.1	13.31	
			Wakeup clock MSI = 4 MHz	13.1	13.31	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	12.2	18.35	μs
			Wakeup clock MSI = 4 MHz	19.14	25.8	
t_{WUSTBY} SRAM2	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	12.1	18.3	μs
			Wakeup clock MSI = 4 MHz	19.2	25.87	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	261.5	315.7	μs

1. Guaranteed by characterization results.

Table 41. Regulator modes transition times⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode ⁽²⁾	Code run with MSI 2 MHz	5	7	μs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2 ⁽³⁾	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.

2. Time until REGLPF flag is cleared in PWR_SR2.

3. Time until VOSF flag is cleared in PWR_SR2.

Table 42. Wakeup time using USART/LPUART⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	μs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 21](#).

Table 44. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7 V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram

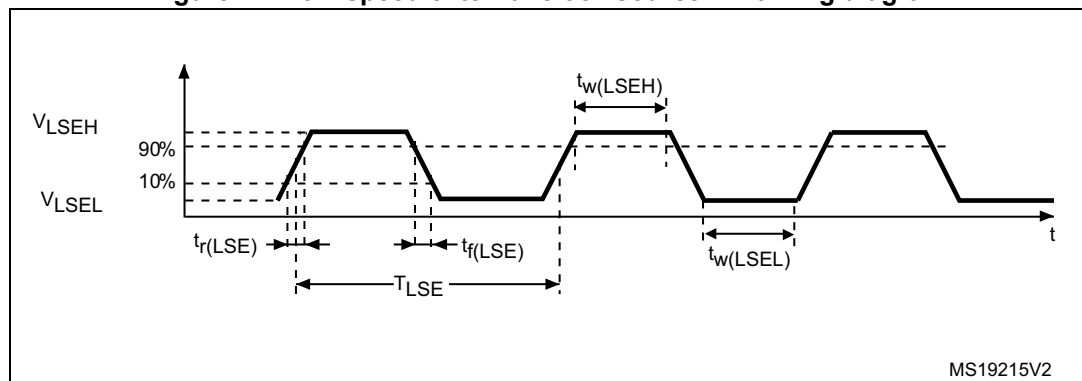
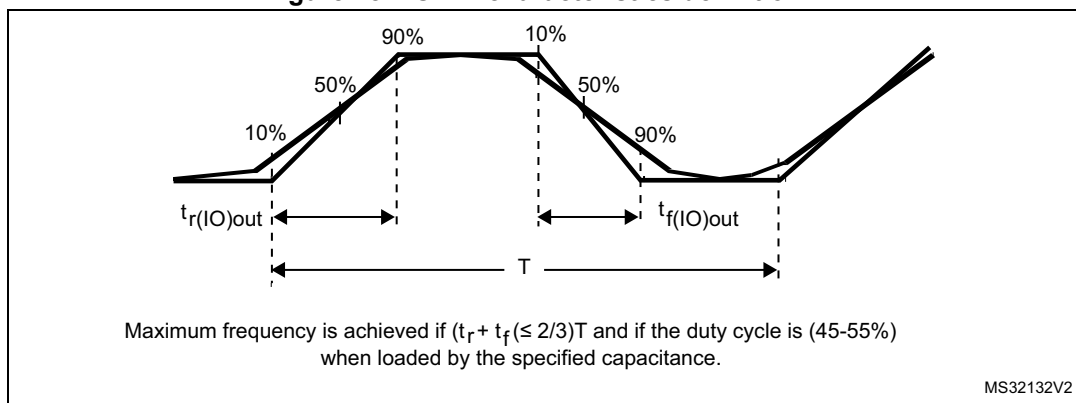


Figure 28. I/O AC characteristics definition⁽¹⁾

1. Refer to [Table 61: I/O AC characteristics](#).

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 62. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	350	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.17 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in [Table 64](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 21: General operating conditions](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 64. ADC characteristics^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
$V_{\text{REF+}}$	Positive reference voltage	$V_{\text{DDA}} \geq 2 \text{ V}$	2	-	V_{DDA}	V
		$V_{\text{DDA}} < 2 \text{ V}$	V_{DDA}			V
$V_{\text{REF-}}$	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_{s}	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Mps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	$f_{\text{ADC}} = 80 \text{ MHz}$ Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{\text{ADC}}$
V_{CMIN}	Input common mode	Differential mode	$(V_{\text{REF+}} + V_{\text{REF-}})/2 - 0.18$	$(V_{\text{REF+}} + V_{\text{REF-}})/2$	$(V_{\text{REF+}} + V_{\text{REF-}})/2 + 0.18$	V
$V_{\text{AIN}}^{(3)}$	Conversion voltage range ⁽²⁾	-	0	-	$V_{\text{REF+}}$	V
R_{AIN}	External input impedance	-	-	-	50	k Ω
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	$f_{\text{ADC}} = 80 \text{ MHz}$	1.45			μs
		-	116			$1/f_{\text{ADC}}$

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

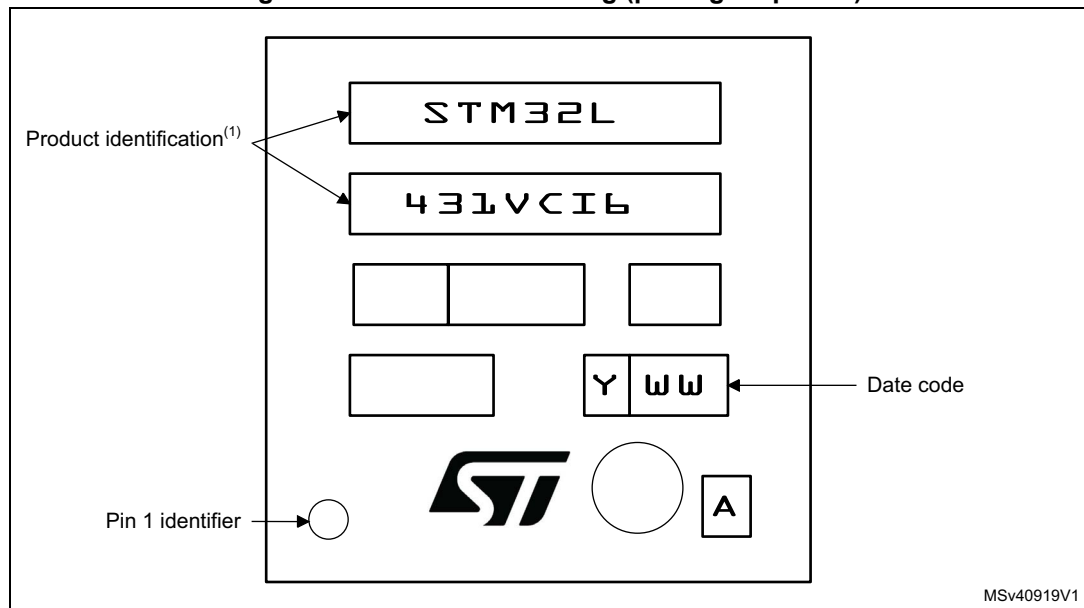
Table 65. Maximum ADC R_{AIN} ⁽¹⁾⁽²⁾

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels ⁽³⁾	Slow channels ⁽⁴⁾
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000

Table 66. ADC accuracy - limited test conditions 1⁽¹⁾(2)(3)

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	5	LSB
			Slow channel (max speed)	-	4	5	
		Differential	Fast channel (max speed)	-	3.5	4.5	
			Slow channel (max speed)	-	3.5	4.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	2.5	
			Slow channel (max speed)	-	1	2.5	
		Differential	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	4.5	
			Slow channel (max speed)	-	2.5	4.5	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
		Differential	Fast channel (max speed)	-	1	2	
			Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.4	10.5	-	bits
			Slow channel (max speed)	10.4	10.5	-	
		Differential	Fast channel (max speed)	10.8	10.9	-	
			Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	64.4	65	-	dB
			Slow channel (max speed)	64.4	65	-	
		Differential	Fast channel (max speed)	66.8	67.4	-	
			Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
		Differential	Fast channel (max speed)	67	68	-	
			Slow channel (max speed)	67	68	-	

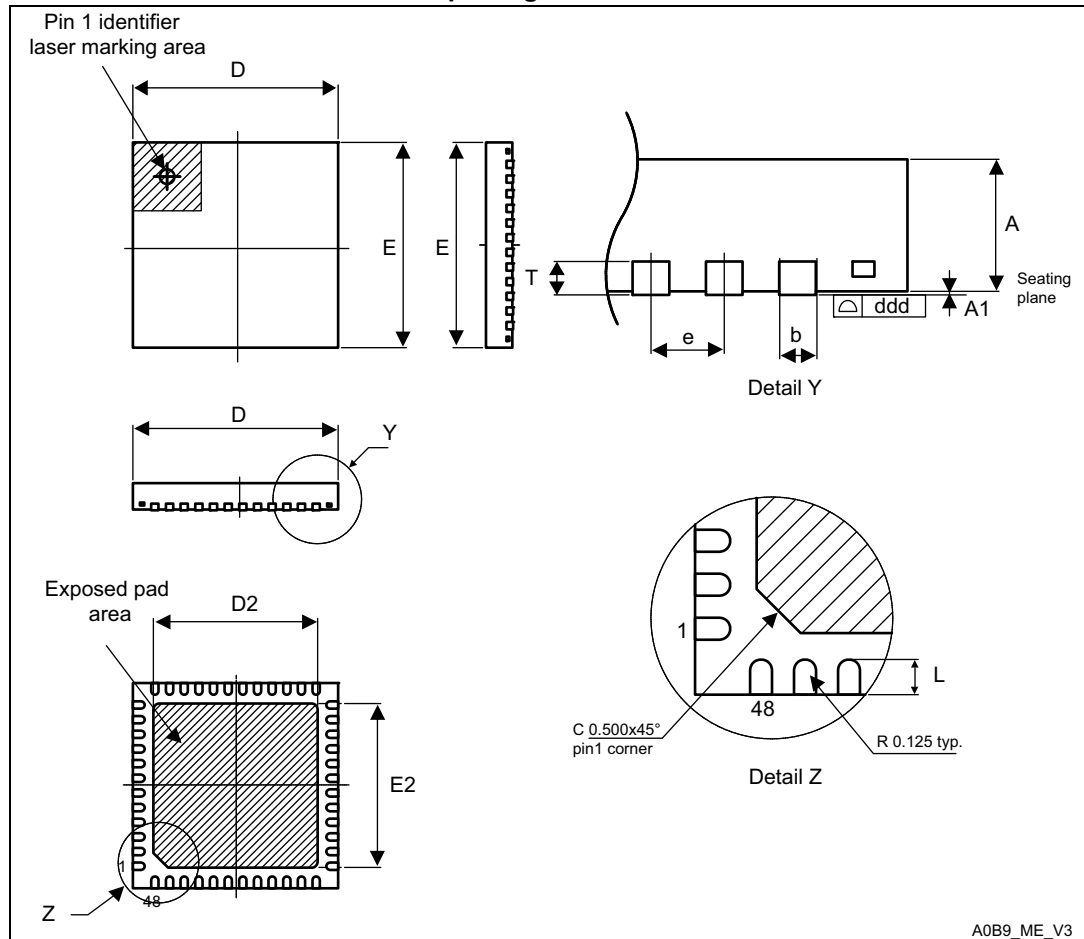
Figure 47. UFBGA100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

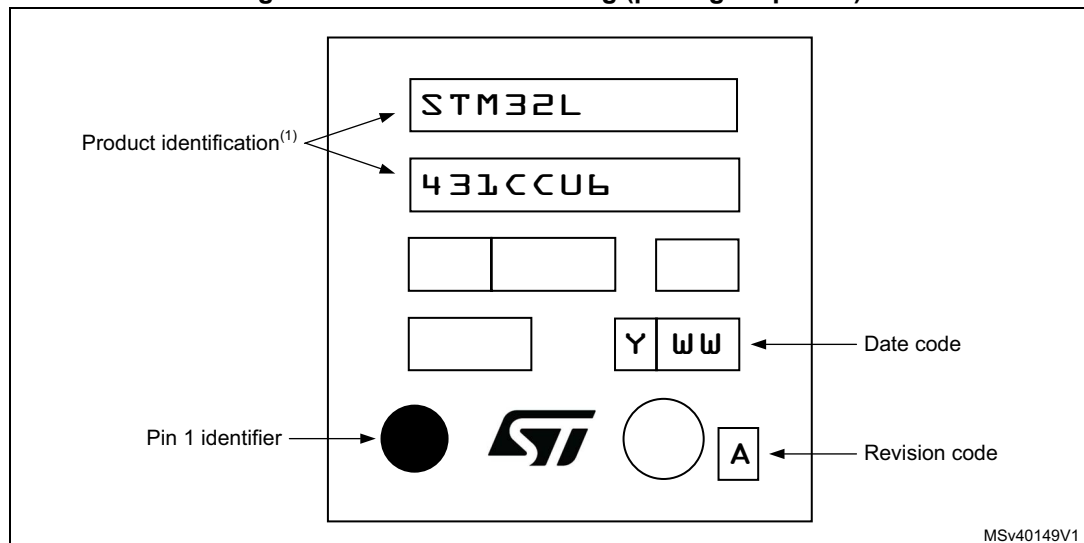
7.8 UFQFPN48 package information

Figure 63. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

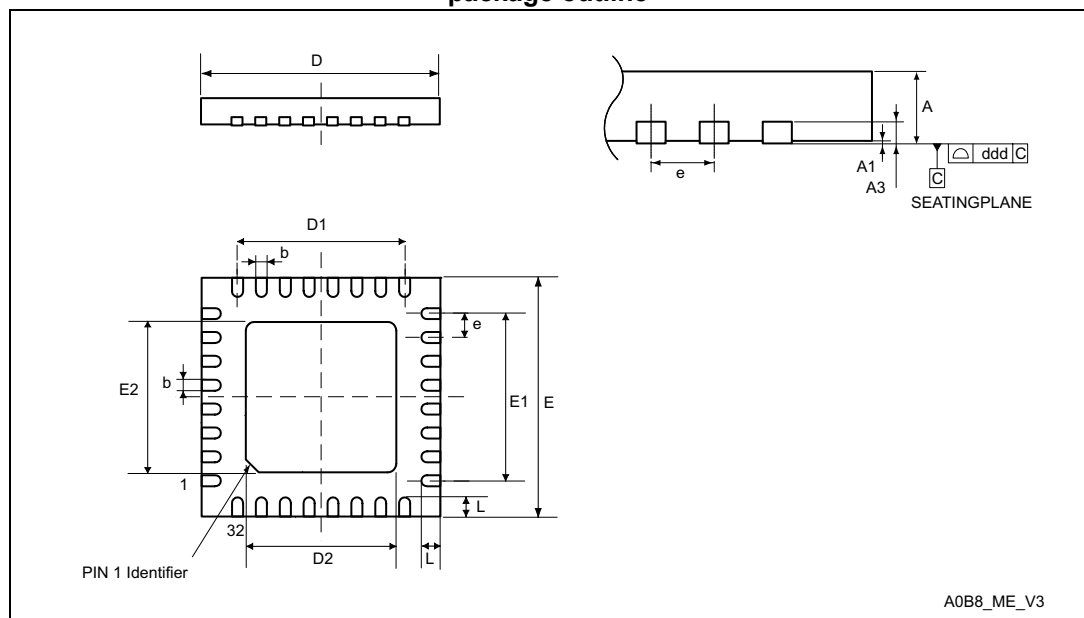
Figure 65. UFQFPN48 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.9 UFQFPN32 package information

Figure 66. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.