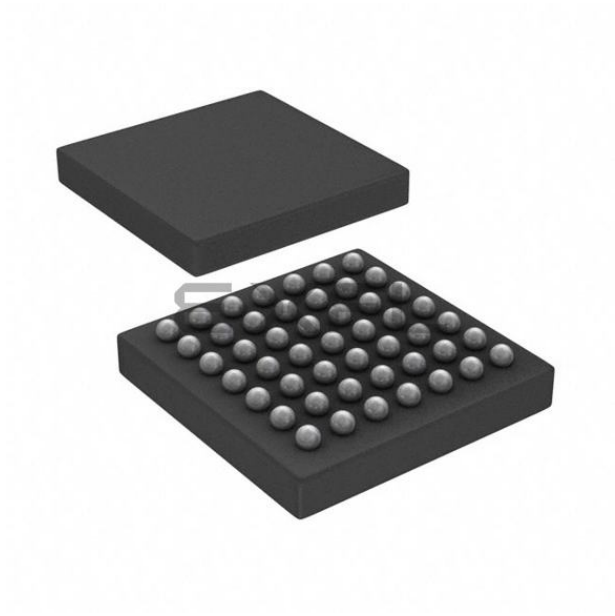

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	39
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.14x3.13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431cby7tr

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 16 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L431xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L431xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources:

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI

Table 4. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.24 Inter-integrated circuit interface (I2C)

The device embeds 3 I2C. Refer to *Table 10: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

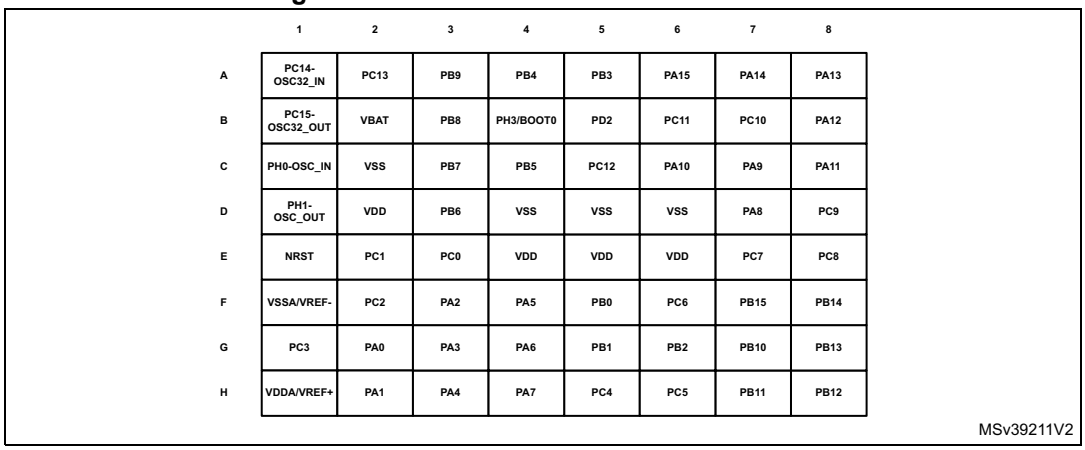
- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 3: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 10. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

1. X: supported

Figure 8. STM32L431Rx UFBGA64 ballout(1)

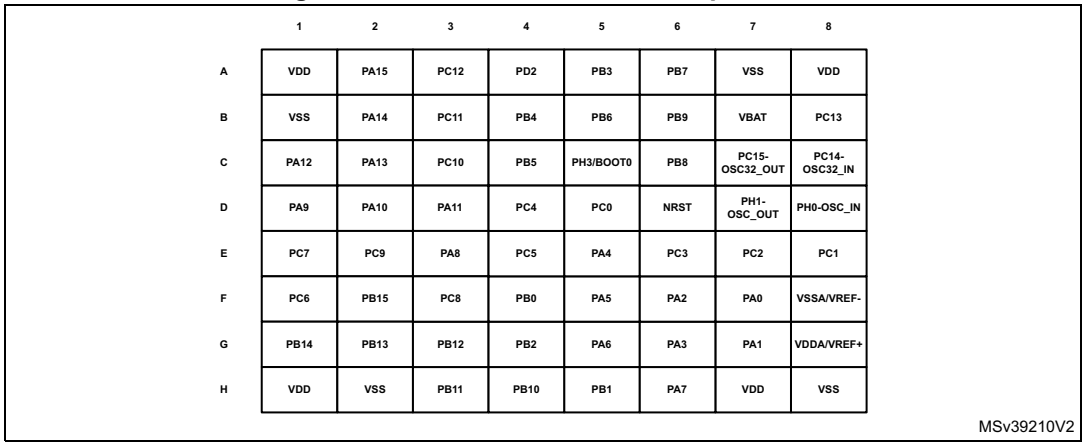


	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN	PC13	PB9	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PB8	PH3/BOOT0	PD2	PC11	PC10	PA12
C	PH0-OSC_IN	VSS	PB7	PB5	PC12	PA10	PA9	PA11
D	PH1-OSC_OUT	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	NRST	PC1	PC0	VDD	VDD	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

MSv39211V2

1. The above figure shows the package top view.

Figure 9. STM32L431Rx WLCSP64 pinout(1)

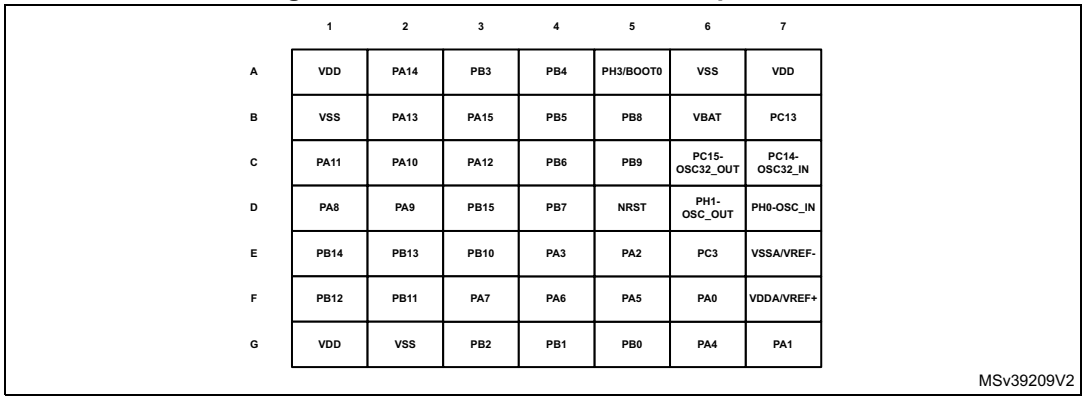


	1	2	3	4	5	6	7	8
A	VDD	PA15	PC12	PD2	PB3	PB7	VSS	VDD
B	VSS	PA14	PC11	PB4	PB6	PB9	VBAT	PC13
C	PA12	PA13	PC10	PB5	PH3/BOOT0	PB8	PC15-OSC32_OUT	PC14-OSC32_IN
D	PA9	PA10	PA11	PC4	PC0	NRST	PH1-OSC_OUT	PH0-OSC_IN
E	PC7	PC9	PA8	PC5	PA4	PC3	PC2	PC1
F	PC6	PB15	PC8	PB0	PA5	PA2	PA0	VSSA/VREF-
G	PB14	PB13	PB12	PB2	PA6	PA3	PA1	VDDA/VREF+
H	VDD	VSS	PB11	PB10	PB1	PA7	VDD	VSS

MSv39210V2

1. The above figure shows the package top view.

Figure 10. STM32L431Cx WLCSP49 pinout(1)



	1	2	3	4	5	6	7
A	VDD	PA14	PB3	PB4	PH3/BOOT0	VSS	VDD
B	VSS	PA13	PA15	PB5	PB8	VBAT	PC13
C	PA11	PA10	PA12	PB6	PB9	PC15-OSC32_OUT	PC14-OSC32_IN
D	PA8	PA9	PB15	PB7	NRST	PH1-OSC_OUT	PH0-OSC_IN
E	PB14	PB13	PB10	PA3	PA2	PC3	VSSA/VREF-
F	PB12	PB11	PA7	PA6	PA5	PA0	VDDA/VREF+
G	VDD	VSS	PB2	PB1	PB0	PA4	PA1

MSv39209V2

1. The above figure shows the package top view.

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	F3	39	E8	65	E10	PC8	I/O	FT	-	TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
-	-	-	-	E2	40	D8	66	D12	PC9	I/O	FT	-	TSC_G4_IO4, SDMMC1_D1, EVENTOUT	-
18	29	29	D1	E3	41	D7	67	D11	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
19	30	30	D2	D1	42	C7	68	D10	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
20	31	31	C2	D2	43	C6	69	C12	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, SAI1_SD_A, EVENTOUT	-
21	32	32	C1	D3	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, TIM1_BKIN2_COMP1, EVENTOUT	-
22	33	33	C3	C1	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, EVENTOUT	-
23	34	34	B2	C2	46	A8	72	A11	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-
-	35	35	B1	B1	47	D5	-	-	VSS	S	-	-	-	-
-	36	36	A1	A1	48	E5	73	C11	VDD	S	-	-	-	-
-	-	-	-	-	-	-	74	F11	VSS	S	-	-	-	-
-	-	-	-	-	-	-	75	G11	VDD	S	-	-	-	-
24	37	37	A2	B2	49	A7	76	A10	PA14 (JTCK-SWCLK)	I/O	FT	(3)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SWPMI1_RX, SAI1_FS_B, EVENTOUT	-

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
25	38	38	B3	A2	50	A6	77	A9	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, TSC_G3_IO1, SWPMI1_SUSPEND, EVENTOUT	-
-	-	-	-	C3	51	B7	78	B11	PC10	I/O	FT	-	SPI3_SCK, USART3_TX, TSC_G3_IO2, SDMMC1_D2, EVENTOUT	-
-	-	-	-	B3	52	B6	79	C10	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, TSC_G3_IO3, SDMMC1_D3, EVENTOUT	-
-	-	-	-	A3	53	C5	80	B10	PC12	I/O	FT	-	SPI3_MOSI, USART3_CK, TSC_G3_IO4, SDMMC1_CK, EVENTOUT	-
-	-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	SPI2_NSS, CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK, CAN1_TX, EVENTOUT	-
-	-	-	-	A4	54	B5	83	C8	PD2	I/O	FT	-	USART3_RTS_DE, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	SPI2_MISO, USART2_CTS, QUADSPI_BK2_NCS, EVENTOUT	-
-	-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	SPI2_MOSI, USART2_RTS_DE, QUADSPI_BK2_IO0, EVENTOUT	-
-	-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, EVENTOUT	-
-	-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX, QUADSPI_BK2_IO2, SAI1_SD_A, EVENTOUT	-

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	TIM16_CH1, EVENTOUT	-
-	-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	47	47	A6	A7	63	D4	99	D3	VSS	S	-	-	-	-
1	48	48	A7	A8	64	E4	100	C4	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0392 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 16*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	-	-	-	-	-	-	-	USART3_RTS_ DE
	PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS_ DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	-	-	-	USART2_RX
	PD7	-	-	-	-	-	-	-	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	-	-	-	USART3_CTS
	PD12	-	-	-	-	-	-	-	USART3_RTS_ DE
	PD13	-	-	-	-	-	-	-	-
	PD14	-	-	-	-	-	-	-	-
	PD15	-	-	-	-	-	-	-	-
Port E	PE0	-	-	-	-	-	-	-	-

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 16*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port E	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	-	-	-	-	-	-
	PE3	TRACED0	-	-	-	-	-	-	-
	PE4	TRACED1	-	-	-	-	-	-	-
	PE5	TRACED2	-	-	-	-	-	-	-
	PE6	TRACED3	-	-	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-	-	-
	PE9	-	TIM1_CH1	-	-	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.66	2.68	2.73	2.81	2.96	3.0	3.1	3.2	3.3	3.6	mA
				16 MHz	1.88	1.9	1.94	2.02	2.17	2.1	2.2	2.3	2.4	2.7	
				8 MHz	1.05	1.06	1.11	1.18	1.33	1.2	1.2	1.3	1.4	1.7	
				4 MHz	0.6	0.62	0.66	0.73	0.87	0.7	0.7	0.8	0.9	1.2	
				2 MHz	0.36	0.37	0.34	0.48	0.62	0.4	0.4	0.5	0.6	0.9	
				1 MHz	0.23	0.25	0.25	0.36	0.5	0.3	0.3	0.4	0.5	0.8	
				100 kHz	0.12	0.14	0.17	0.25	0.39	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.56	8.61	8.69	8.79	8.97	9.6	9.7	9.8	10.0	10.3	
				72 MHz	7.74	7.79	7.86	7.96	8.14	8.7	8.7	8.8	9.0	9.4	
				64 MHz	7.63	7.68	7.75	7.85	8.04	8.6	8.6	8.7	8.9	9.3	
				48 MHz	6.36	6.4	6.48	6.58	6.76	7.2	7.3	7.4	7.6	7.9	
				32 MHz	4.56	4.6	4.66	4.76	4.93	5.2	5.2	5.3	5.5	5.8	
				24 MHz	3.45	3.48	3.54	3.64	3.8	3.9	4.0	4.1	4.2	4.6	
				16 MHz	2.48	2.51	2.56	2.65	2.82	2.8	2.9	3.0	3.1	3.5	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	310	317	364	440	593	375.3	400.9	456.7	595.3	909.6	µA
				1 MHz	157	173	226	296	448	204.8	234.2	298.2	445.8	758.9	
				400 kHz	72.6	89	130	206	356	99.7	131.2	199.7	349.3	663.7	
				100 kHz	32.3	46	89.7	164	314	52.4	82.1	153.3	301.2	616.9	

1. Guaranteed by characterization results, unless otherwise specified.

Table 31. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	0.8	0.9	1.0	1.3	mA
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	0.2	0.3	0.4	0.7	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	0.2	0.3	0.4	0.7	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	2.5	2.6	2.8	3.1	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	2.3	2.4	2.5	2.9	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.1	2.3	2.6	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	1.6	1.7	1.8	2.2	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	1.1	1.2	1.4	1.7	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	0.9	1.0	1.1	1.4	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	0.6	0.7	0.9	1.2	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	71.8	80.7	125	200	350	91.1	122.7	191.3	341.5	653.5	µA
				1 MHz	45.0	57.3	101	176	325	63.2	95.4	165.4	316.5	628.7	
				400 kHz	27.0	40.7	84.6	158	308	43.9	75.8	147.2	297.6	609.2	
				100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	67.9	140.9	290.8	602.4	

1. Guaranteed by characterization results, unless otherwise specified.

Table 37. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	63	133	522	1 490	4 270	-	-	-	-	-	nA
			2.4 V	165	253	710	1 830	4 980	-	-	-	-	-	
			3 V	316	423	990	2 340	6 050	-	-	-	-	-	
			3.6 V	649	787	1 530	3 220	7 710	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	203	293	700	1 675	-	-	-	-	-	-	
			2.4 V	303	411	880	2 001	-	-	-	-	-	-	
			3 V	448	567	1 136	2 479	-	-	-	-	-	-	
			3.6 V	744	887	1 609	3 256	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	0.780	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz/ 80 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-8	dBµV
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	5	
			1 GHz to 2 GHz	8	
			EMI Level	2.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Table 66. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

6.3.18 Digital-to-Analog converter characteristics

Table 70. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.8	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 72. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Table 74. OPAMP characteristics(1) (continued)

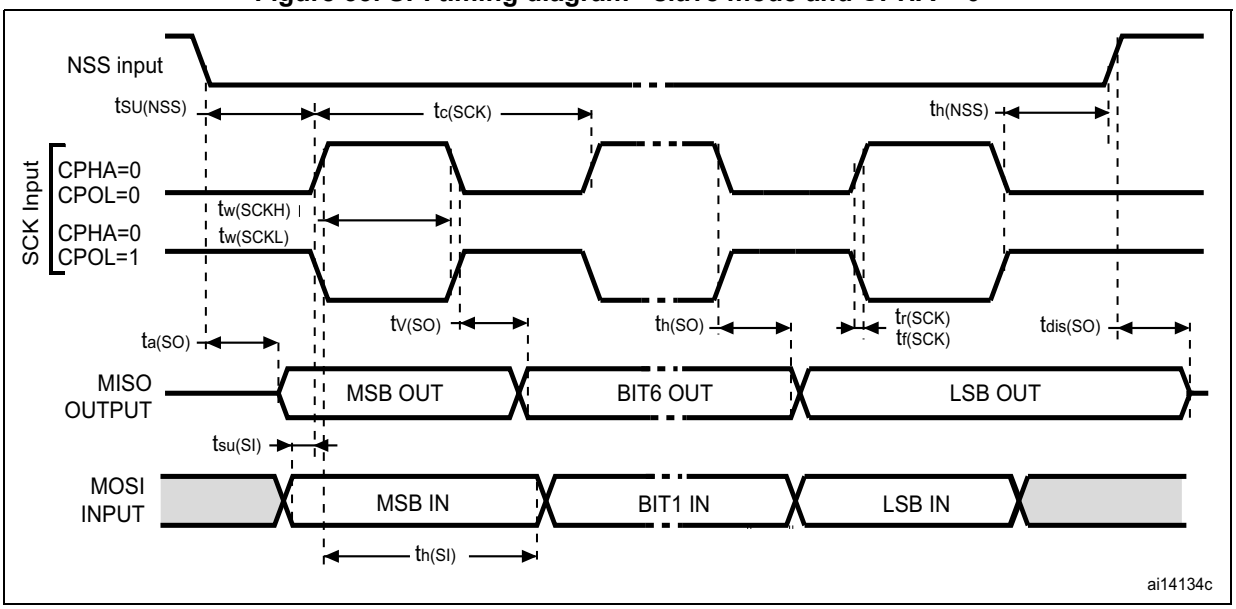
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GBW	Gain Bandwidth Product	Normal mode	V_{DDA} ≥ 2.4 V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	V_{DDA} < 2.4 V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	V_{DDA} ≥ 2.4 V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	V_{DDA} < 2.4 V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input		-	-	-(4)	nA
PGA gain(3)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	

Table 82. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	13.5	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	24	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

Figure 33. SPI timing diagram - slave mode and CPHA = 0



7.10.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L431xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 102* T_{Jmax} is calculated as follows:

– For LQFP64, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.562 °C = 102.562 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Part numbering*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (46°C/W × 447 mW) = 105-20.562 = 84.438 °C

Suffix 7: T_{Amax} = T_{Jmax} - (46°C/W × 447 mW) = 125-20.562 = 104.438 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.