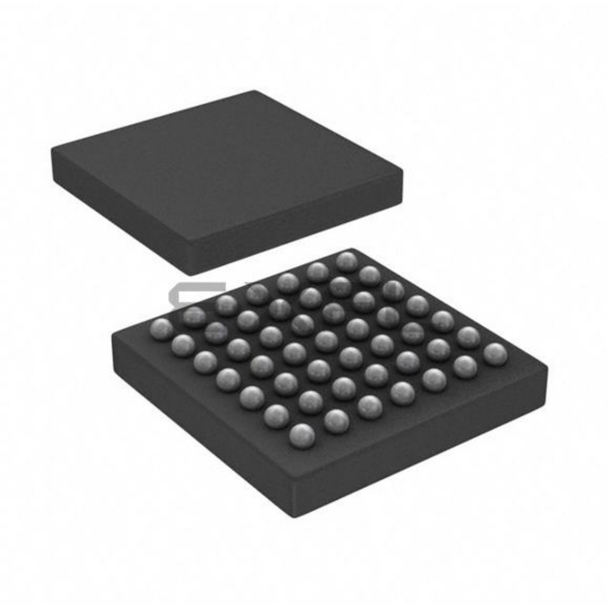

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	39
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.14x3.13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431ccy6tr

List of tables

3.4 Embedded Flash memory

STM32L431xx devices feature up to 256 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 128 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 67 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 37 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

3.24 Inter-integrated circuit interface (I2C)

The device embeds 3 I2C. Refer to *Table 10: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 3: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 10. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

1. X: supported

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
8	12	12	E5	F6	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4, LSCO
9	13	13	E4	G6	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	-	-	H8	18	C2	27	E3	VSS	S	-	-	-	-
-	-	-	-	H7	19	D2	28	H3	VDD	S	-	-	-	-
10	14	14	G6	E5	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
11	15	15	F5	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10, DAC1_OUT2
12	16	16	F4	G5	22	G4	31	L4	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
13	17	17	F3	H6	23	H4	32	M4	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
-	-	-	-	D4	24	H5	33	K5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	-	E4	25	H6	34	L5	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	F3	39	E8	65	E10	PC8	I/O	FT	-	TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
-	-	-	-	E2	40	D8	66	D12	PC9	I/O	FT	-	TSC_G4_IO4, SDMMC1_D1, EVENTOUT	-
18	29	29	D1	E3	41	D7	67	D11	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
19	30	30	D2	D1	42	C7	68	D10	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
20	31	31	C2	D2	43	C6	69	C12	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, SAI1_SD_A, EVENTOUT	-
21	32	32	C1	D3	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, TIM1_BKIN2_COMP1, EVENTOUT	-
22	33	33	C3	C1	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, EVENTOUT	-
23	34	34	B2	C2	46	A8	72	A11	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-
-	35	35	B1	B1	47	D5	-	-	VSS	S	-	-	-	-
-	36	36	A1	A1	48	E5	73	C11	VDD	S	-	-	-	-
-	-	-	-	-	-	-	74	F11	VSS	S	-	-	-	-
-	-	-	-	-	-	-	75	G11	VDD	S	-	-	-	-
24	37	37	A2	B2	49	A7	76	A10	PA14 (JTCK-SWCLK)	I/O	FT	(3)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, SWPMI1_RX, SAI1_FS_B, EVENTOUT	-

Table 16. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 15*)

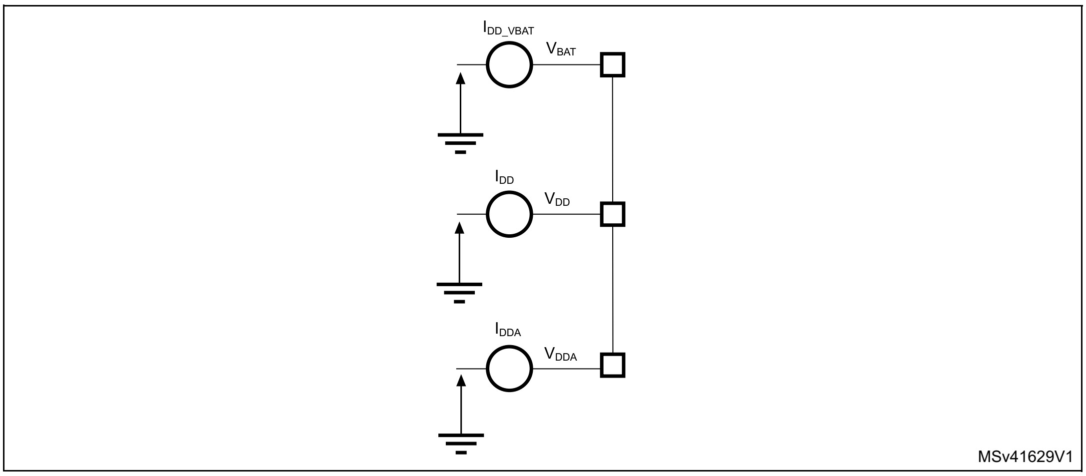
Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	QUADSPI		SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port A	PA0	-	-	-	-	COMP1_OUT	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	-	-	-		-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_ BK1_NCS		COMP2_OUT	-	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK		-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_ BK1_IO3		TIM1_BKIN_ COMP2	-	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_ BK1_IO2		COMP2_OUT	-	-	EVENTOUT
	PA8	-	-	-		SWPMI1_IO	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-		-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-			-	SAI1_SD_A	-	EVENTOUT
	PA11	-	CAN1_RX		-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX		-	-	-	-	EVENTOUT
	PA13	-	-		-	SWPMI1_TX	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	-	-	SWPMI1_RX	SAI1_FS_B	-	EVENTOUT
	PA15	-	TSC_G3_IO1	-		SWPMI1_ SUSPEND	-	-	EVENTOUT

Table 17. STM32L431xx memory map and peripheral register boundary addresses

Bus	Boundary address	Size(bytes)	Peripheral
APB2	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	V_{DDIOx}+0.3	V
		All I/O except TT_xx	-0.3	MIN(MIN(V_{DD}, V_{DDA})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP100	-	476	mW
		LQFP64	-	444	
		LQFP48	-	350	
		UFBGA100	-	350	
		UFBGA64	-	307	
		UFQFPN48	-	606	
		UFQFPN32	-	523	
		WLCSP64	-	434	
		WLCSP49	-	416	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation(5)	–40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation(5)	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version	–40	125	
		Suffix 3 version	–40	130	

Table 34. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	4.34	12.4	43.6	96.4	204	9.3	27.4	98.9	198.7	397.5	µA
			2.4 V	4.35	12.5	43.8	97	205	9.4	27.6	99.5	199.0	398.0	
			3 V	4.41	12.6	44.1	97.7	207	9.5	27.8	100.3	200.4	400.8	
			3.6 V	4.56	12.9	44.8	98.9	210	9.7	28.3	101.7	202.1	404.2	
I_{DD} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	4.63	12.7	43.9	96.8	205	9.9	28.0	99.5	198.9	397.8	µA
			2.4 V	4.78	12.8	44.2	97.4	206	10.1	28.3	100.3	199.5	399.0	
			3 V	4.93	13	44.6	98.1	207	10.4	28.7	101.2	200.9	401.9	
			3.6 V	5.05	13.4	45.3	99.5	210	10.8	29.4	102.8	202.5	405.0	
		RTC clocked by LSE bypassed, at 32768 Hz	1.8 V	4.7	12.8	44	96.9	205	-	-	-	-	-	
			2.4 V	4.95	13	44.4	97.6	206	-	-	-	-	-	
			3 V	5.33	13.6	45.4	99.1	209	-	-	-	-	-	
			3.6 V	6.91	16.1	48.8	103	216	-	-	-	-	-	
		RTC clocked by LSE quartz[2] in low drive mode	1.8 V	4.76	12.3	43.7	99.1	-	-	-	-	-	-	
			2.4 V	4.95	12.4	43.8	99.3	-	-	-	-	-	-	
			3 V	5.1	12.6	44.1	99.6	-	-	-	-	-	-	
			3.6 V	5.65	13	44.8	101	-	-	-	-	-	-	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See [3].	3 V	1.14	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See [3].	3 V	1.22	-	-	-	-	-	-	-	-	-	
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See [3].	3 V	1.20	-	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

Table 39. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB2	FW	0.2	0.2	0.2	µA/MHz
	SAI1 independent clock domain	2.3	1.8	1.9	
	SAI1 clock domain	2.1	1.8	2.0	
	SDMMC1 independent clock domain	4.7	3.9	3.9	
	SDMMC1 clock domain	2.5	1.9	1.9	
	SPI1	1.8	1.6	1.7	
	SYSCFG/VREFBUF/COMP	0.6	0.5	0.6	
	TIM1	8.1	6.5	7.6	
	TIM15	3.7	3.0	3.4	
	TIM16	2.7	2.1	2.6	
	USART1 independent clock domain	4.8	4.2	4.6	
	USART1 clock domain	1.5	1.3	1.7	
	All APB2 on	24.2	19.9	22.6	
ALL		94.8	76.5	94.0	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 40* are the latency between the event and the execution of the first user instruction.

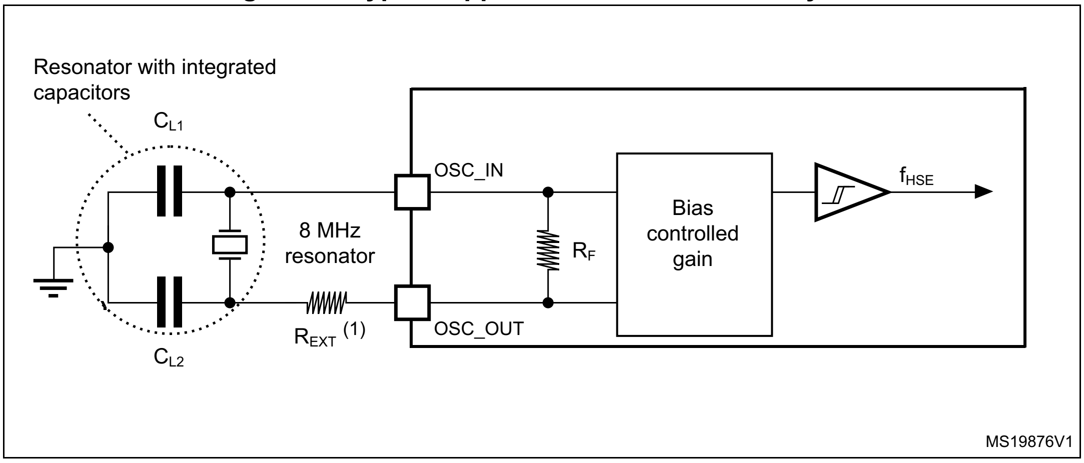
The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 40. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-	6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz	6	8.3	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Table 66. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 68. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 72. VREFBUF characteristics[(1)] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.22 Temperature sensor characteristics

Table 75. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 7: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.23 V_{BAT} monitoring characteristics

Table 76. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 77. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.24 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 102* T_{Jmax} is calculated as follows:

– For LQFP64, 46 °C/W

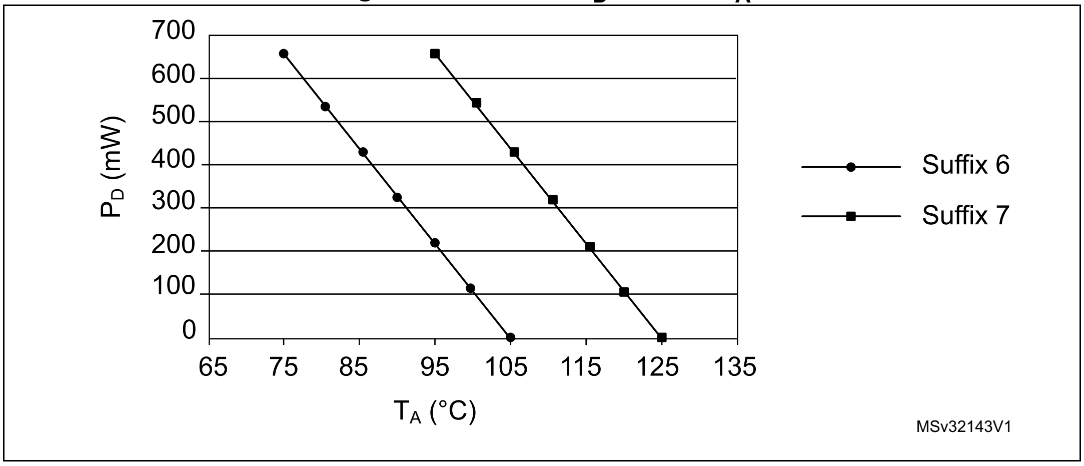
T_{Jmax} = 100 °C + (46 °C/W × 134 mW) = 100 °C + 6.164 °C = 106.164 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 69* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 69. LQFP64 P_D max vs. T_A



8 Part numbering

Table 103. STM32L431xx ordering information scheme

Example: STM32 L 431 C C T 6 TR

Device family

STM32 = ARM® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

431: STM32L431xx

Pin count

K = 32 pins

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

B = 128 kB of Flash memory

C = 256 KB of Flash memory

Package

T = LQFP ECOPACK®2

U = QFN ECOPACK®2

I = UFBGA ECOPACK®2

Y = CSP ECOPACK®2

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

Packing

TR = tape and reel

xxx = programmed parts